

Dual N-channel MOSFET

ELM14842AA-N

General description

ELM14842AA-N uses advanced trench technology to provide excellent $R_{ds(on)}$ and low gate charge.

Features

- $V_{ds}=30V$
- $I_d=7.5A$ ($V_{gs}=10V$)
- $R_{ds(on)} < 22m\Omega$ ($V_{gs}=10V$)
- $R_{ds(on)} < 35m\Omega$ ($V_{gs}=4.5V$)

Maximum absolute ratings

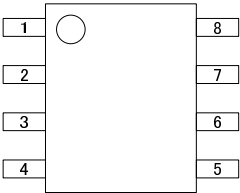
Parameter		Symbol	Limit	Unit	Note
Drain-source voltage		V_{ds}	30	V	
Gate-source voltage		V_{gs}	± 20	V	
Continuous drain current	$T_a=25^{\circ}C$	I_d	7.5	A	1
	$T_a=70^{\circ}C$		6.4		
Pulsed drain current		I_{dm}	30	A	2
Power dissipation	$T_a=25^{\circ}C$	P_d	2.00	W	
	$T_a=70^{\circ}C$		1.44		
Junction and storage temperature range		T_j, T_{stg}	-55 to 150	$^{\circ}C$	

Thermal characteristics

Parameter		Symbol	Typ.	Max.	Unit	Note
Maximum junction-to-ambient	$t \leq 10s$	$R\theta_{ja}$	50.0	62.5	$^{\circ}C/W$	1
Maximum junction-to-ambient	Steady-state		82.0	110.0	$^{\circ}C/W$	
Maximum junction-to-lead	Steady-state	$R\theta_{jl}$	41.0	50.0	$^{\circ}C/W$	3

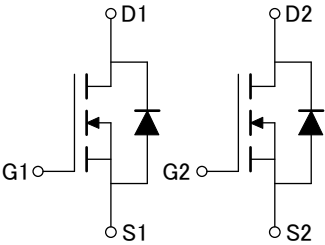
Pin configuration

SOP-8 (TOP VIEW)



Pin No.	Pin name
1	SOURCE2
2	GATE2
3	SOURCE1
4	GATE1
5	DRAIN1
6	DRAIN1
7	DRAIN2
8	DRAIN2

Circuit



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Electrical characteristics

Ta=25°C

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
STATIC PARAMETERS						
Drain-source breakdown voltage	BV _{dss}	I _d =250 μ A, V _{gs} =0V	30			V
Zero gate voltage drain current	I _{dss}	V _{ds} =30V V _{gs} =0V		0.004	1.000	μ A
		T _j =55°C			5.000	
Gate-body leakage current	I _{gss}	V _{ds} =0V, V _{gs} = $\pm$ 20V			100	nA
Gate threshold voltage	V _{gs(th)}	V _{ds} =V _{gs} , I _d =250 μ A	1.00	1.65	3.00	V
On state drain current	I _{d(on)}	V _{gs} =4.5V, V _{ds} =5V	20			A
Static drain-source on-resistance	R _{ds(on)}	V _{gs} =10V		18	22	m Ω
		I _d =7.5A		26	31	
		T _j =125°C				
		V _{gs} =4.5V, I _d =5A		28	35	m Ω
Forward transconductance	G _{fs}	V _{ds} =5V, I _d =7.5A	10	24		S
Diode forward voltage	V _{sd}	I _s =1A, V _{gs} =0V		0.77	1.00	V
Max. body-diode continuous current	I _s				4.3	A
DYNAMIC PARAMETERS						
Input capacitance	C _{iss}	V _{gs} =0V, V _{ds} =15V, f=1MHz		621	820	pF
Output capacitance	C _{oss}			118		pF
Reverse transfer capacitance	C _{rss}			85		pF
Gate resistance	R _g	V _{gs} =0V, V _{ds} =0V, f=1MHz		0.8	1.5	Ω
SWITCHING PARAMETERS						
Total gate charge (10V)	Q _g	V _{gs} =10V, V _{ds} =15V, I _d =7.5A		12.0	17.0	nC
Total gate charge (4.5V)	Q _g			6.0	8.0	nC
Gate-source charge	Q _{gs}			2.1		nC
Gate-drain charge	Q _{gd}			3.0		nC
Turn-on delay time	t _{d(on)}	V _{gs} =10V, V _{ds} =15V R _l =2 Ω , R _{gen} =3 Ω		4.5	6.5	ns
Turn-on rise time	t _r			3.1	5.0	ns
Turn-off delay time	t _{d(off)}			15.1	23.0	ns
Turn-off fall time	t _f			2.7	5.0	ns
Body diode reverse recovery time	t _{rr}	I _f =7.5A, dI/dt=100A/ μ s		15.5	20.0	ns
Body diode reverse recovery charge	Q _{rr}	I _f =7.5A, dI/dt=100A/ μ s		7.1	10.0	nC

NOTE :

1. The value of R θ _{ja} is measured with the device mounted on 1in² FR-4 board of 2oz. Copper, in still air environment with Ta=25°C. The value in any given applications depends on the user's specific board design. The current rating is based on the t $\leq$ 10s thermal resistance rating.
2. Repetitive rating, pulse width limited by junction temperature.
3. The R θ _{ja} is the sum of the thermal impedance from junction to lead R θ _{jl} and lead to ambient.
4. The static characteristics in Figures 1 to 6 are obtained using 80 μ s pulses, duty cycle 0.5%max.
5. These tests are performed with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with Ta=25°C. The SOA curve provides a single pulse rating.

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Typical electrical and thermal characteristics

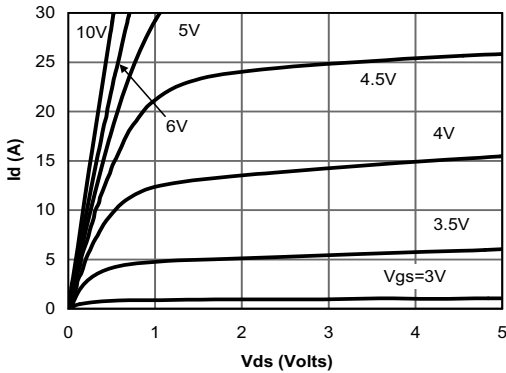


Fig 1: On-Region Characteristics

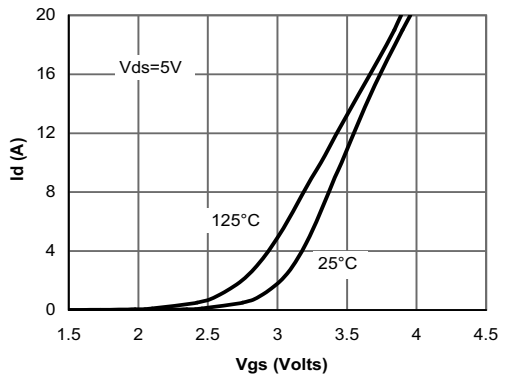


Figure 2: Transfer Characteristics

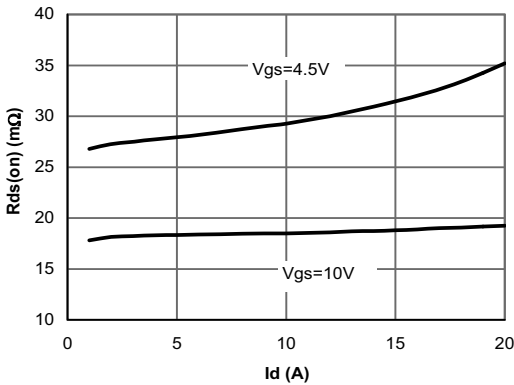


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

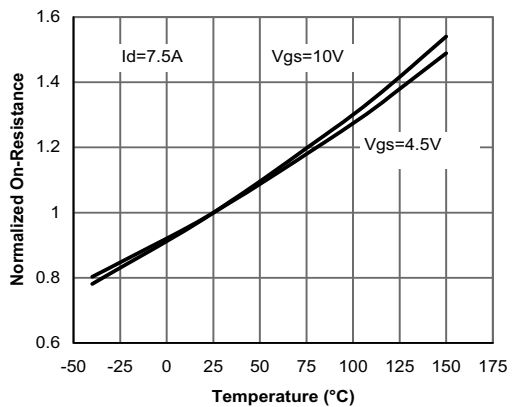


Figure 4: On-Resistance vs. Junction Temperature

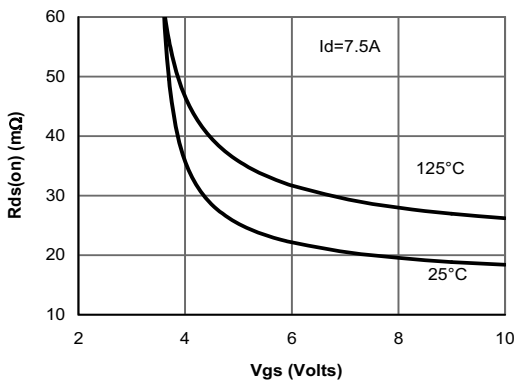


Figure 5: On-Resistance vs. Gate-Source Voltage

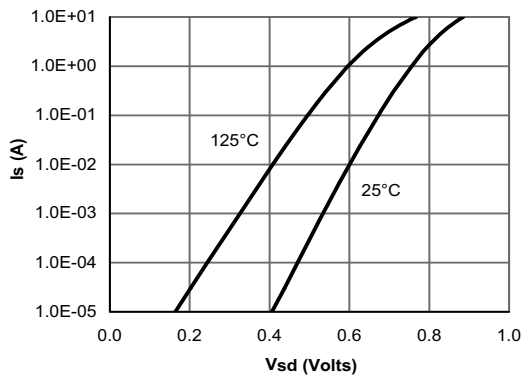


Figure 6: Body-Diode Characteristics

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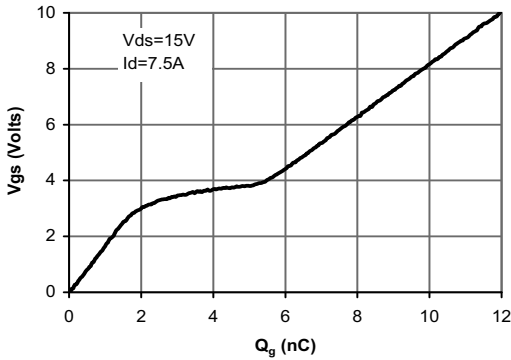


Figure 7: Gate-Charge Characteristics

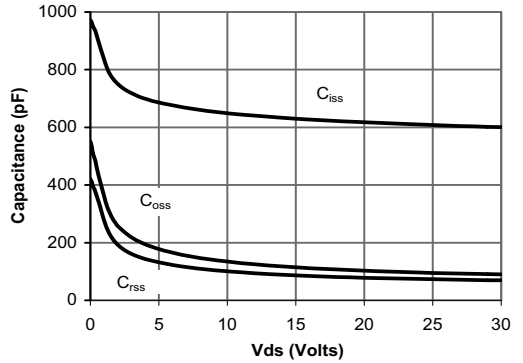


Figure 8: Capacitance Characteristics

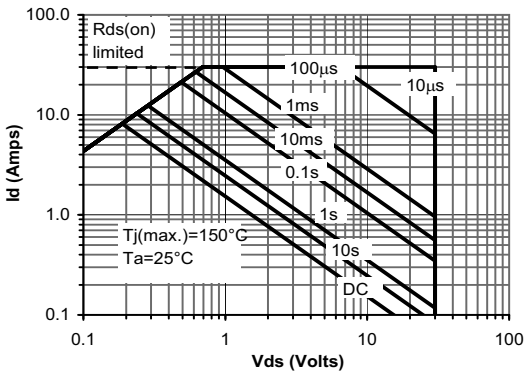


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

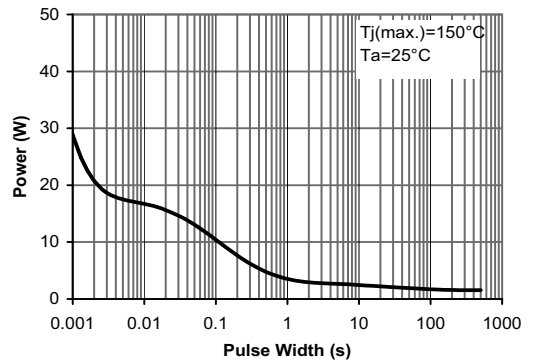


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

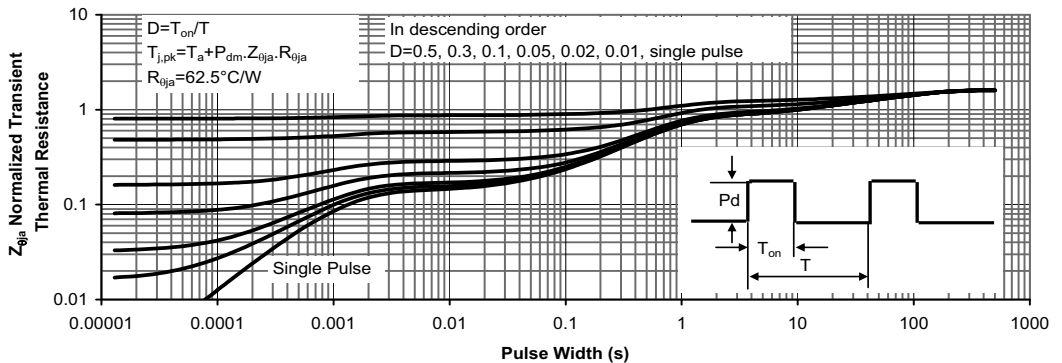


Figure 11: Normalized Maximum Transient Thermal Impedance