

**EN71PL032 Base MCP**

**Stacked Multi-Chip Product (MCP) Flash Memory and RAM  
32 Megabit (2M x 16-bit) CMOS 3.0 Volt-only Simultaneous  
Operation Page Mode Flash Memory and  
16 Megabit (1M x 16-bit) Pseudo Static RAM**

**Distinctive Characteristics****MCP Features**

- **Power supply voltage of 2.7 V to 3.3V**
- **High performance**
  - 70 ns
- **Package**
  - 7 x 9 x 1.2mm 56 ball FBGA
- **Operating Temperature**
  - 25°C to +85°C

**General Description**

The EN71PL series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- EN29PL032 (Simultaneous Read/Write) Flash memory die.
- Pseudo SRAM.

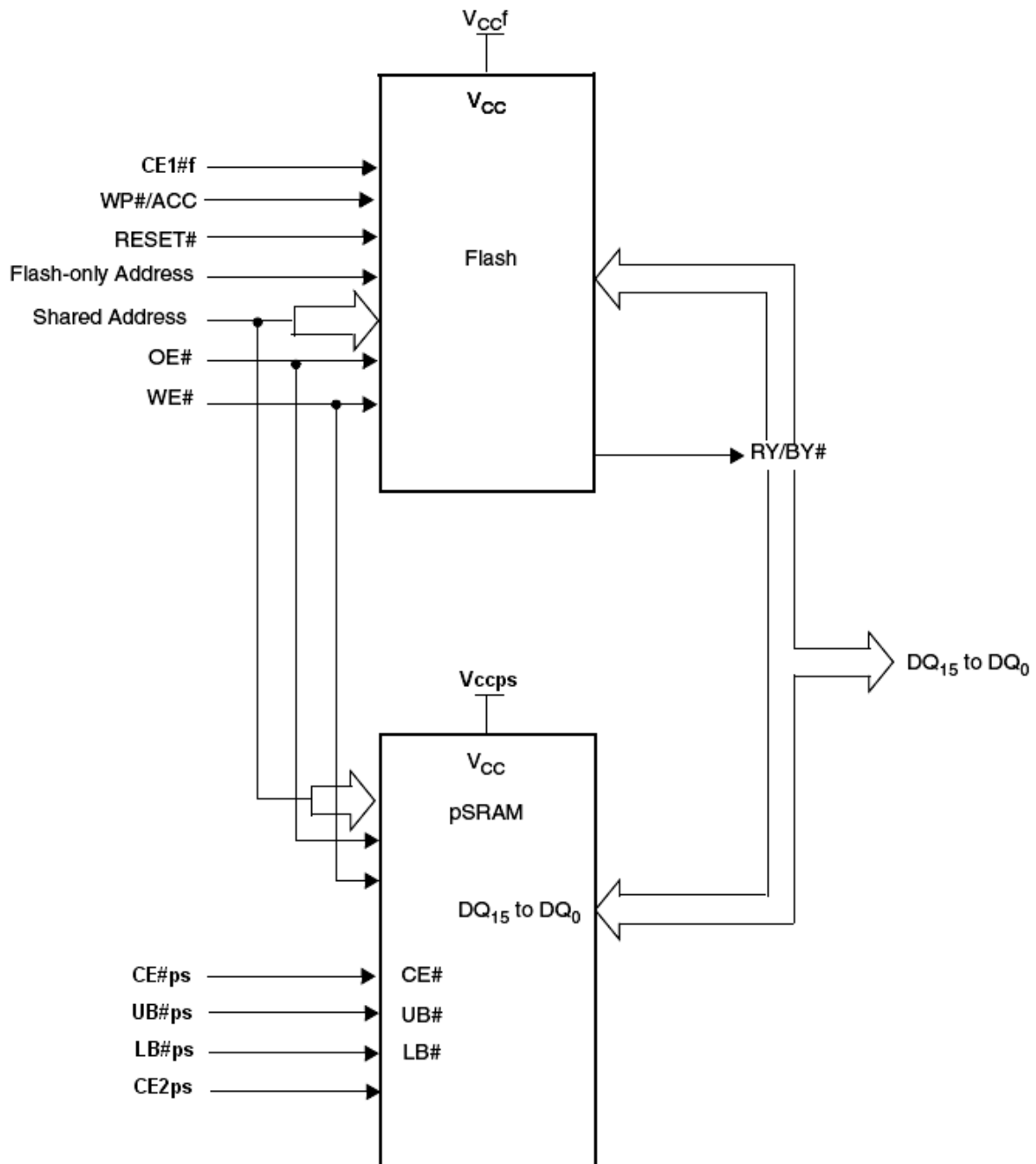
For detailed specifications, please refer to the individual datasheets listed in the following table.

| Device      | Document  |
|-------------|-----------|
| NOR Flash   | EN29PL032 |
| Pseudo SRAM | EN_EM1    |

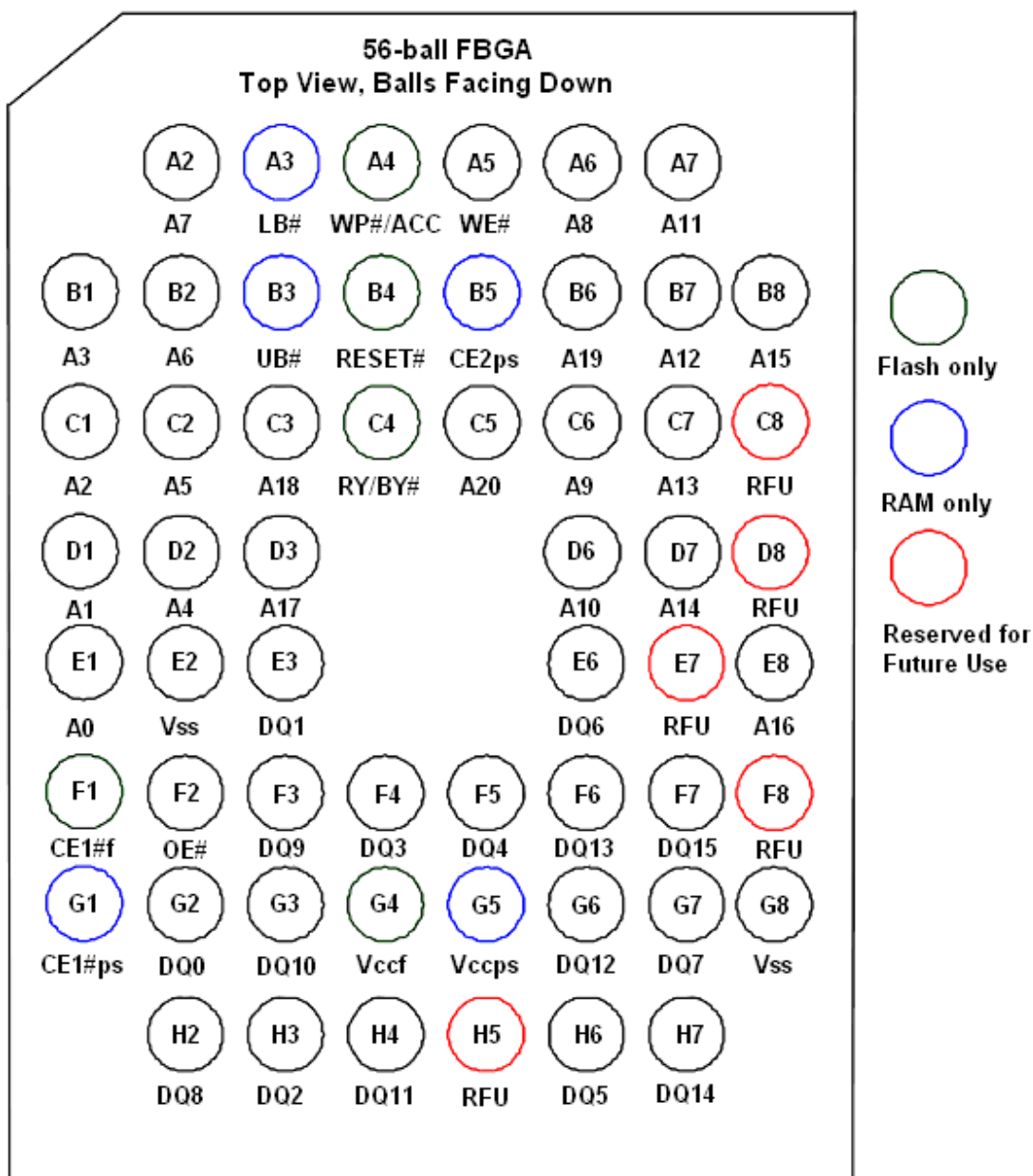
**Product Selector Guide****32Mb Flash Memory**

| Device-Model# | Flash Access time (ns) | pSRAM density | pSRAM Access time (ns) | Package |
|---------------|------------------------|---------------|------------------------|---------|
| EN71PL032A0   | 70                     | 16M pSRAM     | 70                     | 56 FBGA |

## MCP Block Diagram



## Connection Diagram



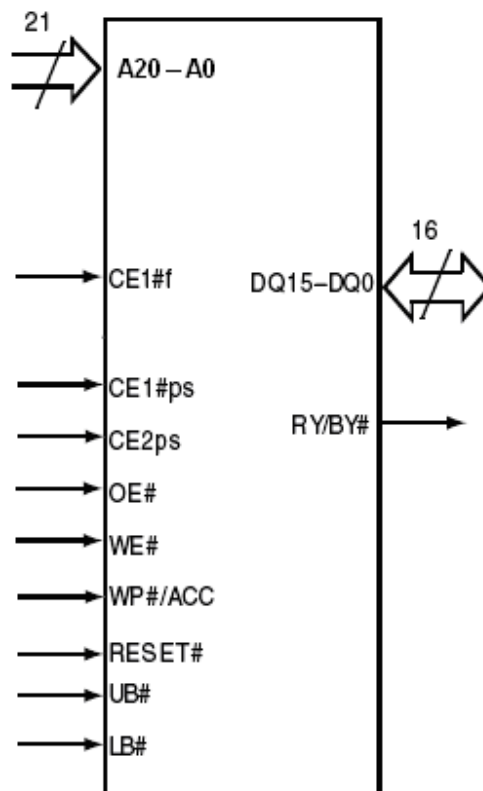
| MCP         | Flash-only Addresses | Shared Addresses |
|-------------|----------------------|------------------|
| EN71PL032A0 | A20                  | A19 – A0         |

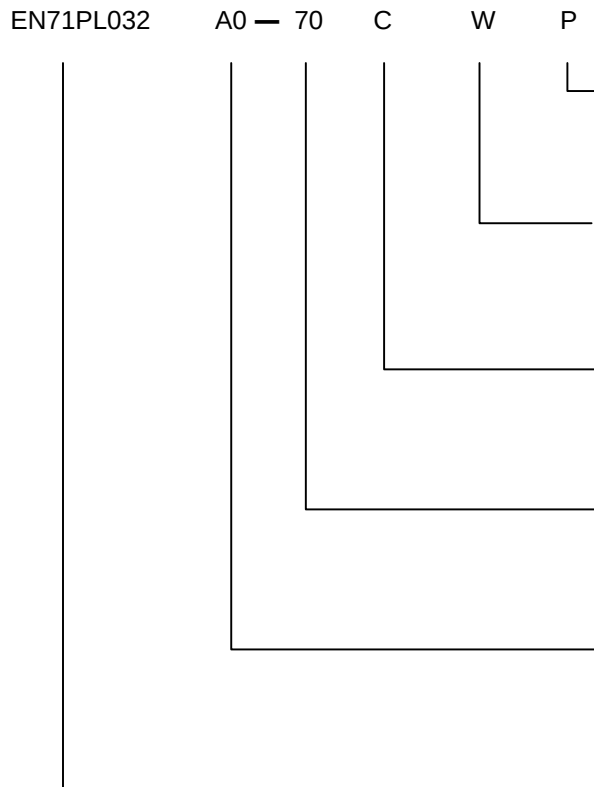


## Pin Description

| Signal            | Description                                     |
|-------------------|-------------------------------------------------|
| A20–A0            | 21 Address Inputs (Common)                      |
| DQ15–DQ0          | 16 Data Inputs/Outputs (Common)                 |
| CE1#f             | Chip Enable 1 (Flash)                           |
| CE1#ps            | Chip Enable 1 (pSRAM)                           |
| CE2ps             | Chip Enable 2 (pSRAM)                           |
| OE#               | Output Enable (Common)                          |
| WE#               | Write Enable (Common)                           |
| RY/BY#            | Ready/Busy Output (Flash)                       |
| UB#               | Upper Byte Control (pSRAM)                      |
| LB#               | Lower Byte Control (pSRAM)                      |
| RESET#            | Hardware Reset Pin, Active Low (Flash)          |
| WP#/ACC           | Hardware Write Protect/Acceleration Pin (Flash) |
| V <sub>ccf</sub>  | Flash 3.0 volt-only single power supply         |
| V <sub>ccps</sub> | pSRAM Power Supply                              |
| V <sub>ss</sub>   | Device Ground (Common)                          |
| NC                | Pin Not Connected Internally                    |

## Logic Symbol



**ORDERING INFORMATION****PACKAGING CONTENT**

(Blank) = Conventional  
P = Pb Free

**TEMPERATURE RANGE**

W = Wireless (-25°C to +85°C)

**PACKAGE**

C = 56-Ball Fine Pitch Ball Grid Array (FBGA)  
0.80mm pitch, 7mm x 9mm package

**SPEED**

70 = 70ns

**pSRAM density**

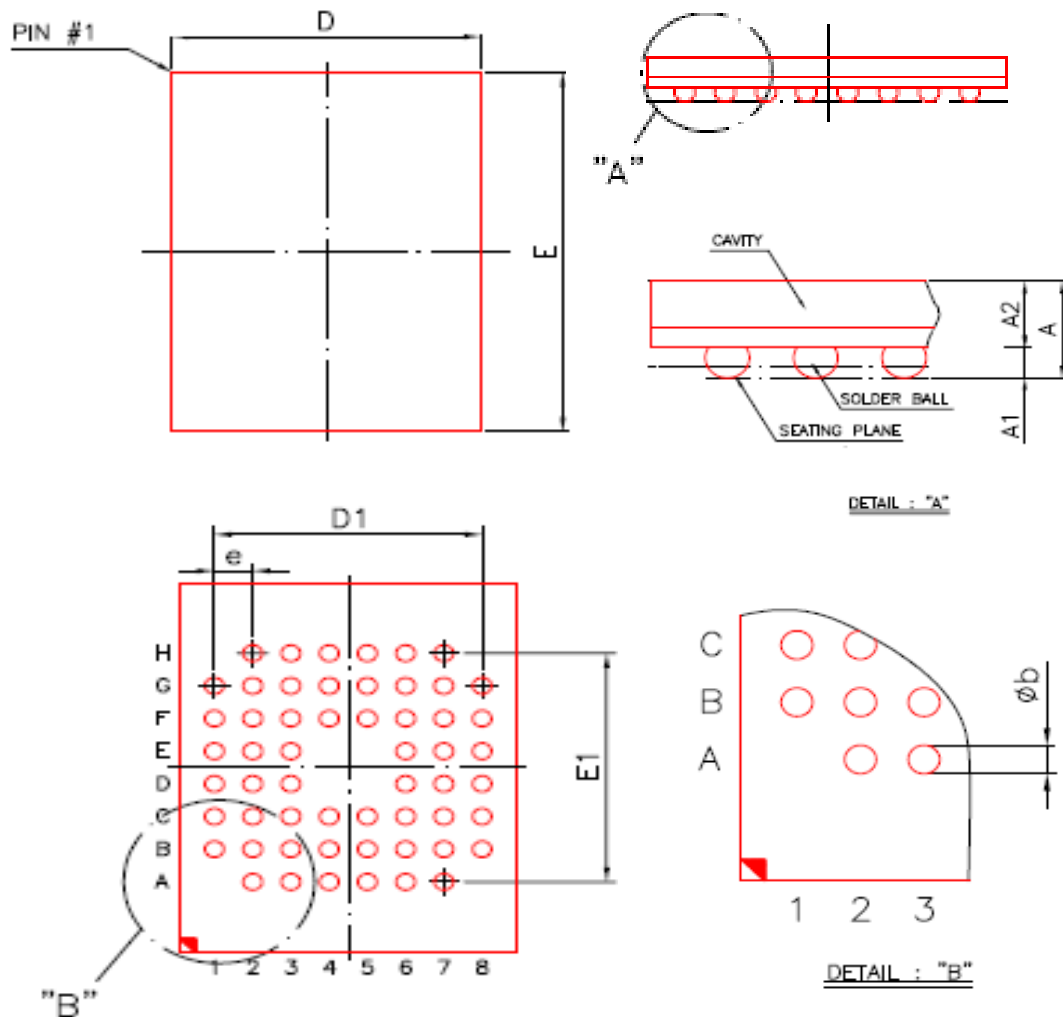
A0 = 16M pSRAM

**BASE PART NUMBER**

EN = Eon Silicon Solution Inc.  
71PL = Multi-chip Product (MCP)  
3.0V Simultaneous Read/Write,  
Page Mode Flash Memory and RAM  
032 = 32 Megabit (2M x 16)

## PACKAGE MECHANICAL

### 56-ball Fine-Pitch Ball Grid Array (FBGA) 7 x 9 mm Package



| SYMBOL | DIMENSION IN MM |      |      |
|--------|-----------------|------|------|
|        | MIN.            | NOR  | MAX  |
| A      | ---             | ---  | 1.20 |
| A1     | 0.25            | 0.30 | 0.35 |
| A2     | 0.61            | 0.66 | 0.71 |
| D      | 6.90            | 7.00 | 7.10 |
| E      | 8.90            | 9.00 | 9.10 |
| D1     | ---             | 5.60 | ---  |
| E1     | ---             | 5.60 | ---  |
| e      | ---             | 0.80 | ---  |
| b      | 0.35            | 0.40 | 0.45 |

**Note : 1. Coplanarity: 0.1 mm**

**Revisions List**

| Revision No | Description                                                                                                                                                               | Date       |
|-------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| A           | Initial Release                                                                                                                                                           | 2008/04/08 |
| B           | 1. Update MCP Block Diagram in page 2 and Pin Description in page 4.<br>2. Remove the individual datasheet descriptions of EN29PL064/032 and EN_EM566168GD from Vision A. | 2008/09/10 |