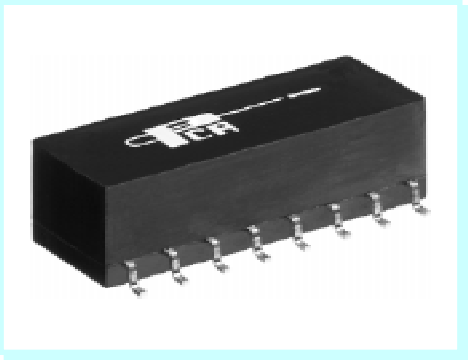
10/100 LAN Interface Module for NIC/HUB Card Applications, Mini Package

EPF8018G



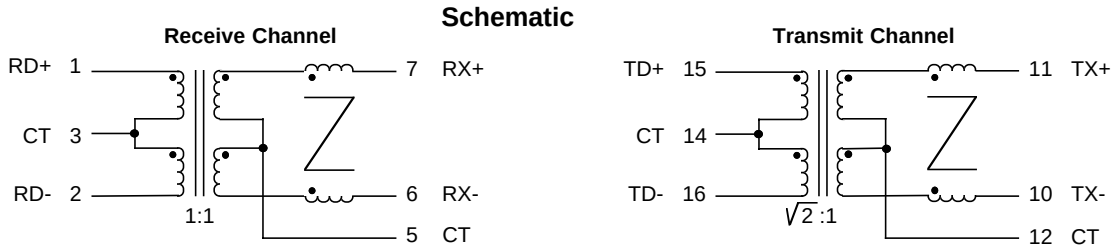
- Guaranteed to operate with 8 mA DC bias at 70°C on cable side •
- Complies with or exceeds IEEE 802.3, 10 BT/100 BX Standards •

Electrical Parameters @ 25° C

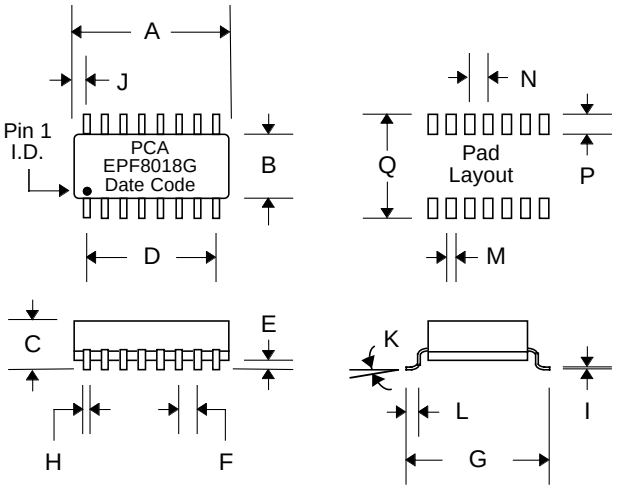
OCL @ 70°C	**Insertion Loss** (dB Max.)						**Return Loss** (dB Min.)						**Common Mode Rejection** (dB Min.)						**Crosstalk** (dB Min.) [Between Channels]	
100 KHz, 0.1 Vrms 8 mA DC Bias	1-80 MHz		80-100 MHz		100-150 MHz		1-30 MHz		30-60 MHz		60-100 MHz		30-100 MHz		100-200 MHz		200-500 MHz		5-10 MHz	10-100 MHz
Cable Side	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv		
350µH	-1	-1	-1	-1	-3.5	-3	-18	-18	-12	-12	-10	-10	-45	-45	-30	-30	-15	-15	-40	-40

• **Isolation** : 1500 Vrms • Cable **Impedance** : 100 Ω • **Rise Time** : 3.0 nS Max. •

Schematic



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	.780	.800		19.81	20.321	
B	.290	.310		12.95	3.46	
C	.223	.243		5.66	6.17	
D	.700	Typ.		17.78	Typ.	
E	.003	.020		0.076	.508	
F	.100	Typ.		2.54	Typ.	
G	.350	.370		8.89	9.40	
H	.016	.022		.406	.559	
I	.008	.012		.203	.305	
J	.045	Typ.		1.14	Typ.	
K	0°	8°		0°	8°	
L	.025	.045		.635	1.14	
M			.030			.762
N			.100			2.54
P			.092			2.34
Q			.410			17.78

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CSF8018Ga Rev. 1 11/26/96

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The circuit below is a guideline for interconnecting PCA's EPF8018G with QSI6611 and QSI6612 chip set for 10/100 Mb/s applications. Further details can be obtained from the chip manufacturer application notes.

Typical insertion loss of the isolation transformer is 0.5dB. This parameter covers the entire spectrum of the encoded signals in 10/100 protocols. Under terminated conditions, to transmit a 2V pk-pk signal across the cable, you must adjust the chips supporting resistor to get at least 2.12V pk-pk across the transmit pins.

It is recommended that system designers do not use the receiver side center tap to ground, via a capacitor. This may worsen EMI, specifically if the secondary "common mode termination" is pulled to chassis ground as shown.

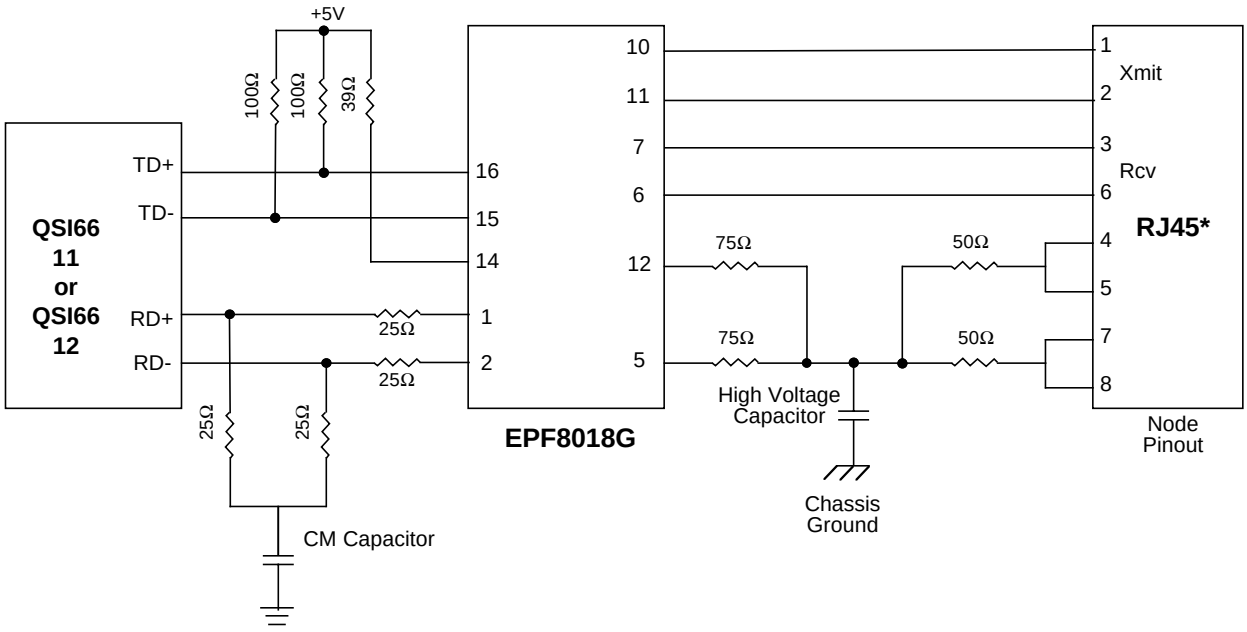
The phantom resistors shown around the connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

The "common mode termination" load of 75 Ω shown from the center taps of the secondary may be taken to chassis ground via a cap of suitable value. This depends upon user's design, EMI margin etc.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.05 inches away from the chip side pins of EPF8018G. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50 Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP



Notes : * NIC Side is shown. Hub side connection will have crossover swapping pins 1-2 & 3-6.

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