F15353

2-wire Real-time Clock

Release Date: Sep, 2008
Version: 0.12P

F15353 Datasheet Revision History

Version	Date	Page	Revision History
0.10P	Jan, 2008		Preliminary version
0.11P	Jul, 2008	4	Modify some contents in General Description Current consumption spec changed to 0.55uA at 3.0V Add TSSOP-8 package for option
0.12P	Sep, 2008	4 5 9 12 19 33 37	supply voltage as low as ~~1.2~~ 1.1 V (min.) Add TSSOP-8 pin configuration Operating voltage ~~3.0~~ 1.3V Input low voltage ~~0.6~~ 0.4V Revise 6.4 description Add “Caution: The figure range which can be corrected is that the calculated value is from 0 to 62.” Remove redundant register 7.9-7.13 Figure 18: F15353~~S~~ Application Circuit

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1 General Description

The F15353 which is a low current consumption 2- wire CMOS real-time clock operates under 1.3V to 3.6V. The current consumption is only 0.55uA and operation voltage is 1.1V as time keeping. In a system that operates on a backup battery, the free register incorporated in the real-time clock can be used for the user backup memory function. The user register can hold data on a supply voltage as low as 1.1 V (min.), so the data stored in the register before the main power supply was removed and can be recalled any time after the power is reconnected.

A clock adjustment function that enables wide range correction of deviation in the frequency of the crystal oscillator at a minimum resolution of 1 PPM is integrated in the F15353. The clock adjustment value can be set in accordance with changes in the temperature. It is possible to make the realization of clock function that retains a high degree of accuracy regardless of temperature variation by combining with a temperature sensor.

2 Feature

- Low Current Consumption: 0.55uA, Typical (VDD = 3.0V, Ta = 25°C)
- Operate Voltage Range: 1.3 to 3.6V
- Minimum Time Keeping Operation Voltage: 1.1V
- Built-in Clock Adjustment Function
- Built-in Free User Register
- Built-in Alarm Interrupt
- Built-in Flag Generator at Power down or Power on
- Built-in Constant Voltage Circuit
- Built-in 32KHz Crystal Oscillator Circuit (Cd Built-in, Cq External)
- Auto Calendar up to the Year 2099, Automatic Leap Year Calculation Function
- I2C Interface
- Powered by 3.3VCC and packaged in SOP-8 and TSSOP-8

3 Pin Configuration

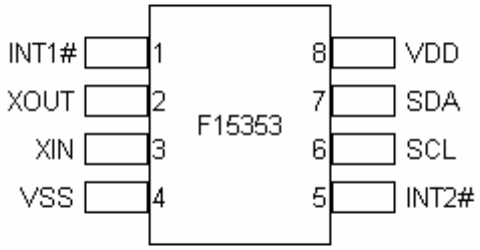


Figure1: F15353 SOP-8 pin configuration

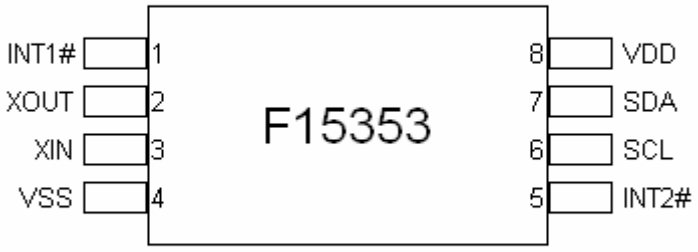


Figure2: F15353 TSSOP-8 pin configuration

4 Pin Description

P - Power pins

IN_{st} - TTL level input pin with schmitt trigger

I/OD_{1ost} - TTL level bi-directional pin with schmitt trigger, Open-drain output with 10 mA sink capability at VDD=3.0V

OD_5 - Output pin with 5mA sink capability at VDD=3.0V

AIN - Input pin (Analog).

AOUT - Output pin (Analog).

4.1. Power Pin

Pin No.	Pin Name	Type	Description
4	VSS	P	Ground
8	VDD	P	Power supply pin

4.2. Crystal Oscillator Pin

Pin No.	Pin Name	Type	PWR	Description
2	XOUT	AOUT	VDD	Crystal oscillator connect pin, 32.768KHz
3	XIN	AIN	VDD	Crystal oscillator connect pin, 32.768KHz

4.3. Interrupt Pin

Pin No.	Pin Name	Type	PWR	Description
1	INT1#	OD_5	VDD	Interrupt 1 signal output pin. Depending on the mode set by INT1 register_1 and the status register, it outputs low or a clock when the time is reached. It is disabled by rewriting the status register.
5	INT2#	OD_5	VDD	Interrupt 2 signal output pin. Depending on the mode set by INT1 register_2 and the status register, it outputs low or clock when time is reached. It is disabled by rewriting the status register.

4.4. I2C Interface Pin

Pin No.	Pin Name	Type	PWR	Description
6	SCL	IN_{st}	VDD	Serial clock input pin. Since signal processing is done on the SCL signal rising/falling edge, give great care to the rising/falling time and comply strictly with the specifications.
7	SDA	I/OD_{1ost}	VDD	Serial data I/O pin. Normally, it is pulled up to the V_{DD} voltage by a resistor and connected with another open-drain output or open-collector output device via a wired-OR connection.

5 Electrical Characteristic

5.1 Absolute Maximum Ratings

PARAMETER	RATING	UNIT
Power Supply Voltage	-0.3 to 3.6	V
Input Voltage	-0.3 to VDD+0.3	V
Operating Temperature	0 to +70	° C
Storage Temperature	-55 to 150	° C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device

5.2 DC Characteristics

(Ta = 0° C to 70° C, VDD = 3.0V ± 10%, VSS = 0V)

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	CONDITIONS
Operating Voltage	VDD	1.3	3.3	3.6	V	
Current Consumption 1	IDD1		0.55	0.93	uA	Out of communication
Current Consumption 2	IDD2		6	14	uA	During communication (SCL=100KHz)
I/OD_{10st} - TTL level and schmitt trigger bi-directional pin with 10 mA source-sink capability						
Input Low Voltage	VIL			0.4	V	
Input High Voltage	VIH	2.4			V	
Hysteresis			0.3		V	
Output Low Current	IOL	5.0	10		mA	VOL = 0.4V
Input High Leakage	ILIH	-0.5		+0.5	μA	
Input Low Leakage	ILIL	-0.5		+0.5	μA	
OD_5 – Output pin with 5mA sink capability						
Input Low Voltage	VIL			0.4	V	
Input High Voltage	VIH	2.4			V	
Hysteresis			0.3		V	
Output Low Current	IOH	3.0	5.0		mA	VOL = 0.4 V
Input High Leakage	ILIH	-0.5		+0.5	μA	
Input Low Leakage	ILIL	-0.5		+0.5	μA	
IN_{ts} – TTL level input pin and schmitt trigger						
Input Low Voltage	VIL			0.4	V	
Input High Voltage	VIH	2.4			V	
Hysteresis			0.3		V	
Input High Leakage	ILIH			+0.5	μA	
Input Low Leakage	ILIL	-0.5			μA	

6 Functional Description

6.1 Power Supply Voltage Detector

Bit 7, POC flag, of status register_1 is set to 1 (“80h”) by the power-on detector and an 1Hz clock is output from the INT1# pin. The oscillation frequency is adjustable. In the common condition, the F15353 must be initialized at power-on. Initialization is performed by setting “1” to bit 0, RESET flag, of the status register_1. After the initialization, the POC flag is set to “0”. In the common operation of the power-on detector, the supply voltage is held at 0Vand then increasing it.

The state of every register after initialization is as following:

Table 1: Initialization States of Register

Real-time data register	00(year),01(month), 01(day), 0(day of week), 00(hour), 00(minute), 00(second)
Status register_1	“0 0 0 0 b3 b2 b1 0”b (The b3, b2, and b1 data of status register_1 after initialization are set in b3, b2, b1)
Status register_2	“00”h
INT1# register_1	“00”h
INT1# register_2	“00”h
Clock adjustment register	“00”h
Free register	“00”h

6.2 Power Supply Voltage Detector

There is an internal power supply voltage detector, which monitors the power supply voltage drops by reading the BLD flag, in the F15353. If the power supply voltage drops under the detect voltage (typical 1.2v), the BLD latch circuit latches “H” level. Bit 6, BLD flag, of the internal status register_1 is set to “1”, and the sampling is stopped. If the BLD flag is detected “1”, the detection is stopped until the initialization is performed or the flag is read by the status register_1 access command, and “1” is held in the BLD flag. The resume condition of sampling operation is the subsequent communication action initialized or the BLD flag read only. If the BLD flag is “1” after the power supply voltage is recovered, it must be initialized additionally.

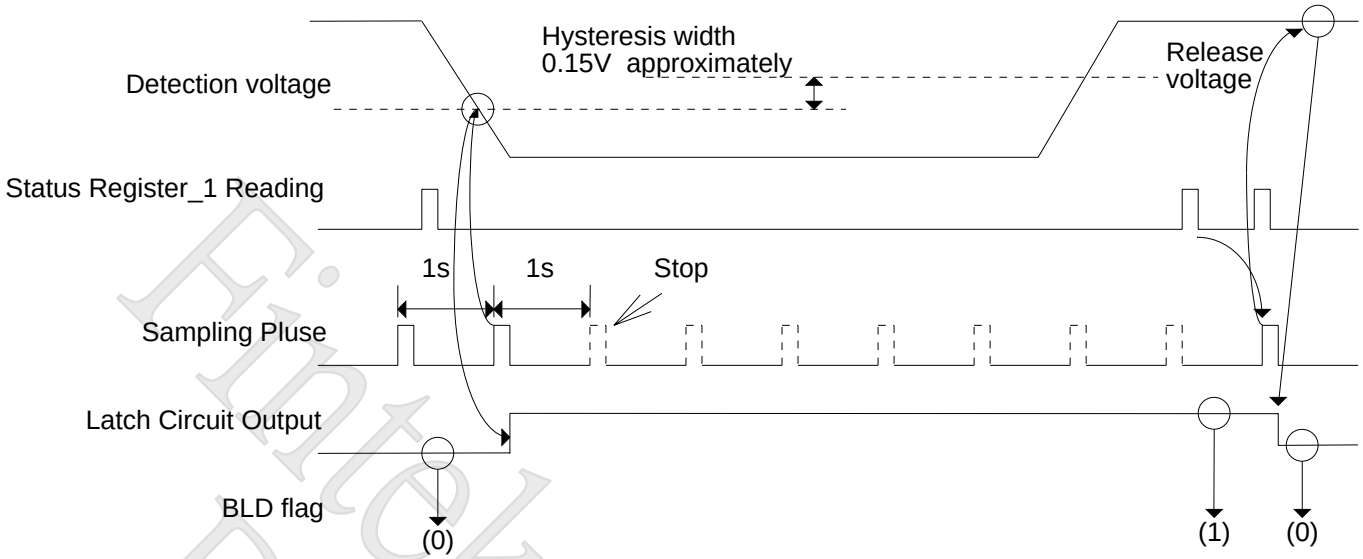
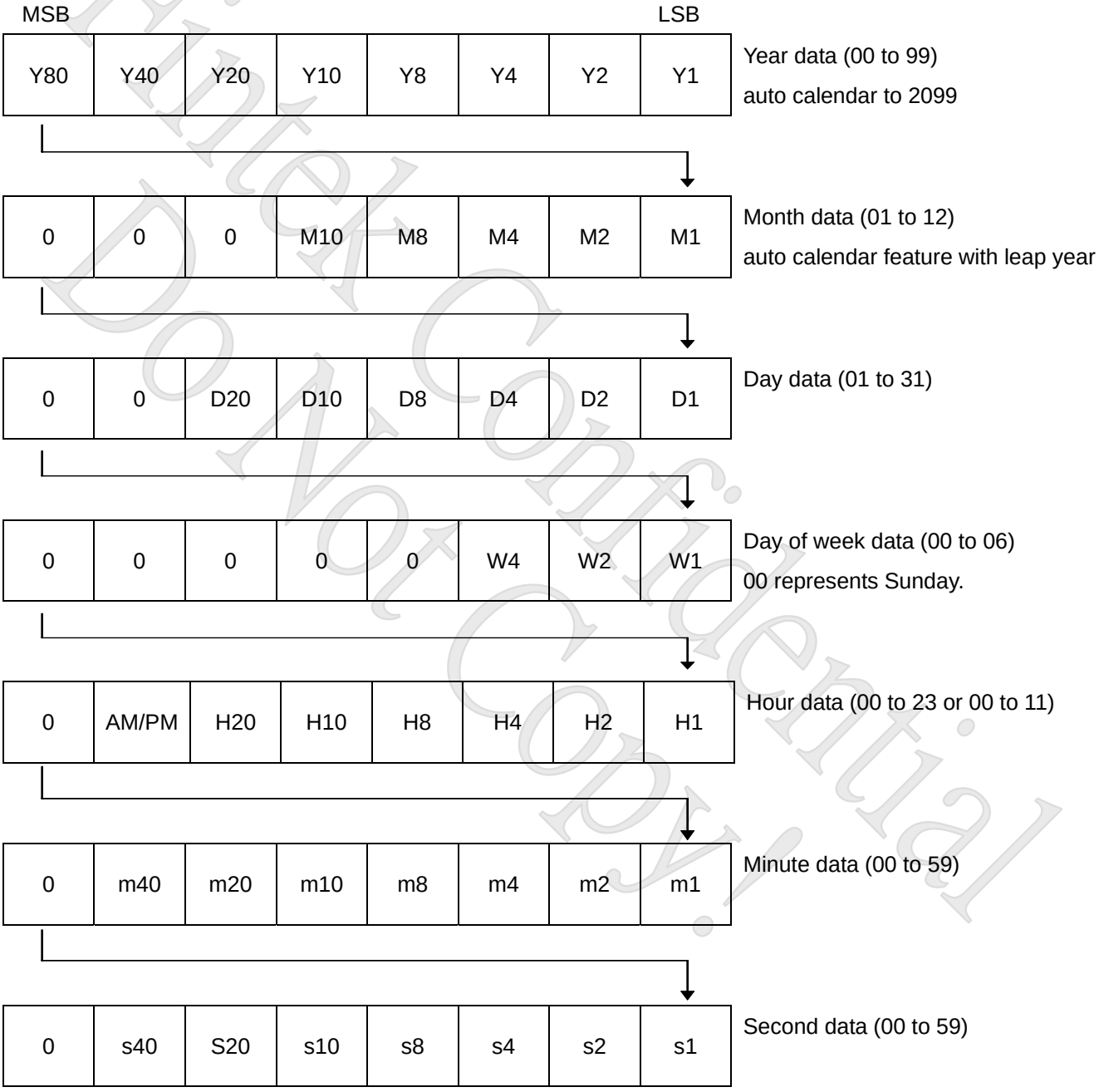


Figure 3: Timing of power supply voltage detector

6.3 Real-time Data

The real-time data is stored in a 56-bit register in BCD code of year, month, day, day of week, hour, minute, and second data. The data from the LSB which is the first digit of the year is transmitted or received by read/write command performed by the real-time access.



6.4 Invalid Date Process

When the real time data is written, the invalid data will be corrected immediately as Table 2.

Table 2: Process of Invalid Date

Register	Normal Data	Error Data	Result
Year data	00 to 99	XA to XF, AX to FX	00
Month data	01 to 12	00, 13 to 19, XA to XF	01
Day data	01 to 31	00, 32 to 39, XA to XF	01
Day of week data	0 to 6	7	0
Hour data*1 (24-hour) (12-hour)	 0 to 23 0 to 11	 24 to 29, 3X, XA to XF 12 to 19, 2X, 3X, XA to XF	 00 00
Minute data	00 to 59	60 to 79, XA to XF	00
Second data	00 to 59	60 to 79, XA to XF	00

*1 For 12-hour expression, setting AM/PM flag, and the flag is ignored in 24-hour expression. “0” for 0 to 11 o’clock and “1” for 12 to 23 o’clock are read in a read operation.

6.5 Interrupt Function

The INT1# pin output mode is selected by the INT1AE, INT1ME, and INT1FE flags of the status register02. The INT2# pin output mode is selected by the INT2AE, INT2ME, and INT2FE flags of the status register02, similarly.

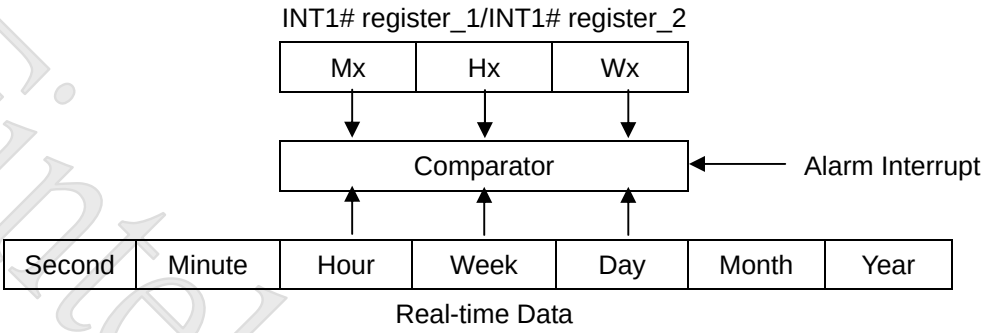
6.5.1 Alarm Interrupt Output

If the INT1# or INT2# pin output mode is set to the alarm setting, the INT1# or INT2# pin will pull low as the set data reached. The set data, the day of week, the hour, and the minute, are stored in INT1 register_1 (command 100b) or INT1 register_2 (command 101b). To Rewrite INT1AE or INT2AE of status register_2 to “0” will release the output from low to high.

Ex:

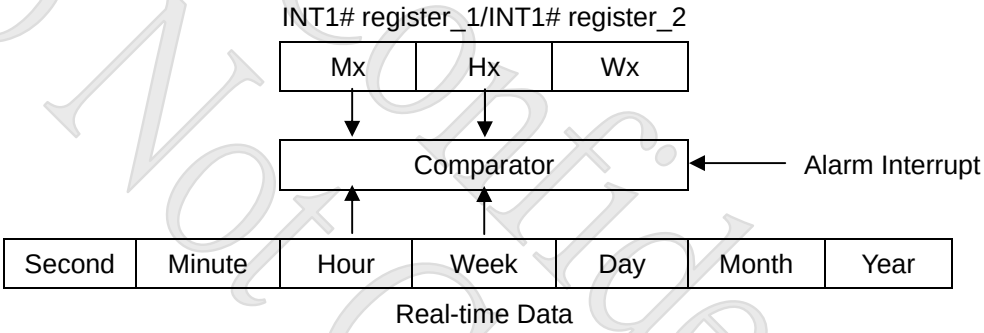
32kE=0, INT1ME=INT1FE=0 (INT1# pin output mode), INT2ME=INT2FE=0 (INT2# pin output mode)

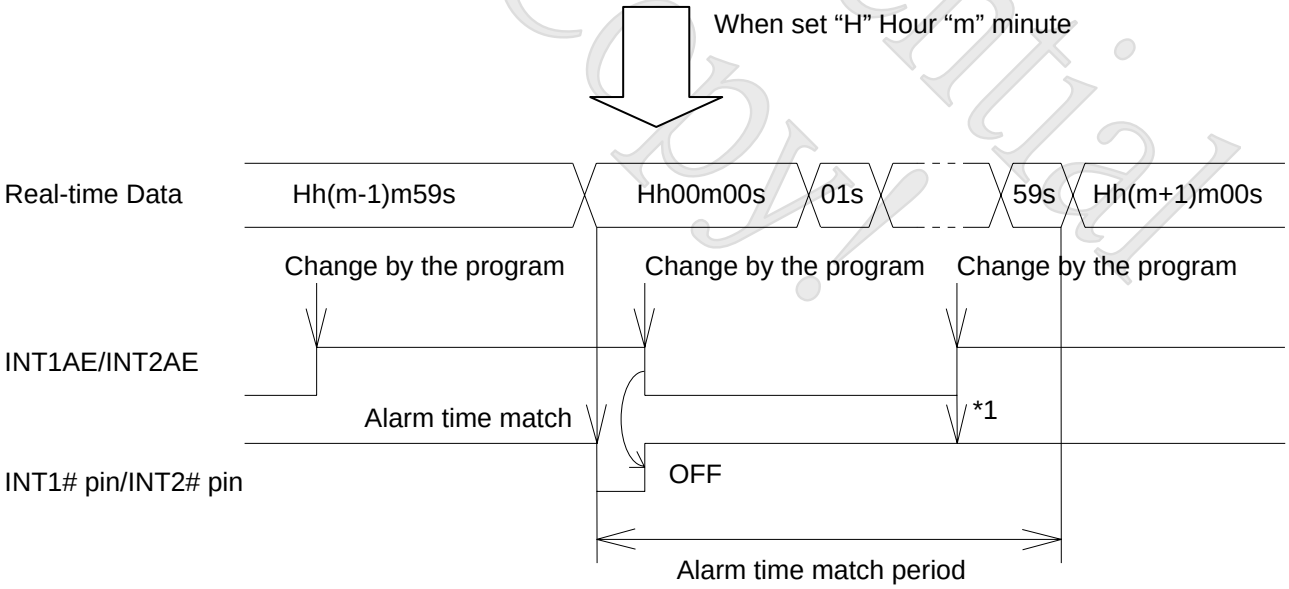
Alarm enable flag: In case of AxWE=AxHE=AxmE="1"



32kE=0, INT1ME=INT1FE=0 (INT1# pin output mode), INT2ME=INT2FE=0 (INT2# pin output mode)

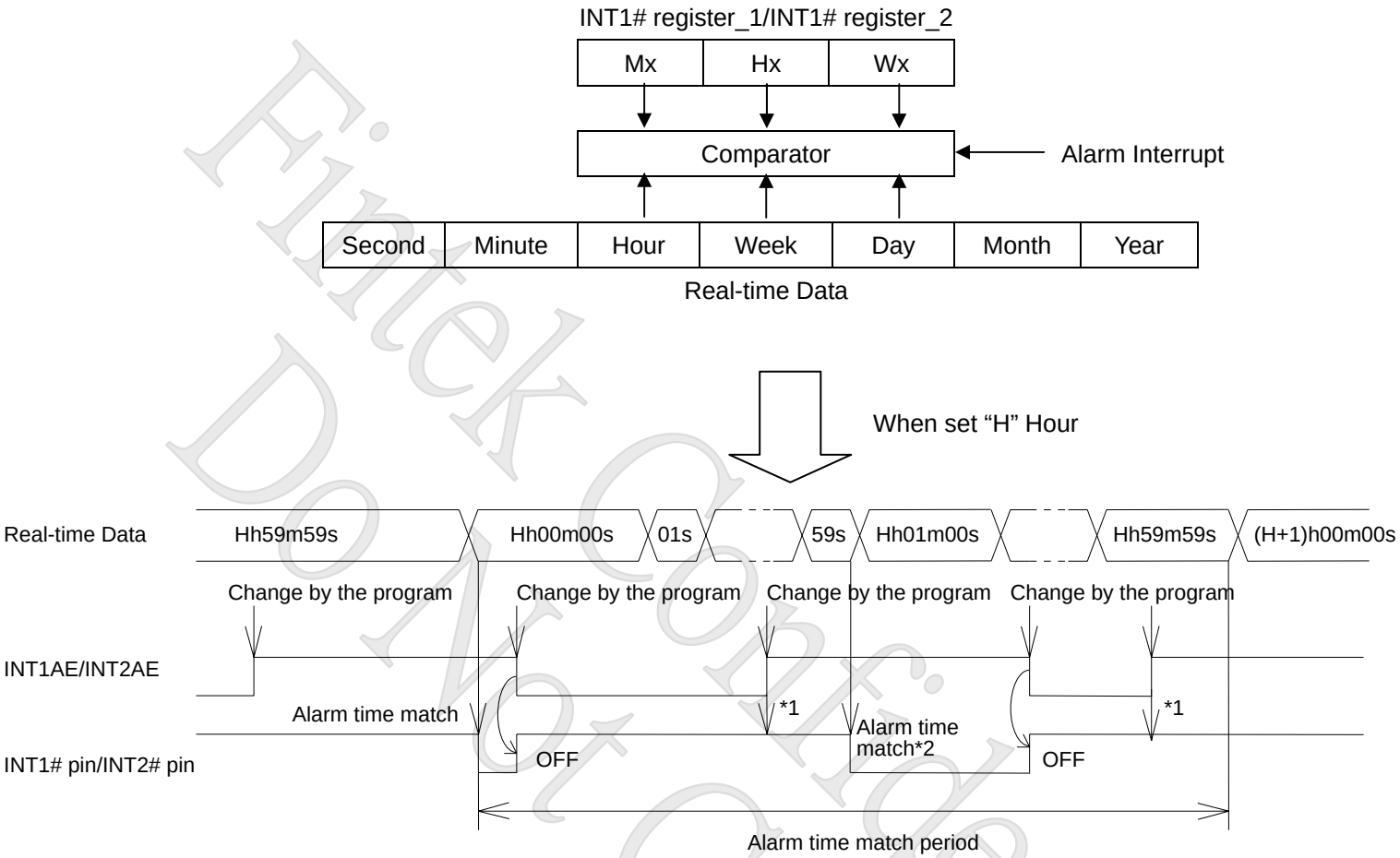
Alarm enable flag: In case of AxWE="0" AxHE=AxmE="1"





32kE=0, INT1ME=INT1FE=0 (INT1# pin output mode), INT2ME=INT2FE=0 (INT2# pin output mode)

Alarm enable flag: In case of AxWE=AxmE="0", AxHE="1"



*1 Once it clears, even if it enables again within a coincidence period, "L" will not be output from an INT1# or INT2# pin.

*2 "L" is output again from INT# pin at the time of change of the following part when an alarm output is turned on by change by the program within a coincidence period.

6.5.2 Selected Frequency Steady Interrupt Output

Set the status register_2 and the INT1# or INT2# pin output mode is set to the selected frequency steady interrupt output. The set clock output follows the frequency data set in INT1# register_1 or register_2.

Ex:

32kE=0, INT1ME=0, INT1AE=Don't care (0 or 1) INT2ME=0 INT2AE=Don't care (0 or 1)

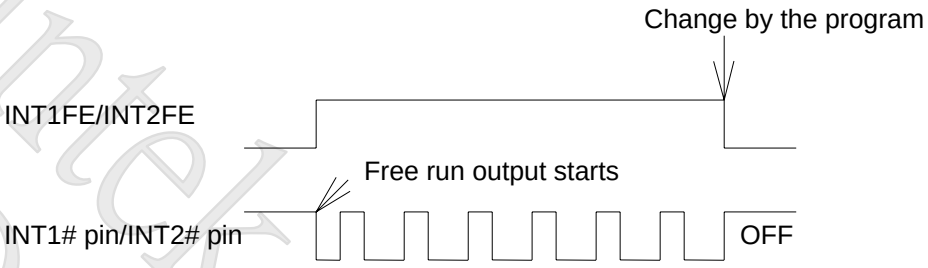


Figure 4: Timing of Selected Frequency Steady Interrupt Output

6.5.3 Per-minute edge interrupt output

If INT1# or INT2# pin output mode is set as the per-minute edge interrupt, INT1# or INT2# will pull low as the first minute carry is performed. Since the output is held, to rewrite 32kE, INT1AE, INT1ME, and INT1FE of the register_2 to "0" sets the output to high (OFF state) in INT1# pin output mode. IN INT2# mode, to rewrite INT2AE, INT2ME, and INT2FE of the register_2 to "0" or INT2AE of status register_2 to "0" will release the output from low to high.

Ex:

32kE=0, INT1ME=0, INT1AE=Don't care (0 or 1) INT2ME=0 INT2AE=Don't care (0 or 1)

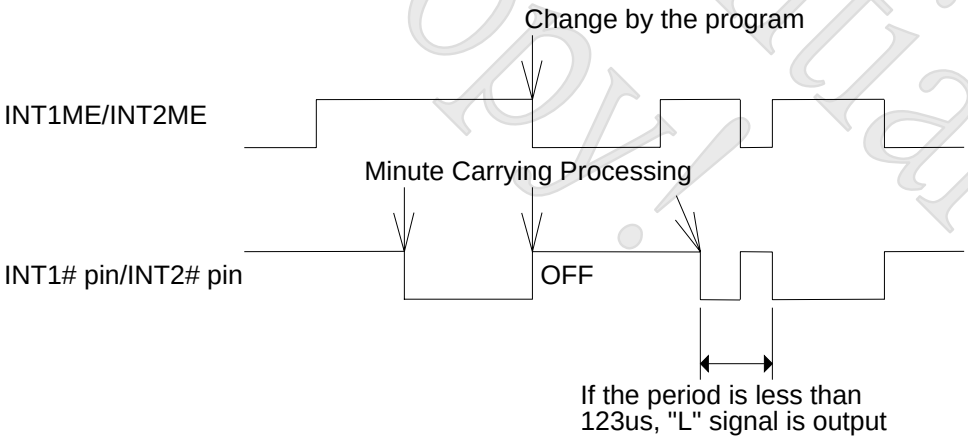


Figure 5: Timing of Per-minute Edge Interrupt Output

6.5.4 Per-minute steady interrupt output1

If INT1# or INT2# pin output mode is set as the per-minute steady interrupt, INT1# or INT2# will pull low as the first minute carry is performed. The data is set in register_2. A whole cycle of clock is 1 minute (50% duty) is output from INT1# or INT2# pin.

Ex:

32kE=0, INT1AE=0 (INT1# pin output mode) INT2AE=0 (INT2# pin output mode)

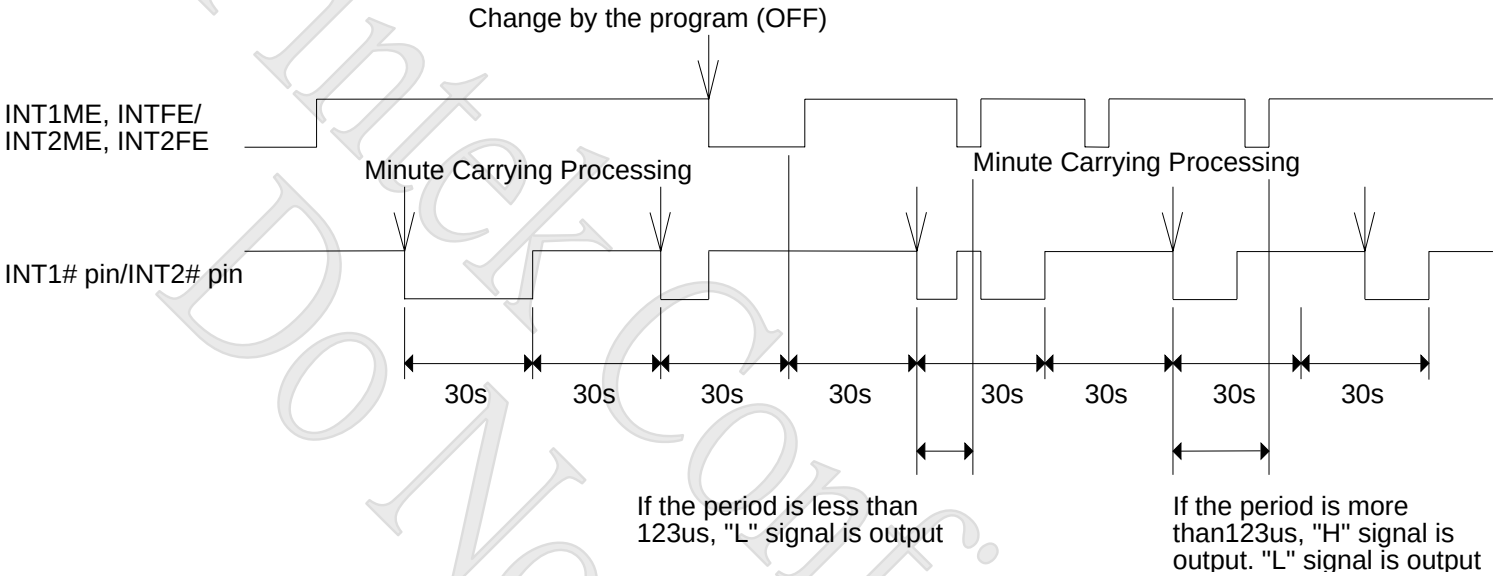
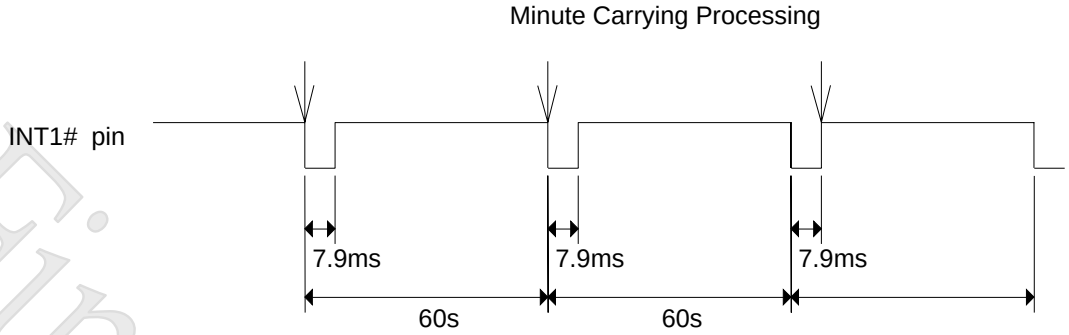


Figure 6: Timing of Pre-minute Steady Interrupt Output1

6.5.5 Per-minute steady interrupt output2 (INT1# pin output mode only)

If INT1# or INT2# pin output mode is set as the per-minute steady interrupt, INT1# will pull low as the first minute carry is performed. The output is the period of 7.9ms in synchronization with the minute carry processing inside the IC. However, when real-time data is read, the minute carry processing is delayed by a maximum of 0.5 s and accordingly low output from the INT1# pin is also delayed by 0.5s maximum. When the second data is rewritten by a real-time data write command, counting starts from the rewritten second data and as a result, the output interval during that period may become either longer or shorter.

6.5.5.1 During Normal Operation



6.5.5.2 During Real-time Data Read

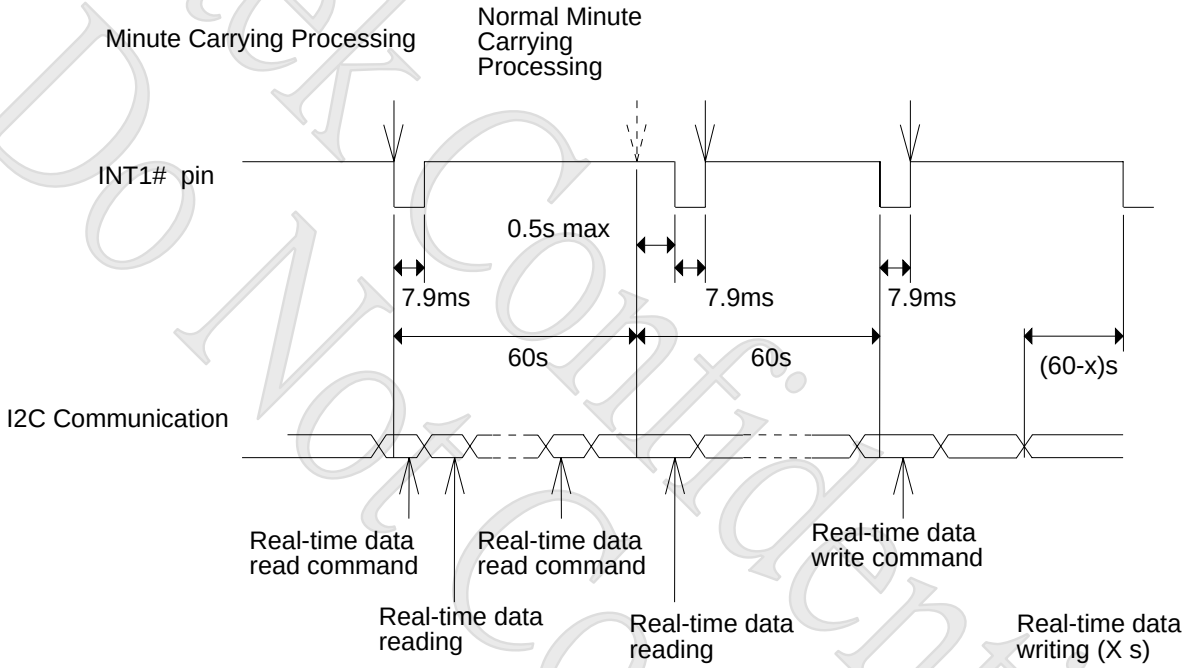


Figure 7: Time of Pre-minute Steady Interrupt Output2

Caution:

1. If Per-minute edge interrupt output mode or Per-minute steady interrupt mode is chosen, there is no difference between INT1 register_1 register_2.
2. When the output mode is changed, take care to the state of INT1 regisert_1 or register_2 and the output

6.5.6 During Power-on Detector Operation

When power is applied to this IC, power-on detection circuit operates, status register_1 is set to “80h” (bit 7 (POC flag) of status register_1 is set to 1) via the power-on detection circuit, and a 1 Hz clock is output from the INT1# pin.

Ex:

INT2AE=INT2ME=INT2FE=32kE=INT1AE=INT1ME=0

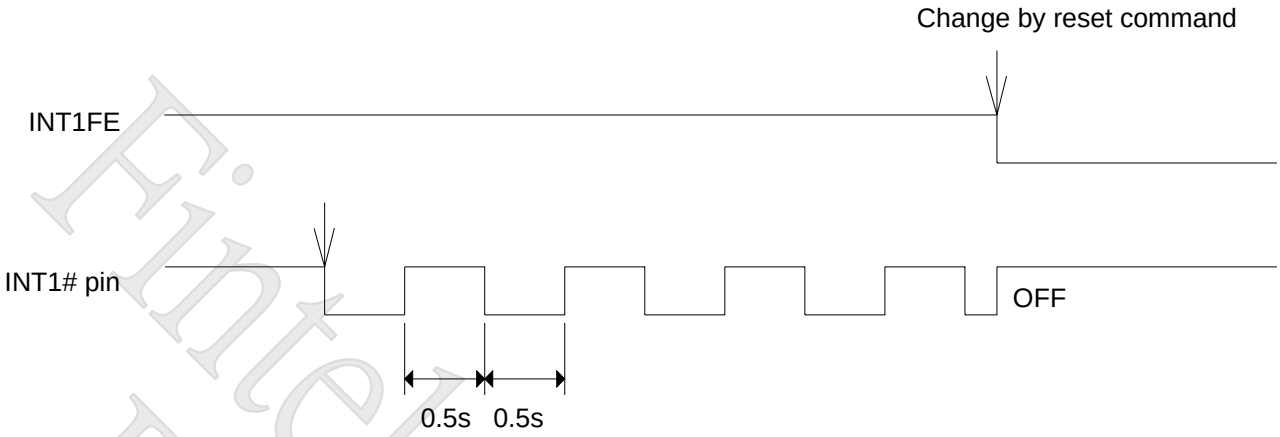


Figure 8: INT1# pin output Timing During Power-on Detector Operation

6.6 Alarm Interrupt Function

Data set in INT1 register_1 and register_2 is considered as alarm time data. There is the same configuration as the hour and minute registers of the real-time data register. These registers represent hours and minutes with BCD codes. Set data must fit the date rule which is in accordance with the 12-hour or 24-hour expression that is set in status register_1.

INT1 register_1

MSB							LSB
A1WE	0	0	0	0	W4	W2	W1
A1HE	AM/PM	H20	H10	H8	H4	H2	H1
A1mE	m40	m20	m10	m8	m4	m2	m1

INT1 register_2

MSB							LSB
A2WE	0	0	0	0	W4	W2	W1
A2HE	AM/PM	H20	H10	H8	H4	H2	H1
A2mE	m40	m20	m10	m8	m4	m2	m1

In INT1 register_1 or register_2, A1WE/A2WE, A1HE/A2HE, and A1mE/A1mE are respectively in MSB of the day of week data, hour data, and minute data by setting “1”

.

6.7 Clock Adjustment Function

A clock adjustment function is provided to logically perform slow/fast adjustment of the 32KHz clock and correct a slow/fast clock with high accuracy. Use the clock adjustment register to set this function. Write “00h” to disable the function. The clock adjustment register value is calculated by the following expression.

6.7.1 Current Frequency > Target Frequency

$$\mathrm{Re}\,gister\_value^{*1} =$$

$$128 - Integral\_value \left[\frac{Current\_oscillatoin\_frequency}{acutal\_measurement\_value^{*2}} \; \frac{-T\,\mathrm{arg}\,et\_oscillation\_frquency^{*3}}{Minimum\_resolution^{*4}} \right]$$

$$\frac{Current\_oscillation\_frequency}{actual\_measurement\_value^{*2}}$$

Caution: The figure range which can be corrected is that the calculated value is from 0 to 64.

Note:

*1. The register value is the value set to the clock adjustment register. Set the binary value of this value to the clock adjustment register.

*2. This is the measurement value of the signal that is output to the INT1# or INT2# pin when the 1 Hz clock output setting is:

32kE = 0, INT1ME = 0, INT1FE = 1, INT1# register_1 is 01h (for the INT1# pin)
INT2ME = 0, INT2FE = 1, INT1# register_2 is 01h (for the INT2 pin)

*3. This is the frequency to be adjusted by using the clock adjustment function.

*4. For the minimum resolution, 3.052ppm or 1.017ppm can be set using bit7 of the clock adjustment register. When bit7 is 0, 3.052ppm is set and logical slow/fast adjustment is performed every 20 seconds. When bit7 is 1, 1.017pm is set and logical slow/fast adjustment is performed every 60

seconds.

	0	1
Slow/fast Adjustment	Every 20 seconds	Every 60 seconds
Minimum Resolution	3.052ppm	1.017ppm
Correction Range	-195.3 to +195.3ppm	-65.1 to +64.1ppm

6.7.2 Current Oscillator Frequency < Target Frequency

$$\mathrm{Re}\,gister\_value = Integral\_value\left[\frac{(T\,\mathrm{arg}\,et\_oscillatoin\_frequency)}{(Current\_oscillation\_frequency)} \times \frac{-\begin{pmatrix} Current\_oscillator\_frequency \\ actual\_measurement\_value \end{pmatrix}}{(Minimum\_resolution)}\right]$$

Caution: The figure range which can be corrected is that the calculated value is from 0 to 62.

6.8 I2C Interface Function

The F15353 receives various commands via an I2C interface to read/write data.

6.8.1 Start Condition

The start condition is established at the point where the SDA line changes from “H” to “L” when the SCL line is “H” level. All operations start with the start condition.

6.8.2 Stop Condition

The stop condition is established at the point where the SDA line changes from “L” to “H” when the SCL line is “H” level. If the stop condition is received during a readout sequence, the read operation is discontinued and the device enters the standby mode.

6.8.3 Data Transfer

Data transfer is performed by changing the SDA line during the period that the SCL line is “L”. If the SDA line changes during the period and the SCL line is “H”, it is recognized as the start or stop condition.

6.8.4 Acknowledge

Data is transferred 8 bits in a row. Subsequently, in the 9th clock cycle period, the device on the system bus that is receiving the data changes the SDA line to “L” and returns the acknowledge signal to acknowledge data

reception.

6.8.5 Data Reading

After detecting the start condition from outside, a device code and command are received. If the read/write bit is “1” at this point, the data read mode is entered. The data output sequence is output from the LSB.

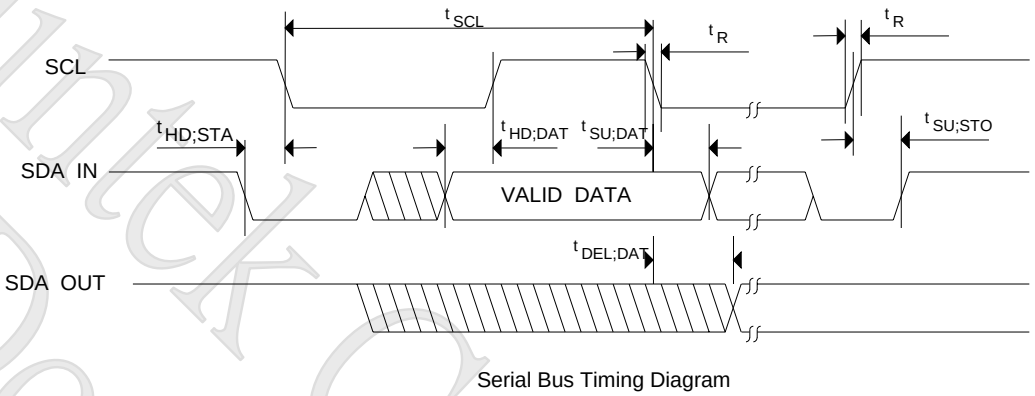


Figure 9: I2C timing chart

Table 3: Serial Bus Timing

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCL clock period	t_{SCL}	3		uS
Start condition hold time	$t_{HD;SDA}$	50		nS
Stop condition setup-up time	$t_{SU;STO}$	50		nS
DATA to SCL setup time	$t_{SU;DAT}$	50		nS
DATA to SCL hold time	$t_{HD;DAT}$	5		nS
DATA OUT to SCL delay time	$t_{DEL:DATA}$	200		ns
SCL and SDA rise time	t_R		200	nS
SCL and SDA fall time	t_F		200	nS

6.9 Data Writing

After detecting the start condition from outside, a device code and command are received. If the read/write bit is “0” at this point, the real-time data write mode or another register write mode is entered.

6.9.1 Real-time Data Access1

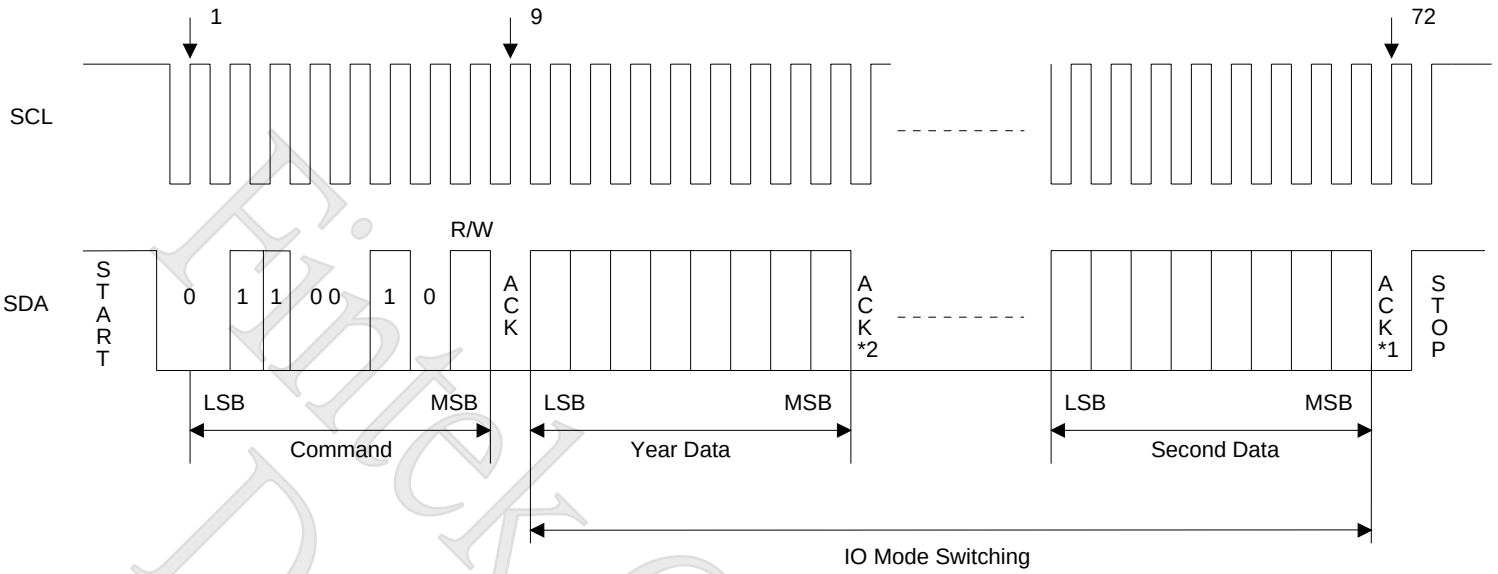


Figure 10: Real-time data access 1

*1 During reading, set NO_ACK to 1

*2 During reading, transmit ACK=0 to F15353 from the master device

6.9.2 Real-time Data Access1

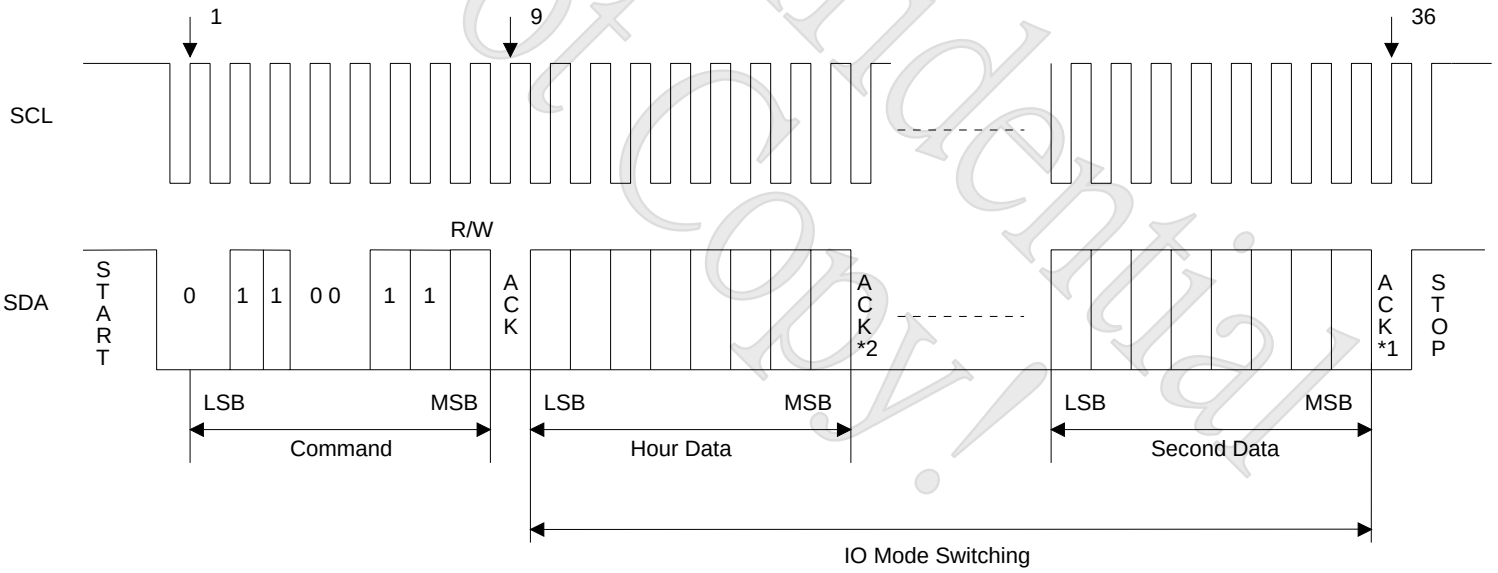


Figure 11: Real-time data access 2

*1 Set NO_ACK to 1 during reading

*2 Transmit ACK=0 to F15353 from the master device during reading

6.9.3 Status Register_1 Access and Status Register_2 Access

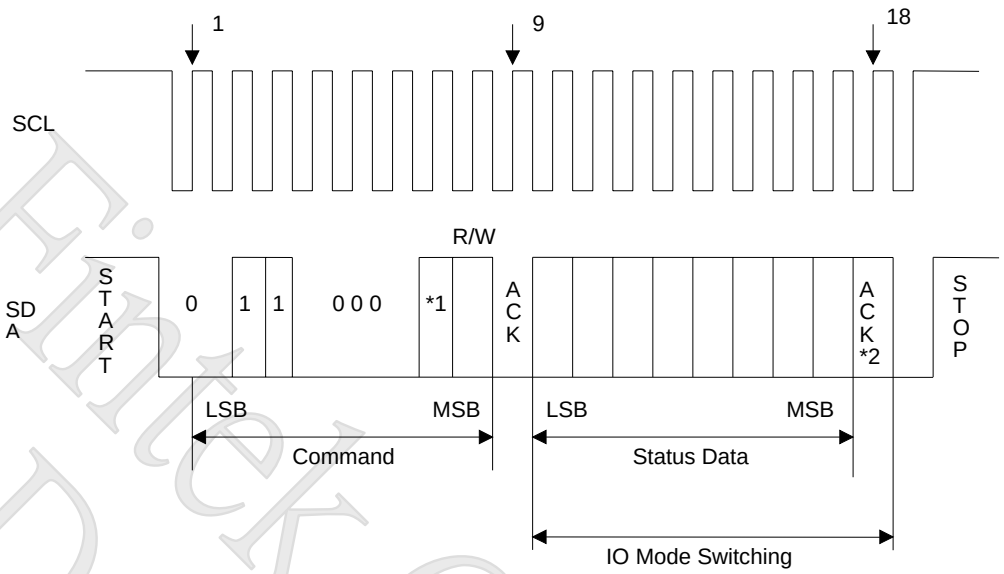


Figure 12: Status register_1 access and status register_2 access

*1 0: Status Register_1 selected, 1: Status Register_2 selected

*2 Set NO_ACK to 1 during reading

6.9.4 INT1# Register_1 Access and INT1# Register_2 Access

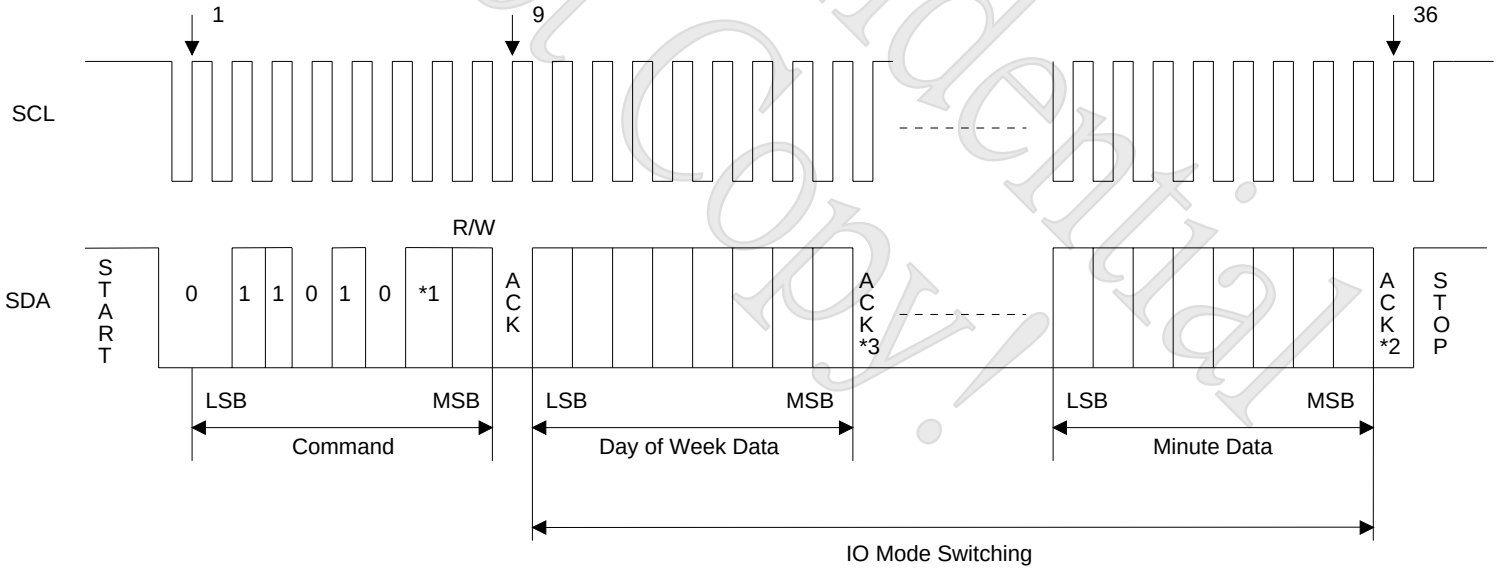


Figure 13: INT1 register_1 access and INT1 register_2 access

*1 0: Status Register_1 selected, 1: Status Register_2 selected

*2 Set NO_ACK to 1 during reading

*3 Transmit ACK=0 to F15353 from the master device during reading

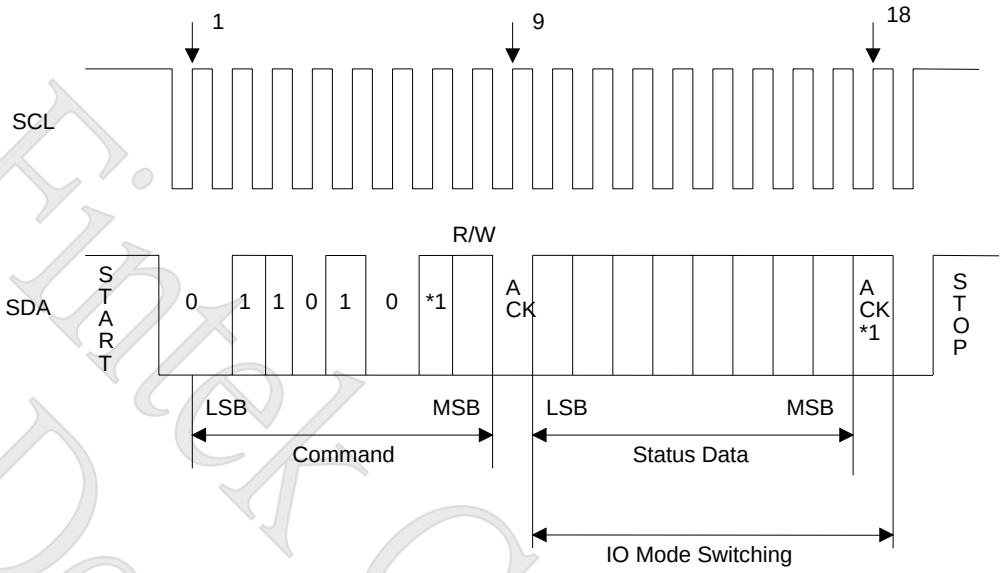


Figure 14: INT1 register_1 access and INT1 register_2 (frequency duty data) access

*1 0: Status Register_1 selected, 1: Status Register_2 selected

*2 Set NO_ACK to 1 during reading

6.9.5 Clock Adjustment Register Access

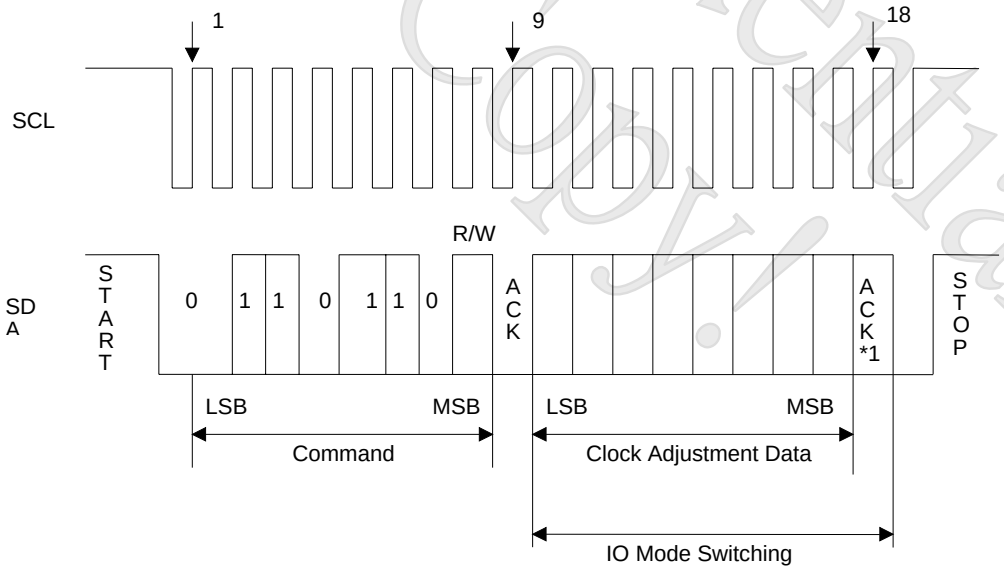


Figure 15: Clock adjustment register access

*1 Set NO_ACK to 1 during reading,

6.9.6 Free Register Access

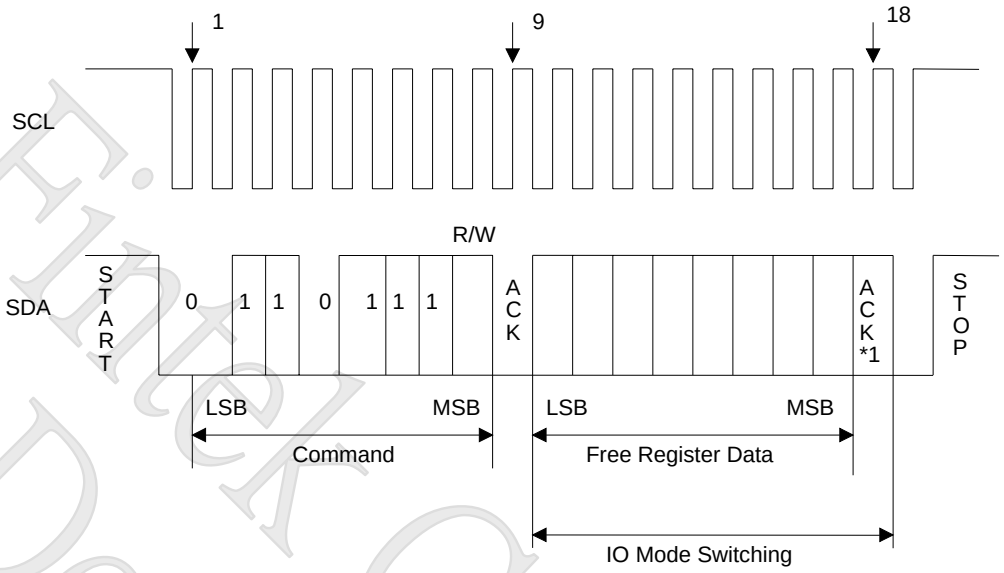


Figure 16: Free register access

*1 Set NO_ACK to 1 during reading,

6.10 Communication Data Configuration

The master device on the system generates a start condition to the slave device to communicate. Then it transmits a 4-bit device address, 3-bit command, and 1-bit read/write command on the SDA bus. The higher 4 bits that indicate the device address are called the device code and are fixed to “0110”.

Device Code				Command Code			Read/Write bit	Acknowledge bit
0	1	1	0	C2	C1	C0	R/W	ACK

7 Register Description (I2C Address = 0x6x)

7.1 Status Register_1 Access (Command 000b)

Bit	Name	R/W	Default	Description
7	POC	R	-	This flag is set to “1” at power-on. Once this flag is set to “1”, it is not set to “0” even when the power supply voltage reaches or exceeds the detection voltage (VDET). This flag is read by the status register_1 access command. It is read-only and read-clear. When the flag is “1”, it must be initialized.
6	BLD	R	-	If the power supply voltage detector detects a voltage of detection voltage (VDET) or less this flag is set to “1”, which enables the detection of a power supply voltage drop. Once this flag is set to “1”, it is not set to “0” even when the power supply voltage reaches or exceeds the detection voltage (VDET). This flag is read by the status register_1 access command. It is read-only and read-clear. When the flag is “1”, it must be initialized.
5	INT2#	R	-	When the interrupt signal is output from the INT1# pin. The INT2# flag is set to “1”, and uses the alarm interrupt function for an interrupt signal output from the INT2# pin.
4	INT1#	R	-	When the interrupt signal is output from the INT1# pin. The INT1# flag is set to “1”, and uses the alarm interrupt function for an interrupt signal output from the INT1# pin.
3	SC1	R/W	-	These flags configure a 2-bit SRAM type register that can be freely set by users. They are read and written within the operating voltage range (1.3 to 3.0 V).
2	SC0	R/W	-	These flags configure a 2-bit SRAM type register that can be freely set by users. They are read and written within the operating voltage range (1.3 to 3.0 V).
1	12/24	R/W	-	This flag is used to set 12-hour or 24-hour expression. 0: 12-hour expression 1: 24-hour expression
0	RESET	W	-	By setting this bit to “1”, the internal IC is initialized. This is a write-only bit and is always “0” when it is read. Be sure to write “1” to the reset flag when applying the power supply voltage to the IC.

7.2 Status Register_2 Access (Command 001b)

<table>
<tr><th>Bit</th><th>Name</th><th>R/W</th><th>Default</th><th>Description</th></tr>
<tr><td>7</td><td>TEST</td><td>R/W</td><td>-</td><td>The TEST flag is a bit for testing the F15353. If the TEST flag is set to “1”, the F15353 is switched to the TEST mode. If this flag is “1”, it is necessary to initialize it to “0” by setting the reset flag of status register_1 to “1”.</td></tr>
<tr><td>6</td><td>INT2#AE</td><td>R/W</td><td>-</td><td rowspan="3">These flags are used to select the output mode from the INT2# pin. Mode selections are shown below. In order to use the alarm 2 function. After setting the alarm interrupt mode, accessing INT2# register_1.
<table>
<tr><th>INT2#AE</th><th>INT2#M</th><th>INT2#FE</th><th>INT2# Pin Output Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>No interrupt</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Selected frequency steady interrupt</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Pre-minute steady interrupt</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Pre-minute steady interrupt 1 (50%)</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Alarm interrupt</td></tr>
</table></td></tr>
<tr><td>5</td><td>INT2#ME</td><td>R/W</td><td>-</td></tr>
<tr><td>4</td><td>INT2#FE</td><td>R/W</td><td>-</td></tr>
<tr><td>3</td><td>32KE</td><td>R/W</td><td>-</td><td rowspan="4">These flags are used to select the output mode from the INT1# pin. Mode selections are shown below. In order to use the alarm 1 function. After setting the alarm interrupt mode, accessing INT1# register_1.
<table>
<tr><th>32KE</th><th>INT1#AE</th><th>INT1#M</th><th>INT1#FE</th><th>INT1# Pin Output Mode</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>No interrupt</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td>32KHz output</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>Selected frequency steady interrupt</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>Pre-minute edge interrupt</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>Pre-minute edge1 interrupt (50%)</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>Alarm interrupt</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>Pre-minute edge2 interrupt (50%)</td></tr>
</table></td></tr>
<tr><td>2</td><td>INT1#AE</td><td>R/W</td><td>-</td></tr>
<tr><td>1</td><td>INT1#ME</td><td>R/W</td><td>-</td></tr>
<tr><td>0</td><td>INT1#FE</td><td>R/W</td><td>-</td></tr>
</table>

7.3 Real-time Data 1 Access, Year Data (Command 010b)

Bit	Name	R/W	Default	Description
7	Y80	R	-	Refer to bit 6.
6	Y40	R/W	-	Year data (00 to 99). Set the lower 2 digitals of the Western Calendar Year (00 to 99) and links together with the auto calendar feature until 2099.
	AMPM			For a 12-hour expression, write 0 and 1 for AM and PM, respectively. For a 24-hour expression, either 0 or 1 can be written. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.
	m40			Minute data (00 to 59)
	s40			Second data (0 to 59).
5	Y20	R/W	-	Refer to bit 6.
	D20			Day data (1 to 31)
	H20			Hour data (00 to 23 or 00 to 11)
	m20			Refer to bit 6.
	s20			
4	Y10	R/W	-	Refer to bit 6.
	M10			Month data (01 to 12). The count value is automatically changed by the auto calendar feature. 1 to 31: 31-day months (1, 3, 5, 7, 8, 10, 12) 1 to 30: 30-day months (4, 6, 9. 11) 1 to 29: 29-day months (2, leap year) 1 to 28: 28-day months (2, common year)
	D10			Refer to bit 5.
	H10			
	m10			
	s10			
3	Y8	R/W	-	Refer to bit 4.
	M8			
	D8			
	H8			
	m8			
	s8			
2	Y4	R/W	-	Refer to bit 4.
	M4			
	D4			

	W4			Day of week data (00 to 06) A septenary counter. Set it so that it corresponds to the day of the week.
	H4			Refer to bit 4.
	m4			
	s4			
1	Y2	R	-	Refer to bit 2
	M2			
	D2			
	W2			
	H2			
	m2			
	s2			
0	Y1	R	-	Refer to bit 2
	M1			
	D1			
	W1			
	H1			
	m1			
	s1			

7.4 Real-time Data 2 Access, Hour Data (Command 011b)

Bit	Name	R/W	Default	Description
7	-	-	-	Reserved
6	AMPM			For a 12-hour expression, write 0 and 1 for AM and PM, respectively. For a 24-hour expression, either 0 or 1 can be written. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.
	m40			Minute data (00 to 59)
	s40			Second data (0 to 59).
5	H20	R/W	-	Hour data (00 to 23 or 00 to 11)
	m20			Refer to bit 6.
	s20			
4	H10	R/W	-	Refer to bit 5.
	m10			
	s10			

3	H8 m8 s8	R/W	-	Refer to bit 5.
2	H4 m4 s4	R/W	-	Refer to bit 5.
1	H2 m2 s2	R/W	-	Refer to bit 5
0	H1 m1 s1	R/W	-	Refer to bit 5

7.5 INT1 Register_1 Access (Command 100b)

Alarm Time1, INT1AE=0, INT1FE=0, INT2FE=0

Bit	Name	R/W	Default	Description
7	A1WE A1HE A1mE	R/W	-	A1WE, A1HE, and A1mE are respectively in the MSB of each byte. By setting every bit to "1", the setting of the day of week data, hour data, and minute data in the corresponding bye becomes valid.
6	AM/PM	R/W	-	For a 12-hour expression, write 0 and 1 for AM and PM, respectively. For a 24-hour expression, either 0 or 1 can be written. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.
	m40			Minute data (00 to 59)
5	H20	R/W	-	Hour data (00 to 23 or 00 to 11)
	m20			Minute data (00 to 59)
4	H10 m10	R/W	-	Refer to bit 5.
3	H8 m8	R/W	-	Refer to bit 5.
2	W4	R/W	-	Day of week data (00 to 06) A septenary counter. Set it so that it corresponds to the day of the week.
	H4 m4			Refer to bit 5.
1	W2	R/W	-	Refer to bit 2

	H2			
	m2			
0	W1	R/W	-	Refer to bit 1.
	H1			
	m1			

Frequency Mode (INT1ME=0, INT1FE=1)

Bit	Name	R/W	Default	Description
7:5	SC	R/W	-	Data set in INT1 register_1 is considered as frequency duty data. By settin each bit from bit[4:0] of the register to "1", the frequency corresponding each bit is selected in an ANDed form. The SC bits configure a 3-bit SRAI type register that can be set freely by users. These bits can be read an written within the operating voltage range (1.3 to 3.0 V). There is no impa on the duty function
4	16Hz	R/W	-	Write 1 to set frequency to 16Hz
3	8Hz	R/W	-	Write 1 to set frequency to 8Hz
2	4Hz	R/W	-	Write 1 to set frequency to 4Hz
1	2Hz	R/W	-	Write 1 to set frequency to 2Hz
0	1Hz	R/W	-	Write 1 to set frequency to 1Hz

7.6 INT1 Register_2 Access (Command 101b)

Alarm Time2, INT2AE=0, INT2FE=0, INT2FE=0

Bit	Name	R/W	Default	Description
7	A2WE	R/W	-	A2WE, A2HE, and A2mE are respectively in the MSB of each byte. By setting every bit to "1", the setting of the day of week data, hour data, and minute data in the corresponding bye becomes valid.
	A2HE			
	A2mE			
6	AM/PM	R/W	-	For a 12-hour expression, write 0 and 1 for AM and PM, respectively. For a 24-hour expression, either 0 or 1 can be written. 0 is read when the hour data is from 00 to 11, and 1 is read when from 12 to 23.
	m40			Minute data (00 to 59)
5	H20	R/W	-	Hour data (00 to 23 or 00 to 11)
	m20			Minute data (00 to 59)
4	H10	R/W	-	Refer to bit 5.
	m10			

3	H8 m8	R/W	-	Refer to bit 5.
2	W4	R/W	-	Day of week data (00 to 06) A septenary counter. Set it so that it corresponds to the day of the week.
	H4 m4			Refer to bit 5.
1	W2 H2 m2	R/W	-	Refer to bit 2
0	W1 H1 m1	R/W	-	Refer to bit 1.

Frequency Mode (INT2ME=0, INT2FE=1)

Bit	Name	R/W	Default	Description
7:5	SC	R/W	-	Data set in INT1 register_2 is considered as frequency duty data. By setting each bit from bit[4:0] of the register to "1", the frequency corresponding to each bit is selected in an ANDed form. The SC bit configure a 3-bit SRAM type register that can be set freely by users. These bits can be read and written within the operating voltage range (1.3 to 3.0 V). There is no impact on the duty function
4	16Hz	R/W	-	Write 1 to set frequency to 16Hz
3	8Hz	R/W	-	Write 1 to set frequency to 8Hz
2	4Hz	R/W	-	Write 1 to set frequency to 4Hz
1	2Hz	R/W	-	Write 1 to set frequency to 2Hz
0	1Hz	R/W	-	Write 1 to set frequency to 1Hz

7.7 Clock Adjustment Register Access (Command 110b)

Bit	Name	R/W	Default	Description
7	V7	R/W	-	The clock adjustment register is a 1-byte register that is used to logically correct real-time data. When not using the clock adjustment register, set this register to 00h using the clock adjustment register write command.
6	V6	R/W	-	
5	V5	R/W	-	
4	V4	R/W	-	
3	V3	R/W	-	
2	V2	R/W	-	

1	V1	R/W	-	
0	V0	R/W	-	

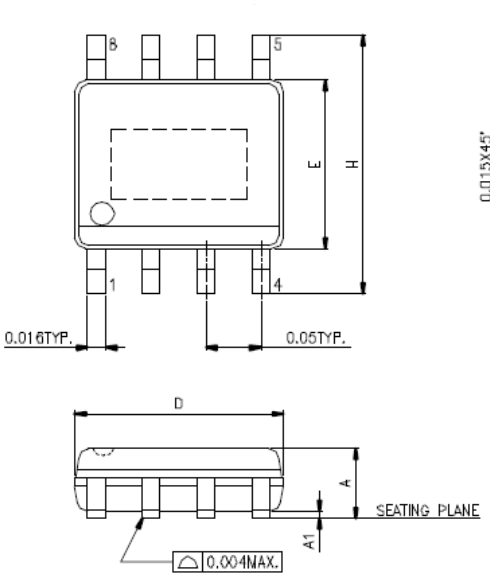
7.8 Free Register Access (Command 111b)

Bit	Name	R/W	Default	Description
7	F7	R/W	-	The free register is a 1-byte SRAM type register that can be set freely b users. It can be read and written within the operating voltage range (1.3 t 3.0 V).
6	F6	R/W	-	
5	F5	R/W	-	
4	F4	R/W	-	
3	F3	R/W	-	
2	F2	R/W	-	
1	F1	R/W	-	
0	F0	R/W	-	

8 Ordering Information

Part Number	Package Type	Production Flow
F15353S	8-SOP (Green Package)	Commercial, 0°C to +70°C
F15353G	8-TSSOP (Green Package)	Commercial, 0°C to +70°C

9 Package Dimensions (8-SOP, 8-TSSOP)

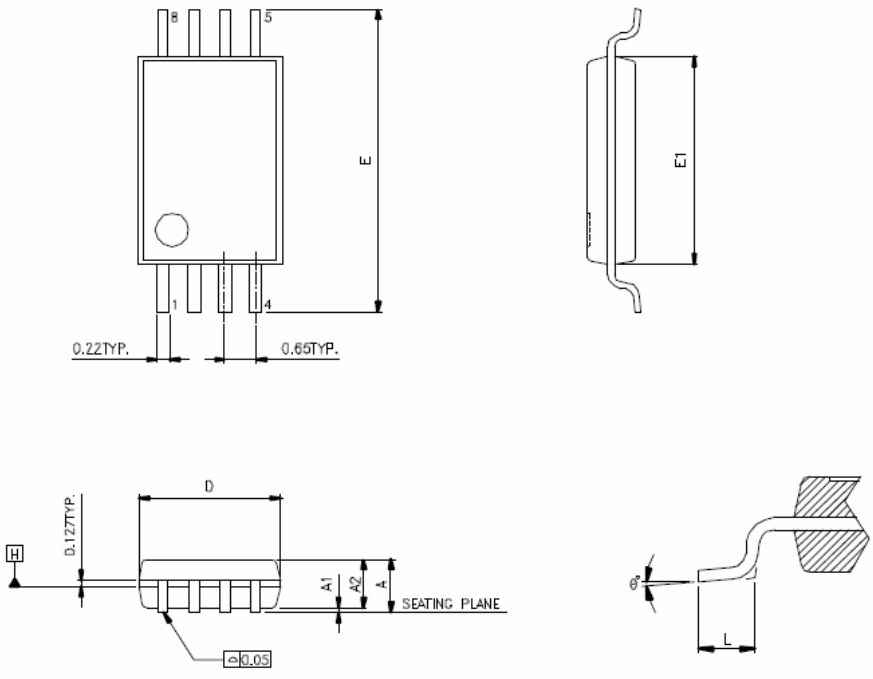


SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:
1.JEDEC OUTLINE : MS-012 AA / E.P. VERSION : N/A
2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.
3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.

Figure 17: 8 Pin SOP Package Diagram



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.96	1.01	1.06
D	2.90	3.00	3.10
E		6.40 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
θ°	0	–	8

UNIT : MM

NOTES:
1.JEDEC OUTLINE : MO-153 AA
2.DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
3.DIMENSION 'E1' DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
4.DIMENSION '0.22' DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM TOTAL IN EXCESS OF THE '0.22' DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT. MINIMUM SPAC BETWEEN PROTRUSION AND ADJACENT LEAD IS 0.07 MM.
5.DIMENSIONS 'D' AND 'E1' TO BE DETERMINED AT DATUM PLANE H.

Figure 18: 8 Pin TSSOP Package Diagram

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10 Application Circuit

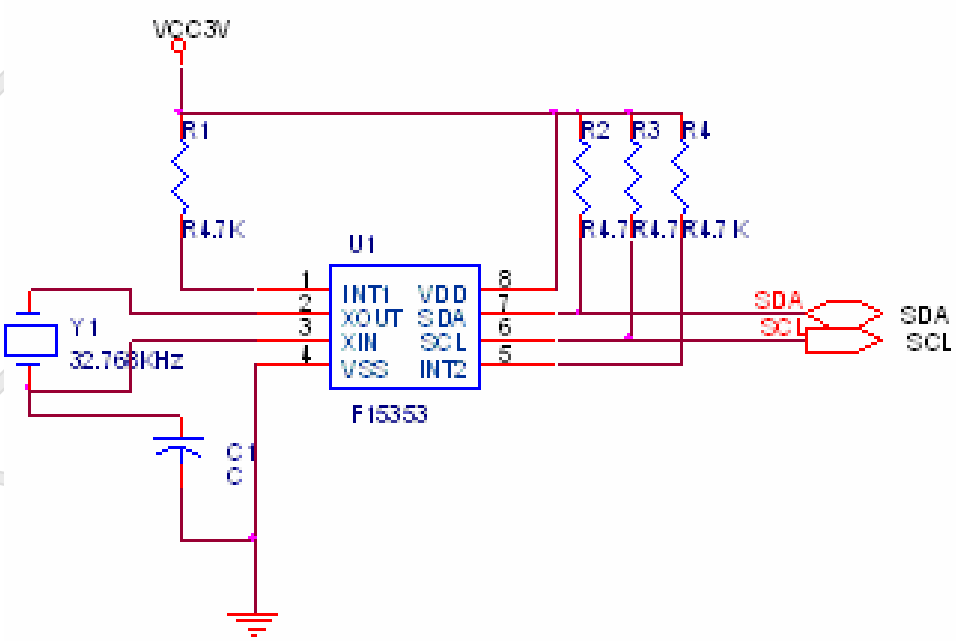

Figure 19: F15353 Application Circuit