VECTRON INTERNATIONAL
A DOVER TECHNOLOGIES COMPANY

Product Data Sheet

F-Type

Voltage Controlled Crystal Oscillator (VCXO)

The FTV Voltage Controlled Crystal Oscillator

Features

- Industry Common Pinout
- Commercial or Industrial Temperature Range
- TTL or CMOS Drive Capability
- Hermetic Package
- 5.0 V or 3.3 V Supply

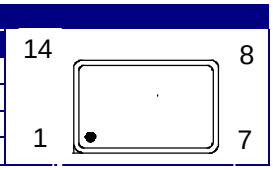
Description

The F-Type Voltage Controlled Crystal Oscillator (VCXO) is used in a phase lock loop applications including clock recovery and frequency translation applications. The metal package is grounded for improved EMI performance.

Pin Information

Table 1. Pin Function

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
7	GND	Case Ground
8	Output	VCXO Output
14	V_{DD}	Power Supply Voltage (3.3 or 5.0 V ±10%)



Performance Characteristics

Table 2. Electrical Performance

Parameter	Symbol	Minimum	Typical	Maximum	Units
Operating Temperature Range	To	0 to 70, -20 To 70, or -40 to 85			°C
Center Frequency[1]	f_0	1	-	52	MHz
Absolute Pull Range		+/- 20 to +/-100			ppm
Supply Voltage[2]	V_{DD}	3.3 or 5.0 (+/-10%)			V
Supply Current	I_{DD}	-	0.45 mA/MHz	35	mA
Output Voltage Levels[3]					
Output High	V_{OH}	0.9 V_{DD}	-		V
Output Low	V_{OL}			0.1 V_{DD}	V
Transition times[3]					
Rise Time	T_R	-	-	5.0	ns
Fall Time	T_F	-	-	5.0	ns
Fanout		-	-	10	TTL
Start-Up Time	t_{su}	-	2	-	ms
Control Voltage	V_C	0.1 V_{DD}	-	0.9 V_{DD}	V
Fanout	Fo	-	-	10 TTL	Loads

1. Other frequencies may be available, please contact factory with your special requirements.
2. A 0.1 µF low frequency tantalum bypass capacitor in parallel with a 0.01 µF high frequency ceramic capacitor is recommended. Both should be located as close to the FTU-Type bias pin as is practical
3. Figure 1 defines these parameters. Figure 2 illustrates the equivalent TTL load and operating conditions under which these parameters are specified and tested.

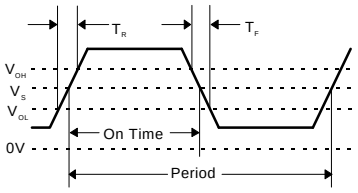


Figure 1. Output Waveform

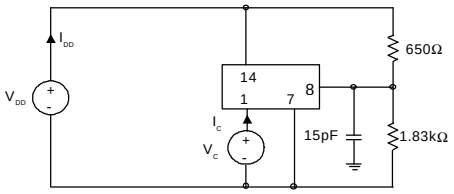


Figure 2. Output Test Conditions (25±5°C)

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. VTI employs a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation.

ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500Ω, capacitance = 100pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained by using these circuit parameters.

Table 3. ESD Threshold Voltage

Model	Threshold	Unit
Human-Body (HBM)	1000*	Volts Min.
Charged-Device (CDM)	500	Volts Min.

*Mil-STD-883D, Method 3015, Class 1

Table 4. Mechanical and Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883C, 2002.3, A
Mechanical Vibration	MIL-STD-883C, 2007.1, A
Temperature Cycle	MIL-STD-883C, 1010, A
Gross Leak	100% Deionized Water
Fine Leak	MIL-STD-883C, 1014.7
Seal Strength	2 lbs Perpendicular to Top and Bottom
Bend Test	MIL-STD-202E, 211A, C
Marking	MIL-STD-202E, 215
Storage Temperature	-55°C to 125°C

Outline Diagram

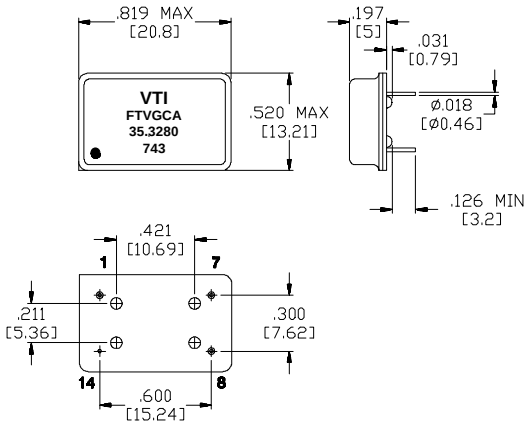


Figure 3 Outline Diagram

Ordering Information

Example Part # ⟶

Table 5. Part Numbering

F	T	V	G	C	A
Package	**Supply Voltage (V)**	**VCXO Type**	**Pull (ppm)**	**Operating Temp. (°C)**	**Output Load**
F 4 pin DIP	**T** 5.0±10%	**V** VCXO	**F** ±32	**C** 0 to 70	**A** TTL 50 ±5%
	D 3.3±10%		**G** ±50	**L** -40 to 85	**B** TTL 50 ±10%
			H ±100	**I** -20 to 70	**J** CMOS 50 ±5%
			A ±100 TPR		**K** CMOS 50 ±10%

Other specifications may be available on request.

For Additional Information Please Contact:

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