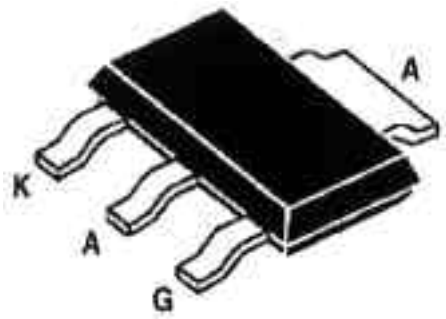
SURFACE MOUNT SCR

SOT223
(Plastic)



On-State Current
1.25 Amp

Gate Trigger Current
< 200 µA

Off-State Voltage
200 V ÷ 800 V

These series of **S**ilicon **C**ontrolled **R**ectifier use a high performance PNPN technology.

These parts are intended for general purpose applications where high gate sensitivity is required using surface mount technology.

Absolute Maximum Ratings, according to IEC publication No. 134

SYMBOL	PARAMETER	CONDITIONS	Min.	Max.	Unit
$I_{T(RMS)}$	On-state Current*	Half Cycle, Θ = 180 °, T_{tab} = 95 °C	1.25		A
$I_{T(AV)}$	Average On-state Current*	Half Cycle, Θ = 180 °, T_{tab} = 95 °C	0.8		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz, T_j = 25 °C	25		A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 50 Hz, T_j = 25 °C	22.5		A
I^2t	Fusing Current	t_p = 10ms, Half Cycle	2.5		A^2s
V_{GRM}	Peak Reverse Gate Voltage	I_{GR} = 10 µA, T_j = 25 °C	8		V
I_{GM}	Peak Gate Current	20 µs max.		1.2	A
P_{GM}	Peak Gate Dissipation	20 µs max.		3	W
$P_{G(AV)}$	Gate Dissipation	20 ms max.		0.2	W
T_j	Operating Temperature		-40	+125	°C
T_{stg}	Storage Temperature		-40	+150	°C
T_{sld}	Soldering Temperature	10s max.		260	°C

* with 5 cm^2 copper (e= 35µm) surface under tab.

SYMBOL	PARAMETER	CONDITIONS	VOLTAGE				Unit
			B	D	M	N	
V_{DRM} V_{RRM}	Repetitive Peak Off State Voltage	R_{GK} = 1 KΩ	200	400	600	800	V

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Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS		SENSITIVITY				Unit
				01	04	02	03	
I_{GT}	Gate Trigger Current	V_D = 12 V_{DC} , R_L = 140Ω, T_j = 25 °C	MIN	1	15		20	µA
			MAX	20	50	200	200	
I_{DRM} / I_{RRM}	Off-State Leakage Current	V_D = V_{DRM} , R_{GK} = 1KΩ, T_j = 125 °C	MAX	500				µA
		V_R = V_{RRM} , T_j = 25 °C	MAX	5				
V_{TM}	On-state Voltage	at I_T = 1.6 Amp, tp = 380 µs, T_j = 25 °C	MAX	1.45				V
$V_{T(O)}$	On-state Threshold Voltage	T_j = 125 °C	MAX	0.9				V
r_d	Dinamic Resistance	T_j = 125 °C	MAX	150				mΩ
V_{GT}	Gate Trigger Voltage	V_D = 12 V_{DC} , R_L = 140Ω, T_j = 25 °C	MAX	0.8				V
V_{GD}	Gate Non Trigger Voltage	V_D = V_{DRM} , R_L = 3.3KΩ, R_{GK} = 1KΩ, T_j = 125 °C	MIN	0.1				V
I_H	Holding Current	I_T = 50 mA , R_{GK} = 1KΩ, T_j = 25 °C	MAX	5				mA
I_L	Latching Current	I_G = 1 mA , R_{GK} = 1KΩ, T_j = 25 °C	MAX	6				mA
dv / dt	Critical Rate of Voltage Rise	V_D = 0.67 x V_{DRM} , R_{GK} = 1KΩ, T_j = 125 °C	MIN	15	15	10	20	V/µs
di / dt	Critical Rate of Current Rise	I_G = 2 x I_{GT} Tr ≤ 100 ns, F = 60 Hz, T_j = 125 °C	MIN	50				A/µs
$R_{th(j-l)}$	Thermal Resistance Junction-Leads for DC			25				°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient			60				°C/W

PART NUMBER INFORMATION

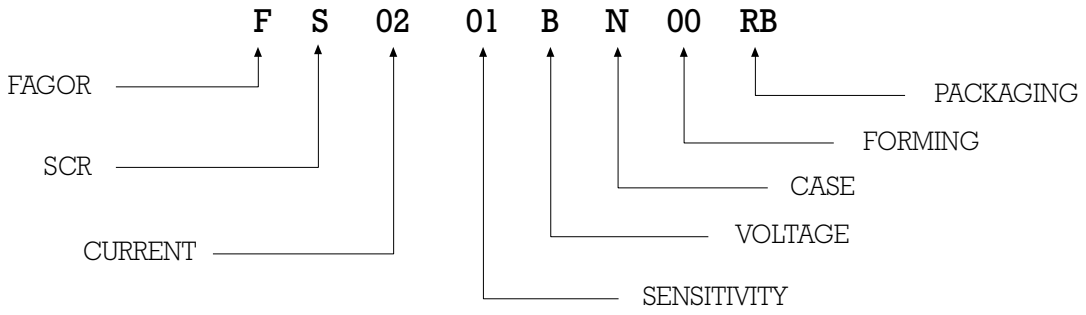

Fig. 1: Maximum average power dissipation versus average on-state current

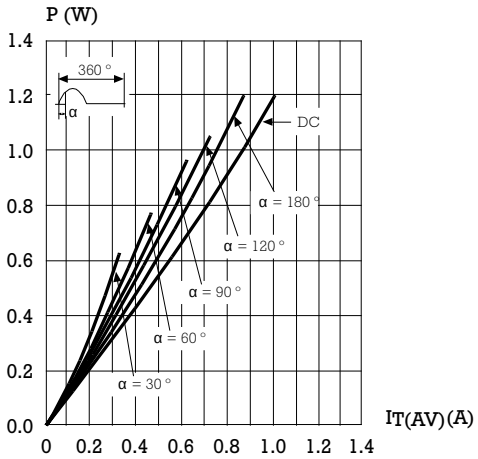

Fig. 2: Correlation between maximum average power dissipation and maximum allowable temperature (Tamb and T tab).

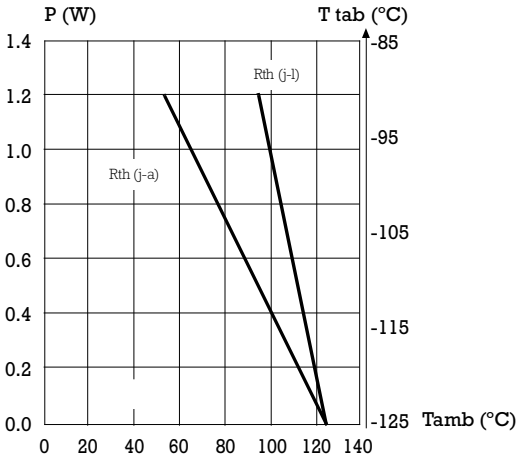

Fig. 3: Average on-state current versus tab temperature

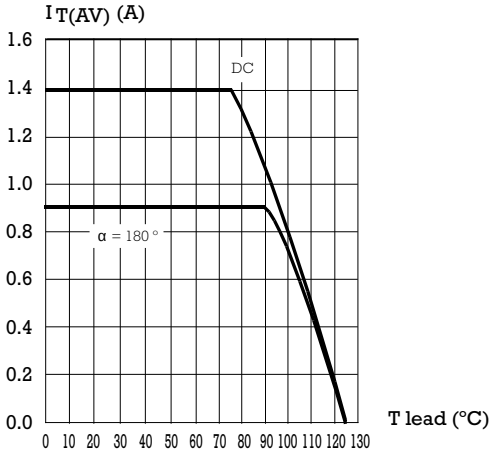

Fig. 4: Relative variation of thermal impedance junction to ambient versus pulse duration.

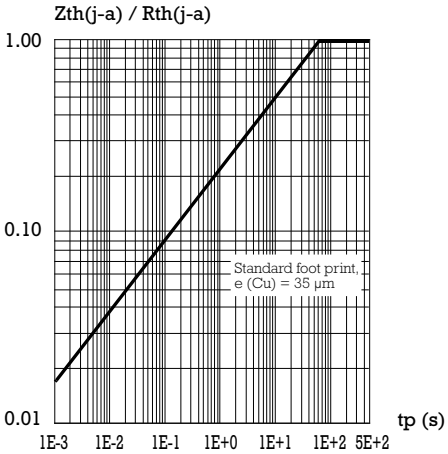

Fig. 5: Relative variation of gate trigger current and holding current versus junction temperature.

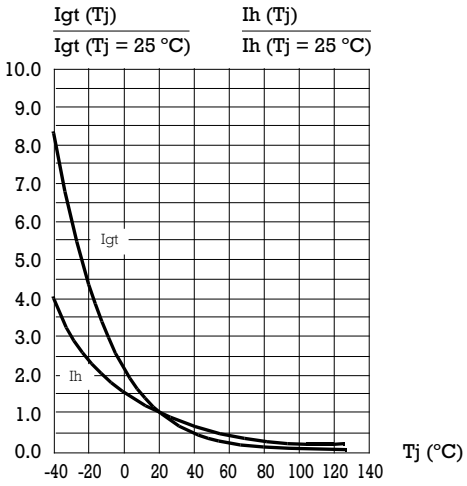

Fig. 6: Non repetitive surge peak on-state current versus number of cycles.

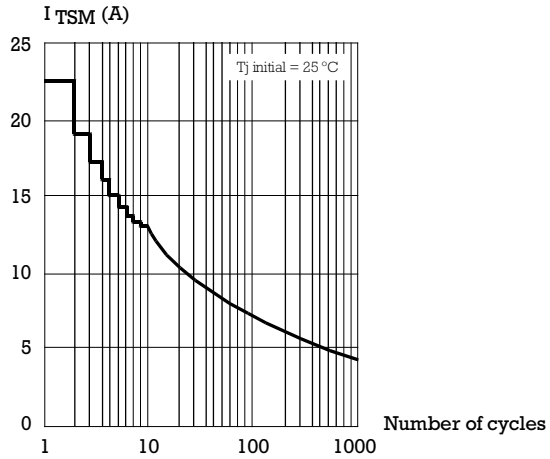

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Fig. 7: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp ≤ 10 ms, and corresponding value of I^2t.

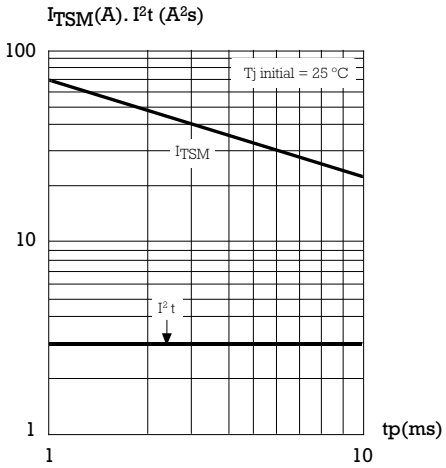
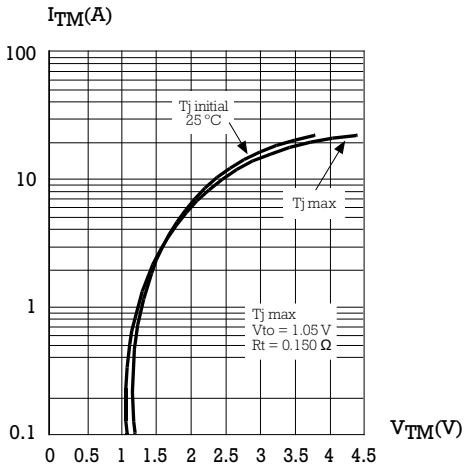
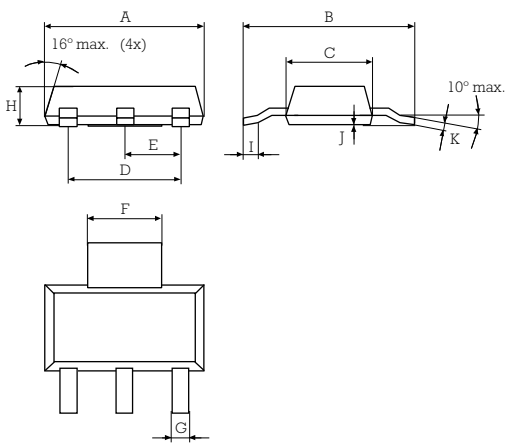


Fig. 8: On-state characteristics (maximum values).



PACKAGE MECHANICAL DATA SOT223 (Plastic)



REF.	DIMENSIONS Milimeters		
	Min.	Typ.	Max.
A	6.30	6.50	6.70
B	6.70	7.00	7.30
C	3.30	3.50	3.70
D	-	4.60	-
E	-	2.30	-
F	2.95	3.00	3.15
G	0.65	0.70	0.85
H	1.50	1.60	1.70
I	0.50	0.60	0.70
J	-	0.02	0.05
K	0.25	0.30	0.35

Weight: 0.11 g

FOOT PRINT