March 1, 2012

LM2700Q

600kHz/1.25MHz, 2.5A, Step-up PWM DC/DC Converter

General Description

The LM2700Q is a step-up DC/DC converter with a 3.6A, 80mΩ internal switch and pin selectable operating frequency. With the ability to produce 500mA at 8V from a single Lithium Ion battery, the LM2700Q is an ideal part for biasing LCD displays. The LM2700Q can be operated at switching frequencies of 600kHz and 1.25MHz allowing for easy filtering and low noise. An external compensation pin gives the user flexibility in setting frequency compensation, which makes possible the use of small, low ESR ceramic capacitors at the output. The LM2700Q features continuous switching at light loads and operates with a switching quiescent current of 2.0mA at 600kHz and 3.0mA at 1.25MHz. The LM2700Q is available in a low profile 14-lead TSSOP package or a 14-lead LLP package.

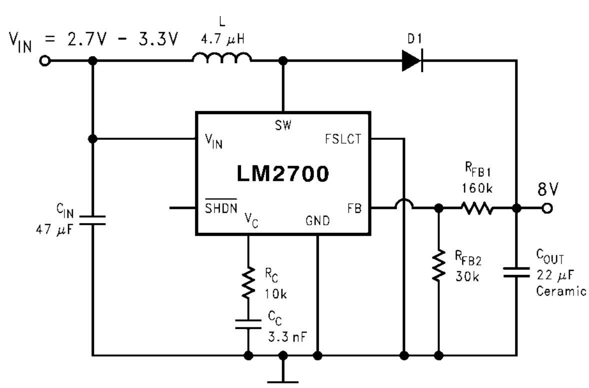
Features

- AEC-Q100 Grade 2 qualified (-40°c to +105°c)
- 3.6A, 0.08Ω, internal switch
- Operating input voltage range of 2.2V to 12V
- Input undervoltage protection
- Adjustable output voltage up to 17.5V
- 600kHz/1.25MHz pin selectable frequency operation
- Over temperature protection
- Small 14-Lead TSSOP or LLP package

Applications

- LCD Bias Supplies
- Handheld Devices
- Portable Applications
- GSM/CDMA Phones
- Digital Cameras

Typical Application Circuit



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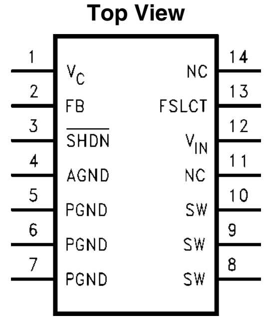
600 kHz Operation

Connection Diagram

Top View



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14-Lead TSSOP

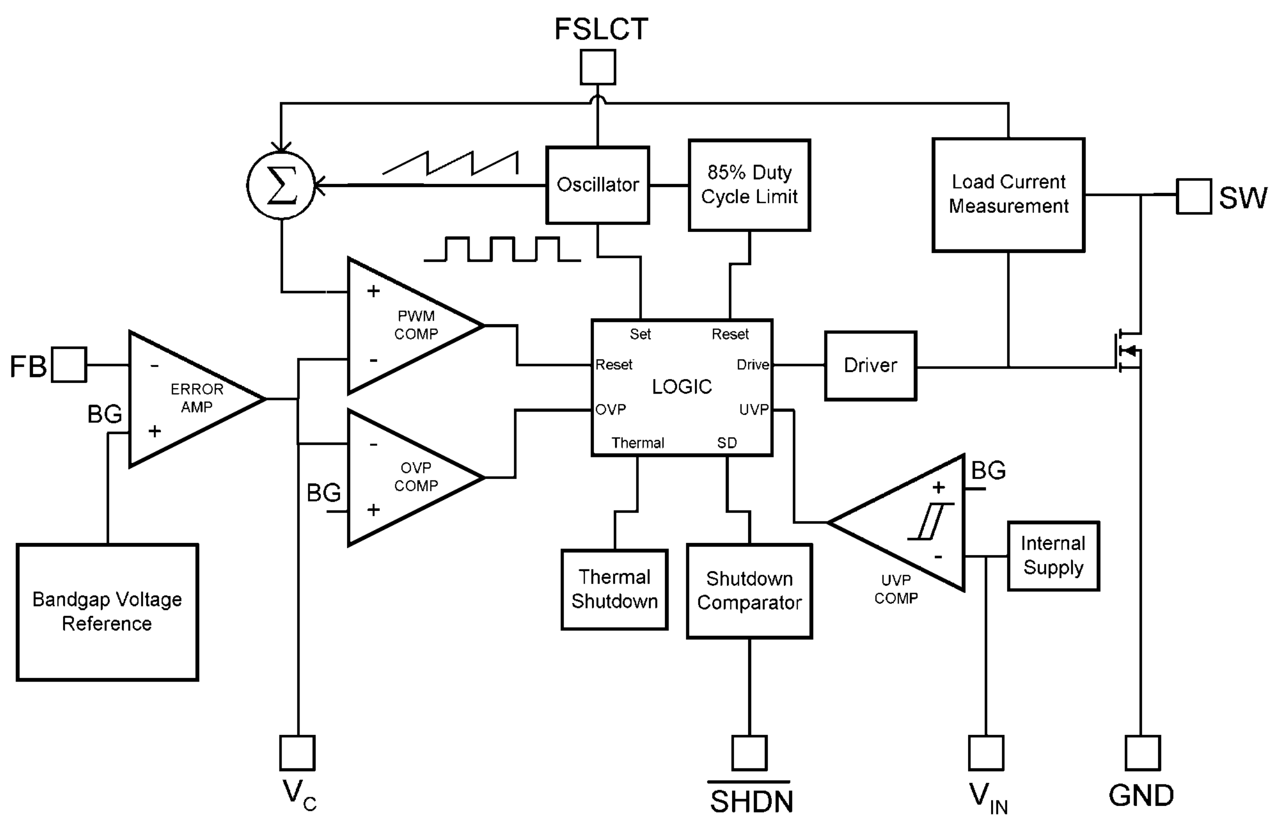
Ordering Information

Order Number	Package Type	NSC Package Drawing	Supplied As
LM2700QMT-ADJ	TSSOP-14	MTC14	94 Units, Rail
LM2700QMTX-ADJ	TSSOP-14	MTC14	2500 Units, Tape and Reel

Pin Description

Pin	Name	Function
1	V_C	Compensation network connection. Connected to the output of the voltage error amplifier.
2	FB	Output voltage feedback input.
3	$\overline{SHDN}$	Shutdown control input, active low.
4	AGND	Analog ground.
5	PGND	Power ground. PGND pins must be connected together directly at the part.
6	PGND	Power ground. PGND pins must be connected together directly at the part.
7	PGND	Power ground. PGND pins must be connected together directly at the part.
8	SW	Power switch input. Switch connected between SW pins and PGND pins.
9	SW	Power switch input. Switch connected between SW pins and PGND pins.
10	SW	Power switch input. Switch connected between SW pins and PGND pins.
11	NC	Pin not connected internally.
12	V_{IN}	Analog power input.
13	FSLCT	Switching frequency select input. V_{IN} = 1.25MHz. Ground = 600kHz.
14	NC	Connect to ground.

Block Diagram



Detailed Description

The LM2700Q utilizes a PWM control scheme to regulate the output voltage over all load conditions. The operation can best be understood referring to the block diagram and *Figure 1* of the *Operation* section. At the start of each cycle, the oscillator sets the driver logic and turns on the NMOS power device conducting current through the inductor, cycle 1 of *Figure 1* (a). During this cycle, the voltage at the V_C pin controls the peak inductor current. The V_C voltage will increase with larger loads and decrease with smaller. This voltage is compared with the summation of the SW voltage and the ramp compensation. The ramp compensation is used in PWM architectures to eliminate the sub-harmonic oscillations that occur during duty cycles greater than 50%. Once the summation of the ramp compensation and switch voltage equals the V_C voltage, the PWM comparator resets the driver logic turning off the NMOS power device. The inductor current then flows through the schottky diode to the load and output capacitor, cycle 2 of *Figure 1* (b). The NMOS power device is then set by the oscillator at the end of the period and current flows through the inductor once again.

The LM2700Q has dedicated protection circuitry running during normal operation to protect the IC. The Thermal Shutdown circuitry turns off the NMOS power device when the die temperature reaches excessive levels. The UVP comparator protects the NMOS power device during supply power startup and shutdown to prevent operation at voltages less than the minimum input voltage. The OVP comparator is used to prevent the output voltage from rising at no loads allowing full PWM operation over all load conditions. The LM2700Q also features a shutdown mode decreasing the supply current to 5µA.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

V_{IN}	12V
SW Voltage	18V
FB Voltage	7V
V_C Voltage	$0.965V \leq V_C \leq 1.565V$
$\overline{SHDN}$ Voltage (Note 1)	7V
FSLCT (Note 1)	12V
Maximum Junction Temperature	150°C
Power Dissipation(Note 3)	Internally Limited
Lead Temperature	300°C
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (Note 4)	
Human Body Model	2kV
Machine Model	200V

Operating Conditions

Operating Junction Temperature Range (Note 5)	−40°C to +105°C
Storage Temperature	−65°C to +150°C
Supply Voltage	2.2V to 12V
SW Voltage	17.5V

Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C) Unless otherwise specified. V_{IN} =2.2V and I_L = 0A, unless otherwise specified.

Symbol	Parameter	Conditions	Min (Note 5)	Typ (Note 6)	Max (Note 5)	Units
I_Q	Quiescent Current	FB = 2.2V (Not Switching) FSLCT = 0V		1.2	**2**	mA
		FB = 2.2V (Not Switching) FSLCT = V_{IN}		1.3	**2**	mA
		$V_{\overline{SHDN}}$ = 0V		5	**20**	μA
V_{FB}	Feedback Voltage		**1.2285**	1.26	**1.2915**	V
I_{CL}(Note 7)	Switch Current Limit	V_{IN} = 2.7V (Note 8)	**2.55**	3.6	**4.3**	A
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	$2.2V \leq V_{IN} \leq 12.0V$		0.02	**0.07**	%/V
I_B	FB Pin Bias Current (Note 9)			0.5	**40**	nA
V_{IN}	Input Voltage Range		**2.2**		**12**	V
g_m	Error Amp Transconductance	ΔI = 5μA	**40**	155	**290**	μmho
A_V	Error Amp Voltage Gain			135		V/V
D_{MAX}	Maximum Duty Cycle	FSLCT = Ground	**78**	85		%
D_{MIN}	Minimum Duty Cycle	FSLCT = Ground		15		%
		FSLCT = V_{IN}		30		
f_S	Switching Frequency	FSLCT = Ground	**480**	600	**720**	kHz
		FSLCT = V_{IN}	**1**	1.25	**1.5**	MHz
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}} = V_{IN}$		0.008	**1**	μA
		$V_{\overline{SHDN}}$ = 0V		−0.5	**−1**	
I_L	Switch Leakage Current	V_{SW} = 18V		0.02	**20**	μA
R_{DSON}	Switch R_{DSON} (Note 10)	V_{IN} = 2.7V, I_{SW} = 2A		80	**150**	mΩ
Th_{SHDN}	$\overline{SHDN}$ Threshold	Output High	**0.9**	0.6		V
		Output Low		0.6	**0.3**	V
UVP	On Threshold		**1.95**	2.05	**2.2**	V
	Off Threshold		**1.85**	1.95	**2.1**	V
θ_{JA}	Thermal Resistance (Note 11)	TSSOP, package only		150		°C/W
		LLP, package only		45		

Note 1: This voltage should never exceed V_{IN}.

Note 2: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 3: The maximum allowable power dissipation is a function of the maximum junction temperature, T_J(MAX), the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ – T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

Note 4: The human body model is a 100 pF capacitor discharged through a 1.5kΩ resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

Note 5: All limits guaranteed at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested or guaranteed through statistical analysis. All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Note 6: Typical numbers are at 25°C and represent the most likely norm.

Note 7: Duty cycle affects current limit due to ramp generator.

Note 8: Current limit at 0% duty cycle. See TYPICAL PERFORMANCE section for Switch Current Limit vs. V_{IN}

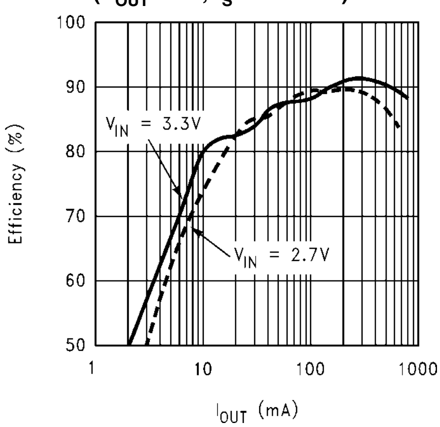
Note 9: Bias current flows into FB pin.

Note 10: Does not include the bond wires. Measured directly at the die.

Note 11: Refer to National's packaging website for more detailed thermal information and mounting techniques for the LLP and TSSOP packages.

Typical Performance Characteristics

Efficiency vs. Load Current (V_{OUT} = 8V, f_S = 600 kHz)



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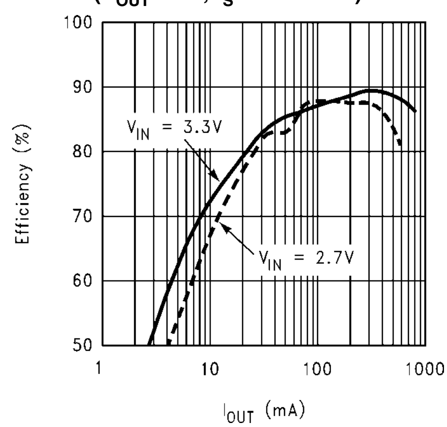
Efficiency vs. Load Current (V_{OUT} = 8V, f_S = 1.25 MHz)



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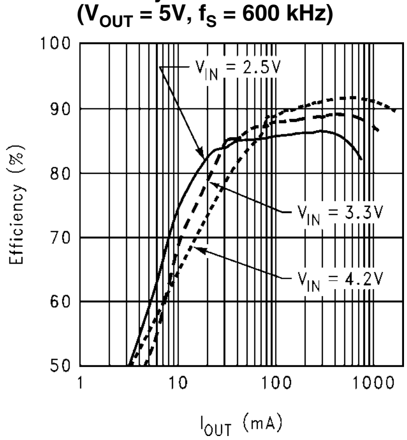
Efficiency vs. Load Current (V_{OUT} = 5V, f_S = 600 kHz)



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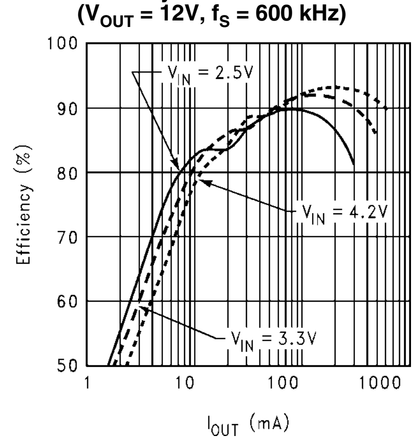
Efficiency vs. Load Current (V_{OUT} = 12V, f_S = 600 kHz)



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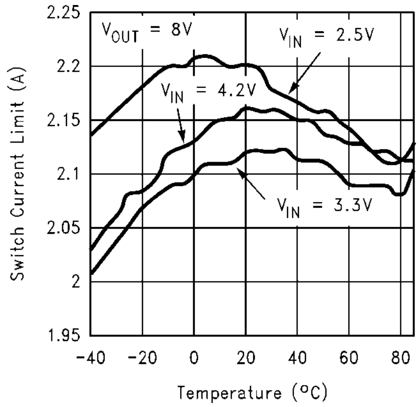
Switch Current Limit vs. Temperature



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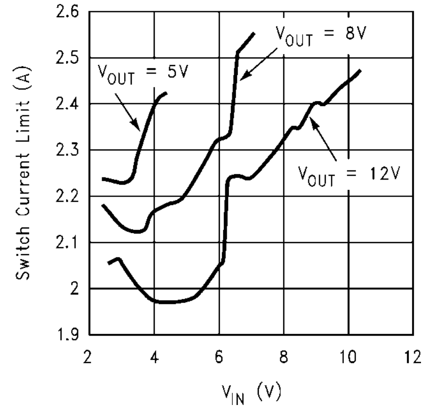
Switch Current Limit vs. V_{IN}



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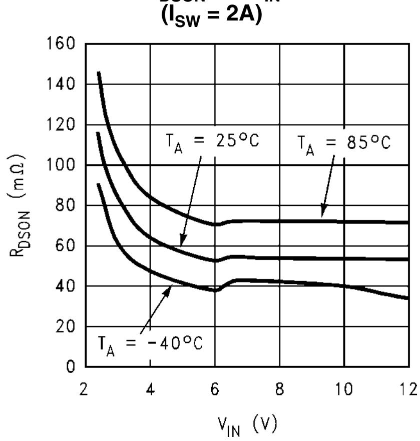
R_{DSON} vs. V_{IN} (I_{SW} = 2A)



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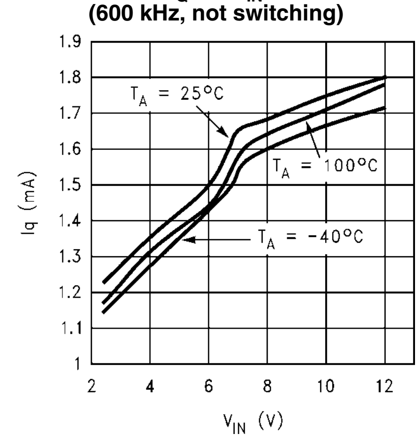
I_Q vs. V_{IN} (600 kHz, not switching)



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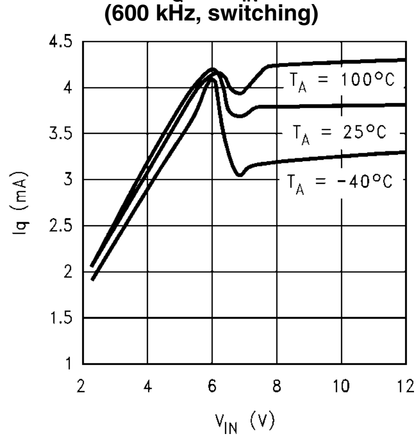
I_Q vs. V_{IN} (600 kHz, switching)



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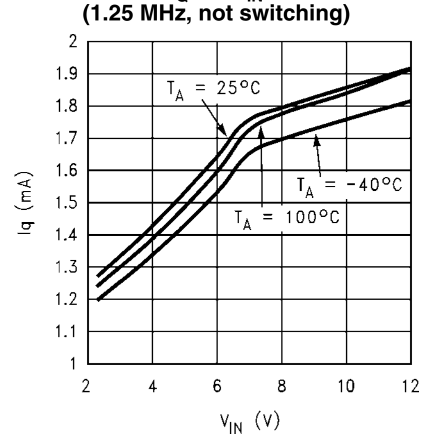
I_Q vs. V_{IN} (1.25 MHz, not switching)



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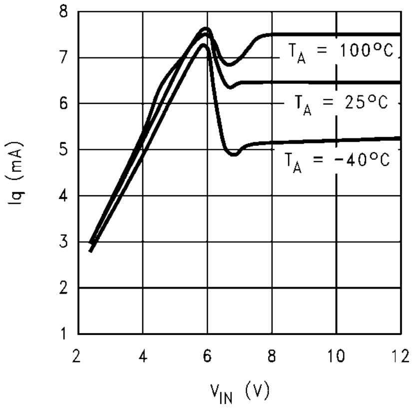
I_Q vs. V_{IN} (1.25 MHz, switching)



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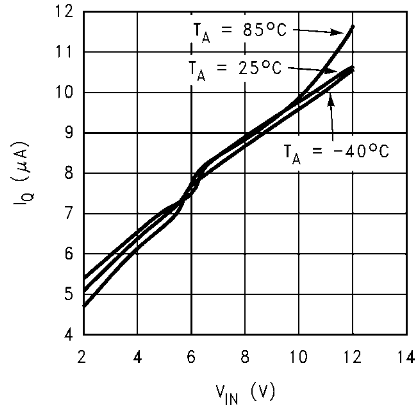
I_Q vs. V_{IN} (In shutdown)



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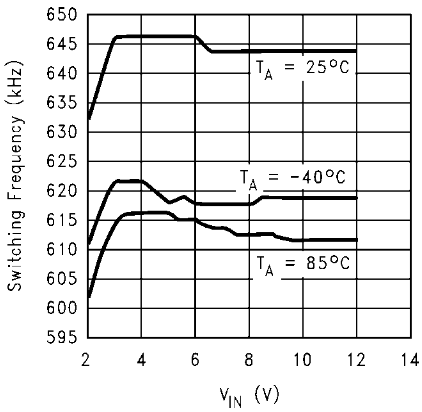
Frequency vs. V_{IN} (600 kHz)



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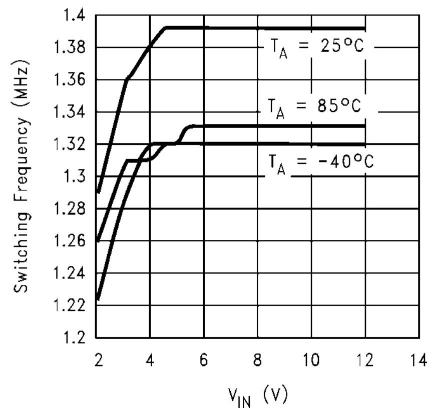
Frequency vs. V_{IN} (1.25 MHz)



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Operation

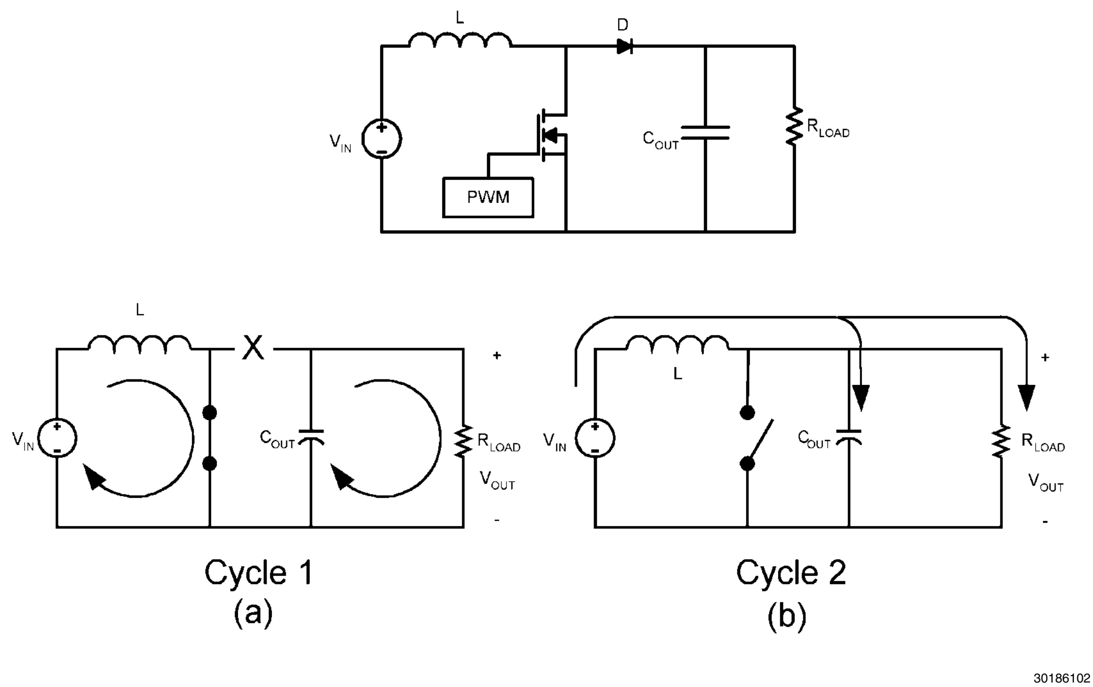


FIGURE 1. Simplified Boost Converter Diagram
(a) First Cycle of Operation (b) Second Cycle Of Operation

CONTINUOUS CONDUCTION MODE

The LM2700Q is a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in *Figure 1* (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in *Figure 1* (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1\text{-}D},\ D' = (1\text{-}D) = \frac{V_{IN}}{V_{OUT}}$$

where D is the duty cycle of the switch, D and D′ will be required for design calculations.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in *Figure 3*. The feedback pin voltage is 1.26V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 1.26}{1.26}\ \Omega$$

INTRODUCTION TO COMPENSATION

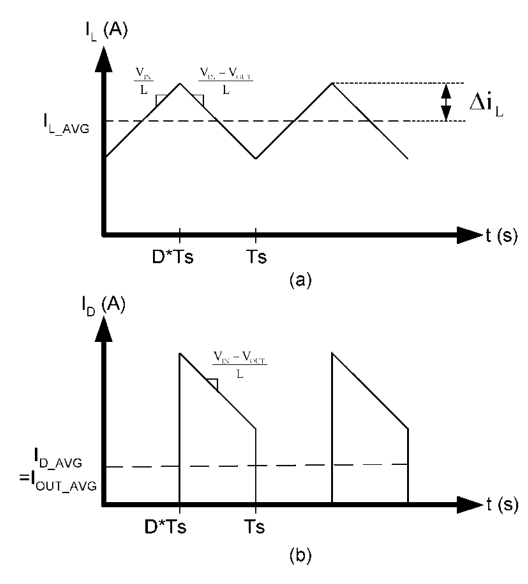


FIGURE 2. (a) Inductor current. (b) Diode current.

The LM2700Q is a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see *Figure 2* (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 4.7µH inductor is recommended for most 600 kHz applications, while a 2.2µH inductor may be used for most 1.25 MHz applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See *Inductor and Diode Selection* for more detailed inductor sizing.

The LM2700Q provides a compensation pin (V_C) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in *Figure 3*. For any given application, there exists a unique combination of R_C and C_C that will optimize the performance of the LM2700Q circuit in terms of its transient response. The series combination of R_C and C_C introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ Hz}$$

where R_O is the output impedance of the error amplifier, approximately 850kΩ. For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ R_C ≤ 20kΩ (R_C can be up to 200kΩ if C_{C2} is used, see *High Output Capacitor ESR Compensation*) and 680pF ≤ C_C ≤ 4.7nF. Refer to the *Applications Information* section for recommended values for specific circuits and conditions. Refer to the *Compensation* section for other design requirement.

COMPENSATION

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation (loads greater than approximately 100-mA), in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

INDUCTOR AND DIODE SELECTION

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN} R_{DSON}}{0.144 \text{ fs}} \left[\frac{\left(\frac{D}{D'}\right)^2 - 1}{\left(\frac{D}{D'}\right) + 1} \right] \text{(in H)}$$

where fs is the switching frequency, D is the duty cycle, and R_{DSON} is the ON resistance of the internal switch taken from the graph "R_{DSON} vs. V_{IN}" in the *Typical Performance Characteristics* section. This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The corresponding inductor current ripple as shown in *Figure 2* (a) is given by:

$$\Delta i_L = \frac{V_{IN} D}{2Lfs} \text{ (in Amps)}$$

The inductor ripple current is important for a few reasons. One reason is because the peak switch current will be the average inductor current (input current or I_{LOAD}/D') plus Δi_L. As a side note, discontinuous operation occurs when the inductor current falls to zero during a switching cycle, or Δi_L is greater than the average inductor current. Therefore, continuous conduction mode occurs when Δi_L is less than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in *Figure 2* (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45°) is desired for the best stability and transient response. For the purpose of stabilizing the LM2700Q, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin. A discussion of the right half plane zero and checking the crossover using the DC gain will follow.

INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful condtions while a 33µF or 47µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2\Delta i_L R_{ESR} \text{ (in Volts)}$$

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)}$$

$$f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}} \text{ (in Hz)}$$

Where R_L is the minimum load resistance corresponding to the maximum load current. The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the *High Output Capacitor ESR Compensation* section.

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90° in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$\text{RHPzero} = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD} L} \text{ (in Hz)}$$

where I_{LOAD} is the maximum load current.

SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components R_C and C_C is to set a dominant low frequency pole in the control loop. Simply choose values for R_C and C_C within the ranges given in the *Introduction to Compensation* section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi(R_C + R_O)C_C} \text{ (in Hz)}$$

where R_O is the output impedance of the error amplifier, approximately 850kΩ. Since R_C is generally much less than R_O, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel out the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)}$$

Now R_C can be chosen with the selected value for C_C. Check to make sure that the pole f_{PC} is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range. After checking the design at the end of this section, these values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of R_C should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimal performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C2}, directly from the compensation pin V_C to ground, in parallel with the series combination of R_C and C_C. The pole should be placed at the same frequency as f_{Z1}, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2}(R_C // R_O)} \text{ (in Hz)}$$

To ensure this equation is valid, and that C_{C2} can be used without negatively impacting the effects of R_C and C_C, f_{PC2} must be greater than $10f_{ZC}$.

CHECKING THE DESIGN

The final step is to check the design. This is to ensure a bandwidth of ½ or less of the frequency of the RHP zero. This is done by calculating the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a −20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding C_{C2} as discussed earlier in the section. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega c L_{eff}) // R_L] // R_L\}\right\rangle \text{ (in dB)}$$

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)}$$

$$L_{eff} = \frac{L}{(D')^2}$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)}$$

$$mc \cong 0.072fs \text{ (in V/s)}$$

$$m1 \cong \frac{V_{IN}R_{DSON}}{L} \text{ (in V/s)}$$

where R_L is the minimum load resistance, V_{IN} is the minimum input voltage, g_m is the error amplifier transconductance found in the *Electrical Characteristics* table, and R_{DSON} is the value chosen from the graph "R_{DSON} vs. V_{IN} " in the *Typical Performance Characteristics* section.

LAYOUT CONSIDERATIONS

The LM2700Q uses two separate ground connections, PGND for the driver and NMOS power device and AGND for the sensitive analog control circuitry. The AGND and PGND pins should be tied directly together at the package. The feedback and compensation networks should be connected directly to a dedicated analog ground plane and this ground plane must connect to the AGND pin. If no analog ground plane is available then the ground connections of the feedback and compensation networks must tie directly to the AGND pin. Connecting these networks to the PGND can inject noise into the system and effect performance.

The input bypass capacitor C_{IN}, as shown in *Figure 3*, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN} pin, to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R_{FB1} and R_{FB2}, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. For more detail on switching power supply layout considerations see Application Note AN-1149: *Layout Guidelines for Switching Power Supplies*.

Application Information

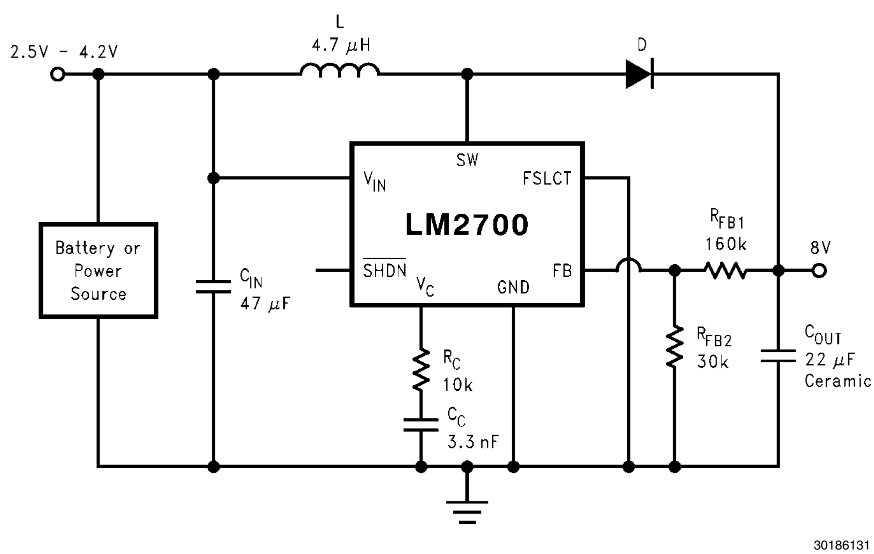


FIGURE 3. 600 kHz operation, 8V output

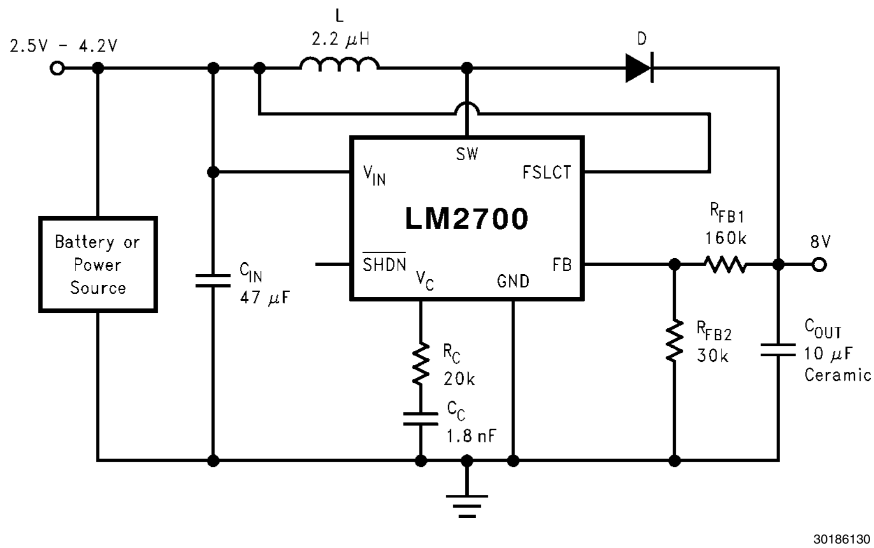


FIGURE 4. 1.25 MHz operation, 8V output

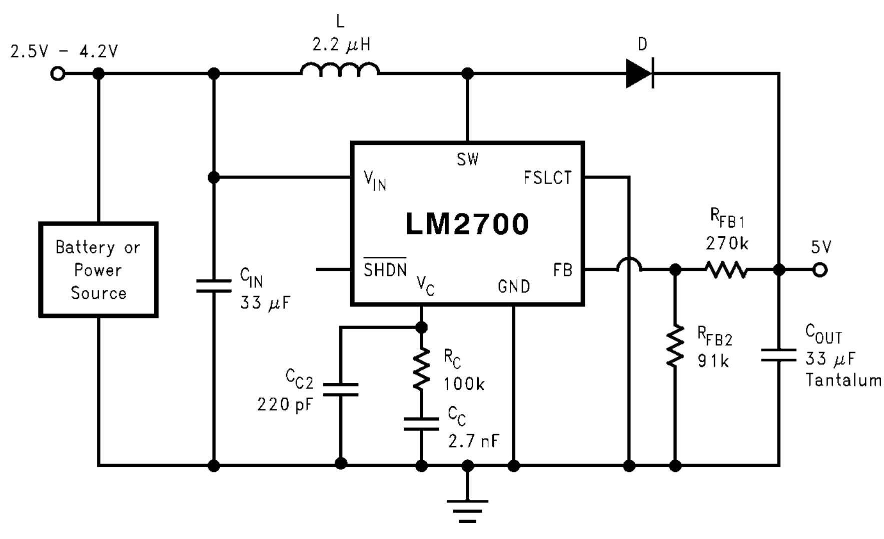
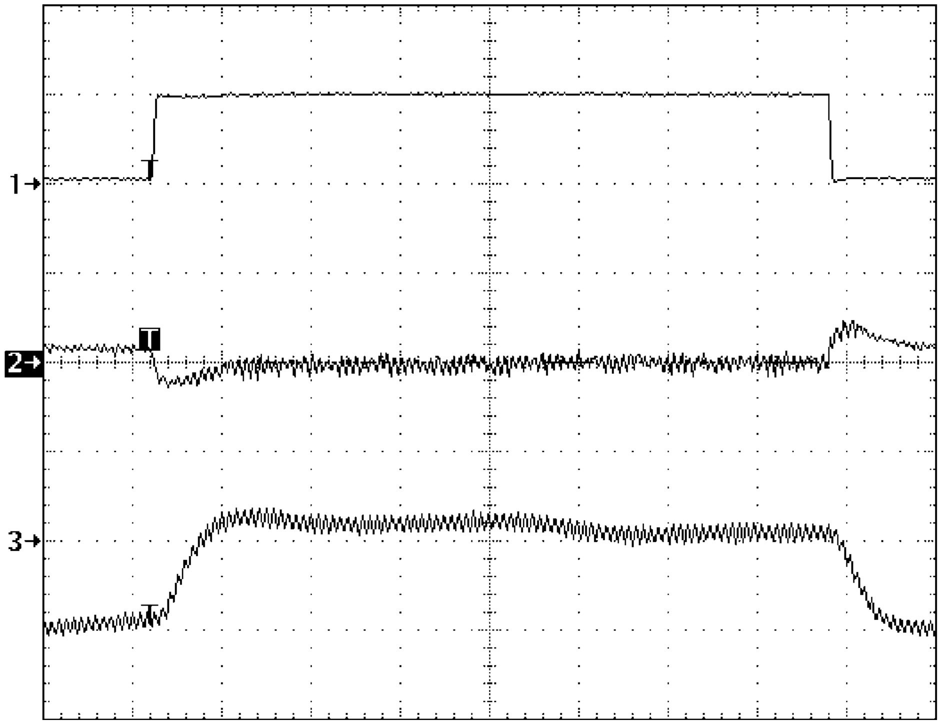


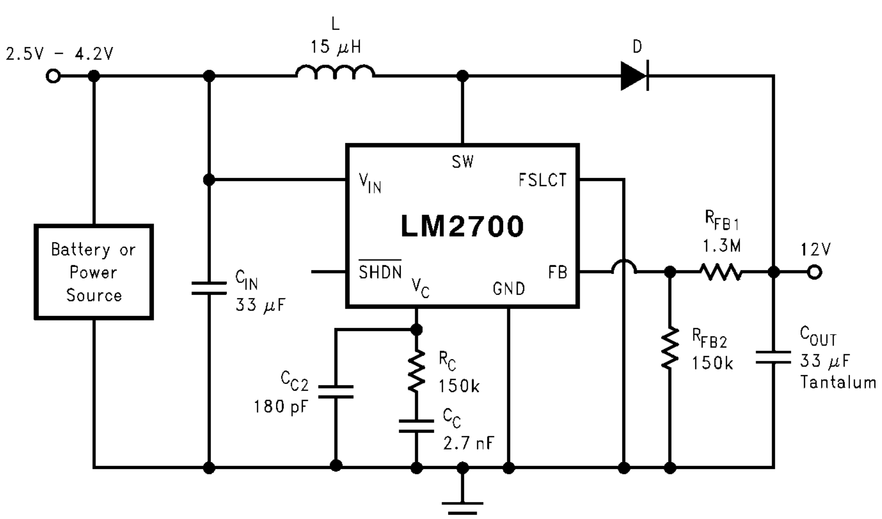
FIGURE 5. 600 kHz operation, 5V output



30186152

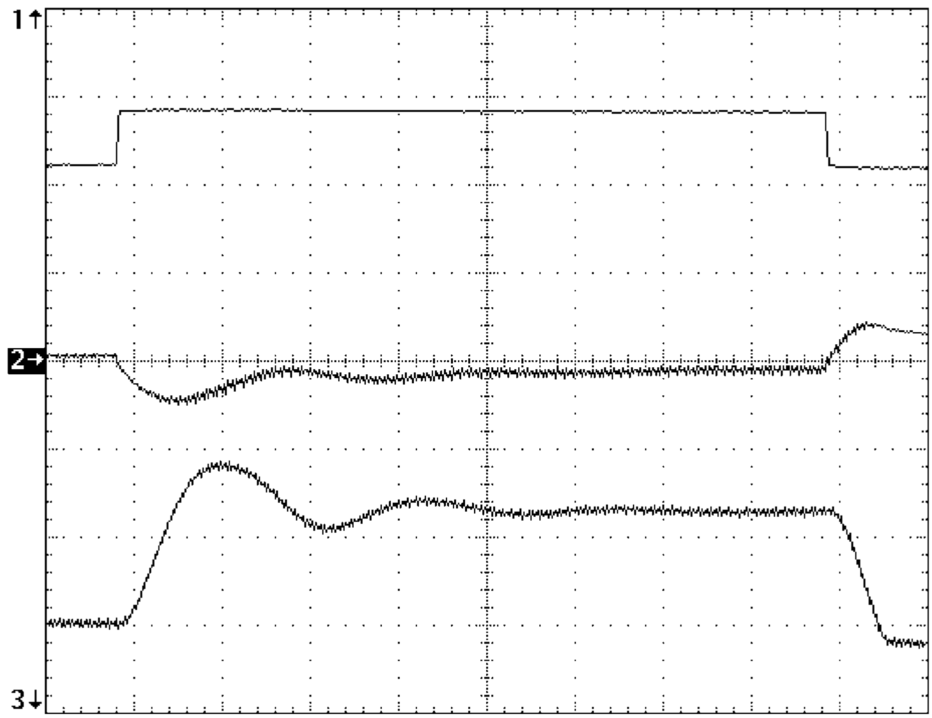
V_{IN} = 3.3V, I_{OUT} = 200mA~> 700mA ~>200mA
CH1: I_{OUT} 0.5A/div DC Coupled
CH2: V_{OUT} 500mV/div AC Coupled
CH3: Inductor Current 1A/div DC Coupled
20µs/div

Load Transient for *Figure 5*



30186133

FIGURE 6. 600 kHz operation, 12V output



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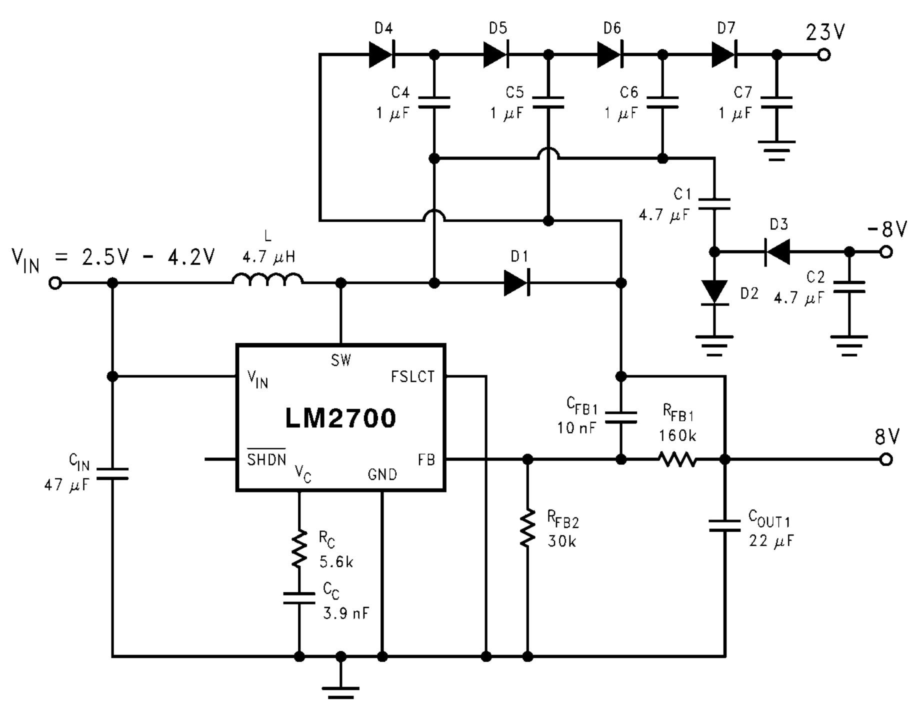
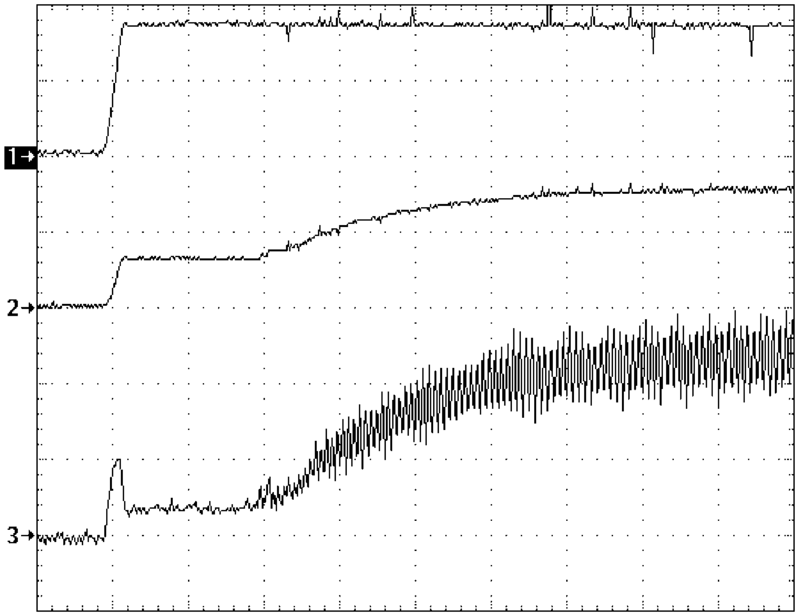
V_{IN} = 3.3V, I_{OUT} = 50mA~> 350mA ~>50mA
CH1: I_{OUT} 0.5A/div DC Coupled
CH2: V_{OUT} 500mV/div AC Coupled
CH3: Inductor Current 1A/div DC Coupled
50µs/div

Load Transient for *Figure 6*



30186108

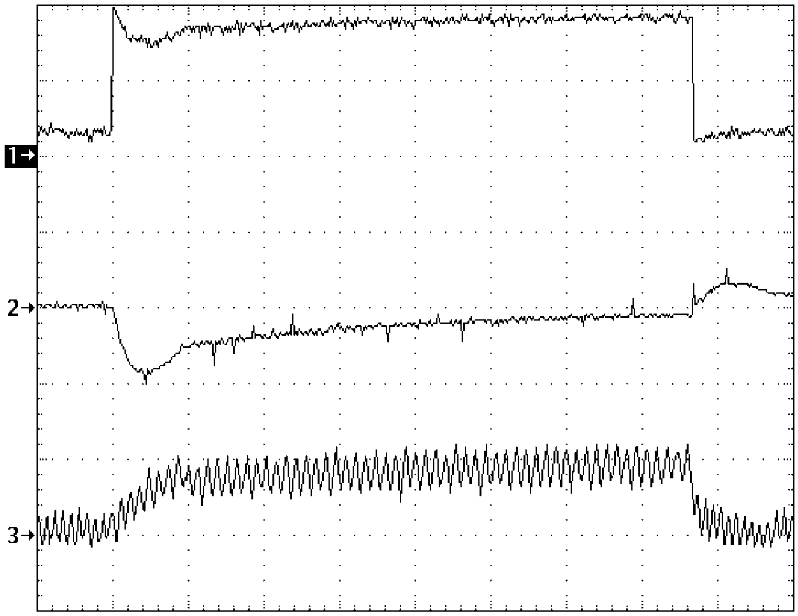
FIGURE 7. Triple Output TFT Bias (600 kHz operation)



30186149

V_{IN} = 3.3V, I_{OUT} = 500mA
CH1: V_{IN} 2V/div DC Coupled
CH2: V_{OUT} 5V/div DC Coupled
CH3: Inductor Current 500mA/div DC Coupled
1ms/div

Start Up Waveform for *Figure 7*

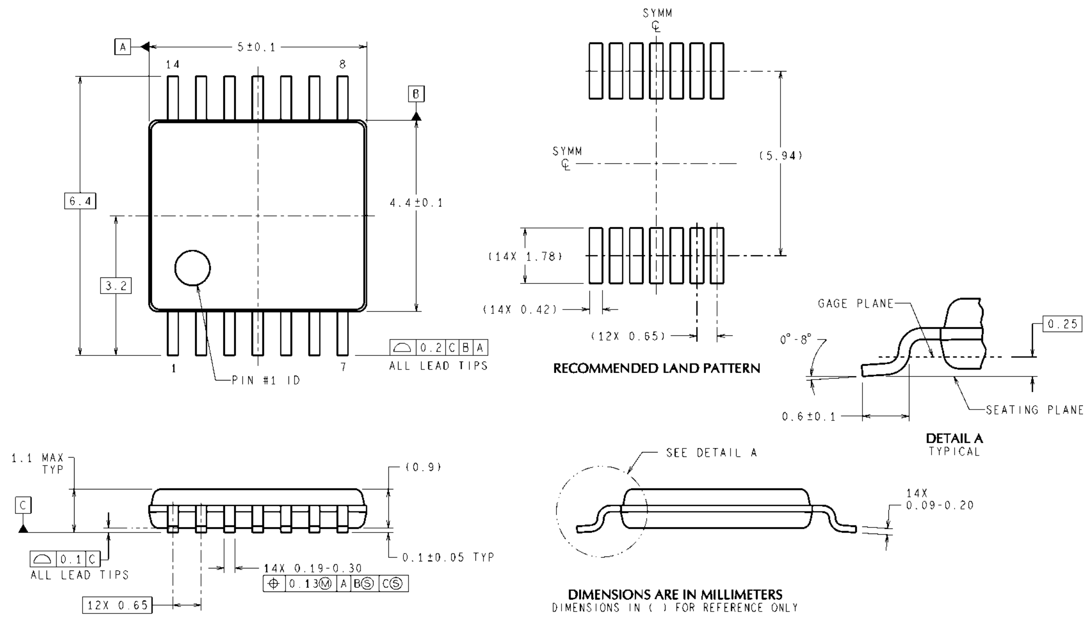


30186150

V_{IN} = 3.3V, I_{OUT} = 50mA~> 375mA ~>50mA
CH1: I_{OUT} 0.2A/div DC Coupled
CH2: V_{OUT} 2V/div AC Coupled
CH3: Inductor Current 1A/div DC Coupled
500µs/div

Load Transient for *Figure 7*, 8V Output

Physical Dimensions inches (millimeters) unless otherwise noted



MTC14 (Rev D)

TSSOP-14 Pin Package (MTC)
For Ordering, Refer to Ordering Information Table
NS Package Number MTC14

Notes

Notes