ISO 11'784 / 11'785 COMPLIANT READ ONLY CONTACTLESS IDENTIFICATION DEVICE

Features

- 128 bit memory array laser programmable
- Bit duration : 32 periods of RF field
- Bit coding according to ISO FDX-B
- On chip resonnance capacitor
- On chip supply buffer capacitor
- Wide dynamic range
- On chip voltage limiter
- Full wave rectifier
- Large modulation depth
- Operating frequency 100 - 150 kHz
- Very small chip size convenient for implantation
- Very low power consumption

Typical Operating Configuration

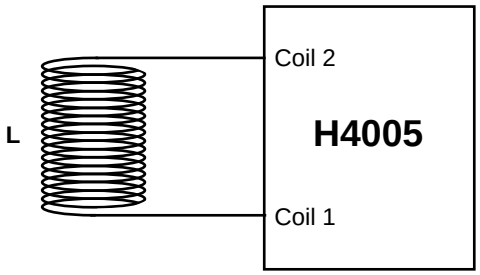


Fig. 1

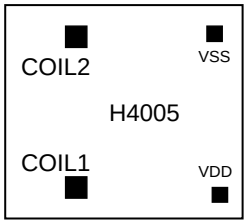
Description

The H4005 is a CMOS integrated circuit intented for use in electronic Read Only RF Transponders. The circuit is powered by an external coil placed in an electromagnetic field, and gets its master clock from the same field via one of the coil terminals. The other coil terminal is affected by the modulator. By turning on and off the modulation current, the chip will send back the 128 bits of information contained in a factory pre-programmed memory array.

The programming of the chip is performed by laser fusing of polysilicon links in order to store a unique code on each chip.

Due to the low power consumption of the logic core, no supply buffer capacitor is required. Only an external coil is needed to obtain the chip function. A parallel resonance capacitor of 75 pF is also integrated.

Pin Assignment



COIL 1	Coil terminal / Clock input
COIL 2	Coil terminal

Fig. 2

Applications

- Animal implantable transponder
- Animal ear tag
- Industrial transponder

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum AC peak Current induced on COIL1 and COIL2	I_{COIL}	± 30 mA
Power Supply	V_{DD}	-0.3 to 7.5 V
Storage temperature	T_{store}	-55 to +200°C
Electrostatic discharge maximum to MIL-STD-883C method 3015	V_{ESD}	1000 V

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device.
Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Temperature	T_{op}	-40		+85	°C
Maximum coil current	I_{COIL}			10	mA
AC Voltage on Coil	V_{coil}		14*		Vpp
Supply Frequency	f_{coil}	100		150	kHz

Table 2

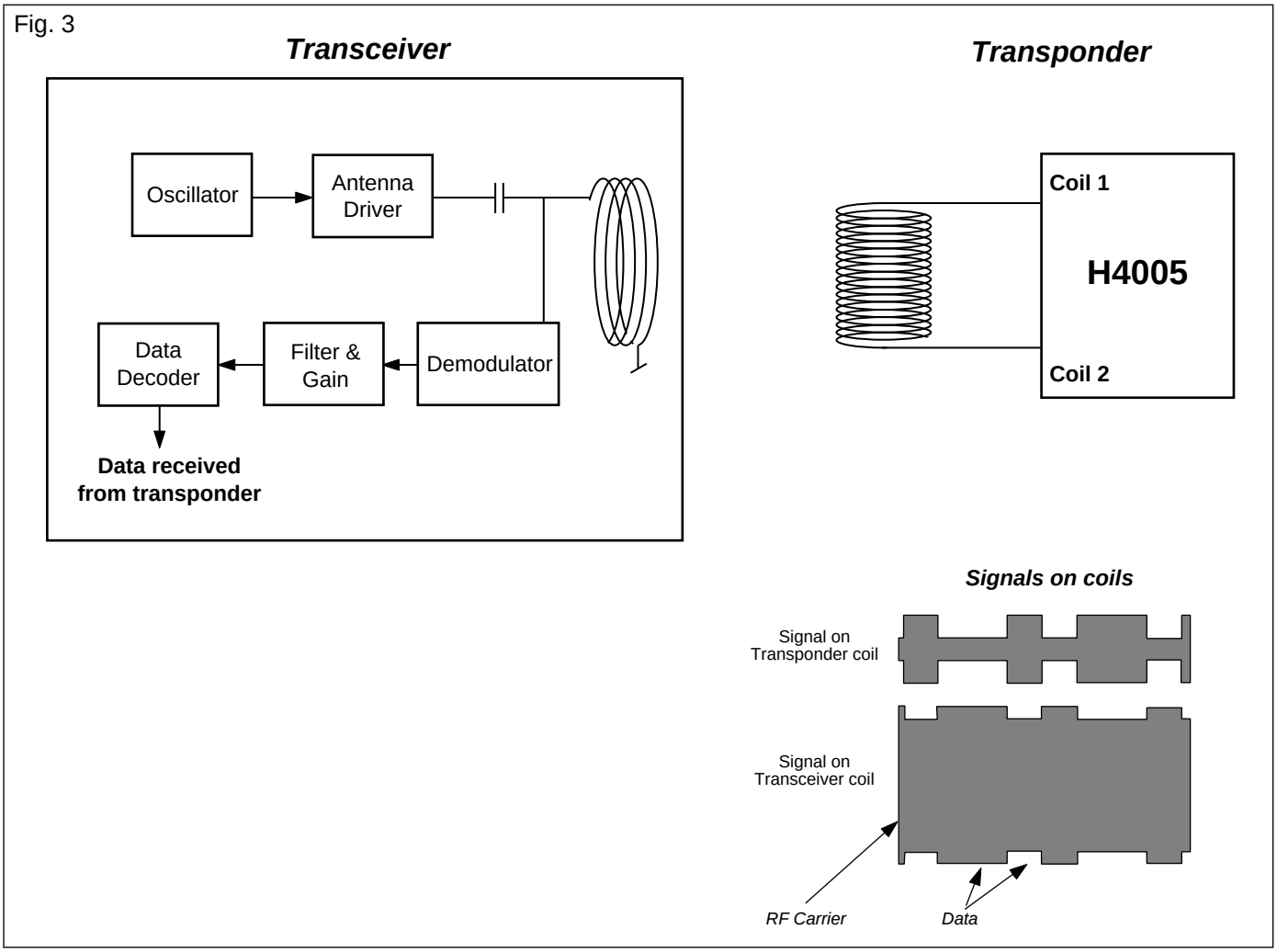
*) The AC Voltage on Coil is limited by the on chip voltage limitation circuitry.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component.

System Principle

Fig. 3



Electrical Characteristics

V_{DD} = 1.5 V V_{SS} = 0 V f_{coil} = 134 kHz Sine wave T_{op} = 25°C
V_{C1} = 1.0 V with positive peak at V_{DD} and negative peak at V_{DD} - 1 V unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{DD}		1.5		1)	V
Supply Current	I_{DD}				1.5	µA
Rectified Supply Voltage	V_{DD}	V_{C2} -V_{C1} = 2.8 VDC Modulator Switch = "ON"	1.5			V
C2 pad Modulator ON voltage drop	V_{ONC2}	V_{DD} = 1.5V I_{VDDC2} = 100 µA with ref. to V_{DD} V_{DD} = 5.0V I_{VDDC2} = 1 mA with ref. to V_{DD}	0.9 2.1		1.3 3.0	V V
C1 pad Modulator ON voltage drop	V_{ONC1}	V_{DD} = 5.0V I_{VDDC1} = 1 mA with ref. to V_{DD}	2.1		3.0	V
Coil1 - Coil2 capacitance	C_{res}	V_{coil} = 100 mVRMS f = 10 kHz		75 2)		pF
Power Supply Capacitor	C_{sup}			150		pF

1) The maximum voltage is defined by forcing 10 mA on C1 - C2
2) The toleranceof the resonant capacitor is ± 15 % over the whole production. On a wafer basis and on process statistics, the tolerance is ± 2%

Table 3

Timing Characteristics

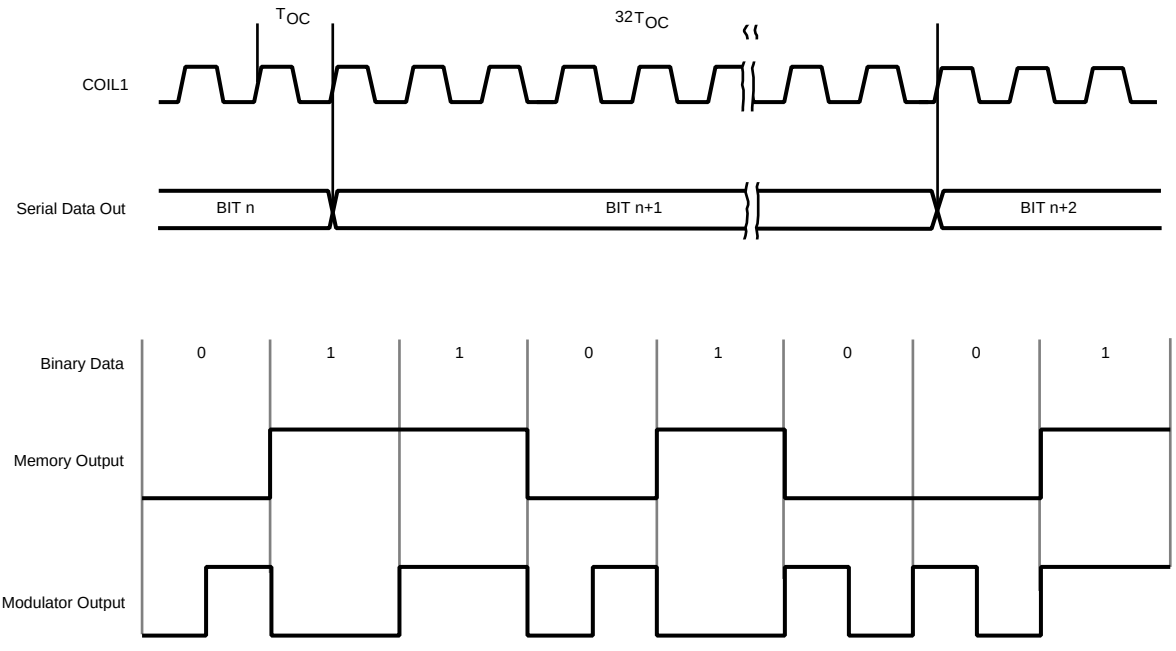
V_{DD} = 1.5 V V_{SS} = 0 V f_{coil} = 134 kHz Sine wave T_{op} = 25°C
V_{C1} = 1.0 V with positive peak at V_{DD} and negative peak at V_{DD} - 1 V unless otherwise specified
Timings are derived from the field frequency and are specified as a number of RF periods.

Parameter	Symbol	Test Conditions	Value	Units
Read Bit Period	t_{rdb}		32	RF periods

Table 4

Timing Waveforms

Fig. 4



Block Diagram

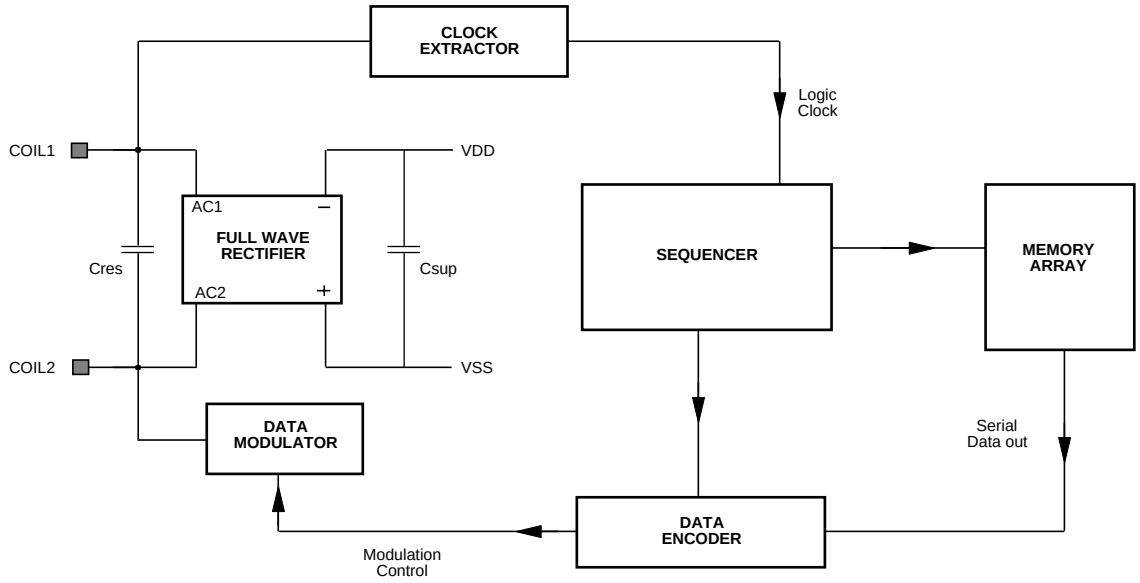


Fig. 4

Functional Description

General

The H4005 is supplied by means of an electromagnetic field induced on the attached coil. The AC voltage is rectified in order to provide a DC internal supply voltage. When the DC voltage is sufficient the chip sends data continuously. When the last bit is sent, the chip will continue with the first bit until the power goes off.

Full Wave Rectifier

The AC input induced in the external coil by an incident magnetic field is rectified by a Graetz bridge. The bridge will limit the internal DC voltage to avoid malfunction in strong fields.

Clock extractor

One of the coil terminals (COIL1) is used to generate the master clock for the logic function. The output of the clock extractor drives a sequencer.

Sequencer

The sequencer provides all necessary signals to address the memory array and to encode the serial data out. The data rate is set to 32 clocks per bit.

Data Encoder

The data is coded according to the FDX-B scheme. At the beginning of each bit, a transition will occur. A logic bit "1" will keep its state for the whole bit duration and a logic bit "0" will show a transition in the middle of the bit duration (refer to fig. 4). The FDX-B allows an advance of up to 8 clocks in the ON to OFF transition. Due to its low power consumption, there is no difference in performance for the H4005 when implementing a transition advance. No clock advance is provided on the standard version.

Data Modulator

The data modulator is controlled by the signal Modulation Control in order to induce a high current on COIL2 terminal when this signal is at logic "0". This will affect the magnetic field according to the data stored in the memory array.

Memory

The memory contains 128 bits laser programmed during manufacturing according to a customer list of codes. The bits are read serially in order to control the modulator. The 128 bits output sequence is repeated continuously until power goes off.

Memory Map

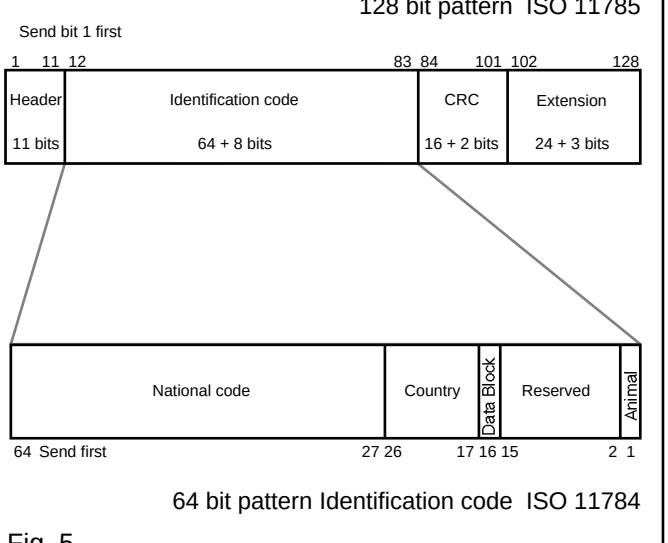


Fig. 5

Memory organisation
The structure of the 128 bits is as follows :

The **header** is sent first and is used to identify the start of the sequence. It is composed of 11 bits having a bit pattern which is unique in the data stream. **00000000001**

The header is followed by the **Identification code** which is composed of 64 bits organised in 8 blocks of 8 bits. Each block of 8 bits is trailed by a control bit set to logic "1" to prevent that the header is reproduced in the data. Bit 64 is transmitted first.
Bit 1 is a flag for animal "1" or non-animal "0" application.
Bits 2-15 are a reserved code for future use.
Bit 16 is a flag for additional data block "1" or no additional data block "0".
Bits 17-26 ISO 3166 Numeric country code
Bits 27-64 National identification code

The next two 8 bit blocks contain the **16 CRC-CCITT** error detection bits. LSB is transmitted first, and the 2 block are trailed with with a binary "1".

The data stream with 3 blocks of 8 bits trailed with a logical "1" representing the **extension bits**. The extension bits are planned for future extension in which for instance information from sensors or contents of trailing pages may be stored. In the current version the standard coding will be **000000001 000000001 000000001** and the flag bit 16 of the identification code "0".

Resonance Capacitor
The Resonance Capacitor is integrated, and its value is typically 75 pF.

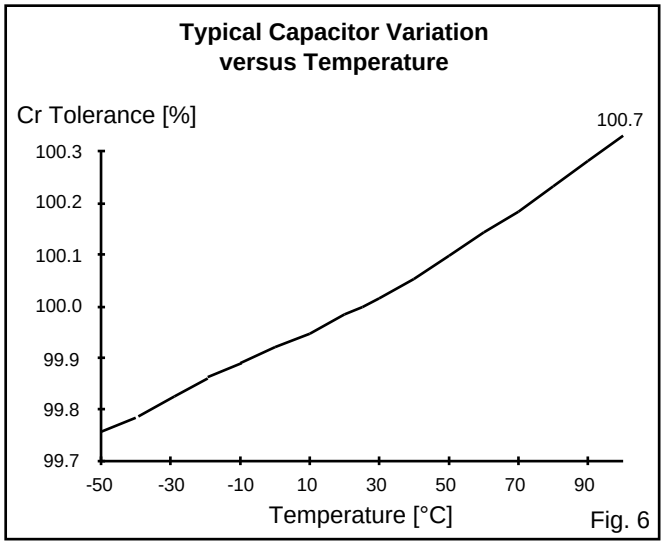


Fig. 6

Pad Description

Pad	Name	Function
1	COIL2	Coil Terminal 2 / Data output
2	COIL1	Coil Terminal 1 / Clock input
3	VDD	Positive Internal Supply Voltage
4	VSS	Negative Internal Supply Voltage

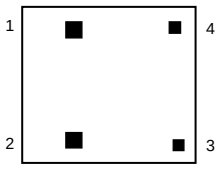
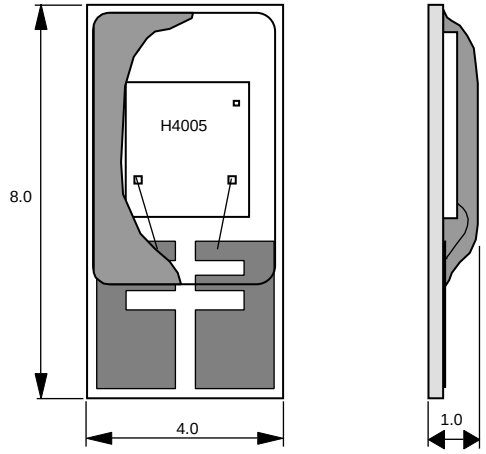


Table 5

Package and Ordering Information

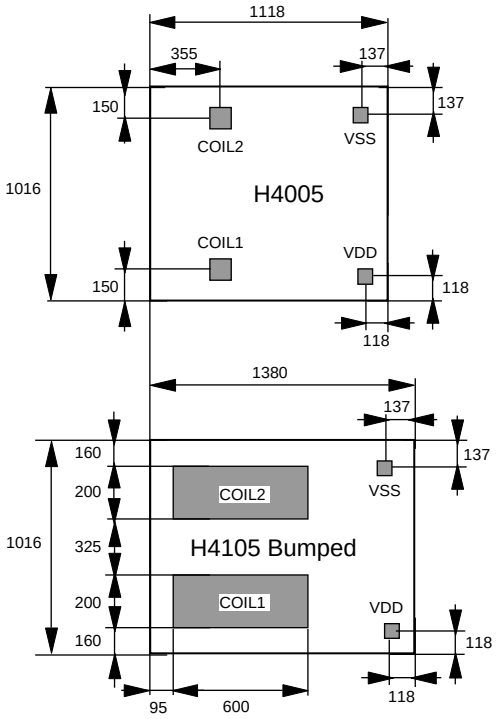
Dimensions of PCB version



Dimensions in [mm]

Fig. 7

CHIP Dimensions



IC Thickness : 280 µm ± 25 µm
Bump Height : 25 µm ± 5 µm

Dimensions in µm

Fig. 8

Ordering Information

The H4005 is available	in chip form without Bumps	H4005 IC
	in chip form with Bumps	H4105 Bumped IC
	PCB	H4005 COB