

1Gb DDR3 SDRAM

H5TQ1G43AFP(R)-xxC

H5TQ1G83AFP(R)-xxC

H5TQ1G63AFP(R)-xxC

**** Contents are subject to change at any time without notice.**

Revision History

Revision No.	History	Draft Date	Remark
0.01	Preliminary Initial Release	Nov. 2007	Preliminary
0.02	IDD Added	March 2008	Preliminary
0.1	Revision 0.1 specification Release	April 2008	
0.2	Added Halogen free products	April 2008	
0.3	Applied New IDD definition	Sep 2008	
0.4	Notation change of package outline	Jan 2009	

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1. DESCRIPTION

The H5TQ1G43AFP-xxC, H5TQ1G83AFP-xxC and H5TQ1G63AFP-xxC are a 1,073,741,824-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 1Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it.

The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

1.1 Device Features and Ordering Information

1.1.1 FEATURES

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, $\overline{\text{CK}}$) operation
- Differential Data Strobe (DQS, $\overline{\text{DQS}}$)
- On chip DLL align DQ, DQS and $\overline{\text{DQS}}$ transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 6, 7, 8, 9, and (10) supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- 8K refresh cycles /64ms
- JEDEC standard 78ball FBGA(x4/x8), 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- Auto Self Refresh supported
- On Die Thermal Sensor supported
- 8 bit pre-fetch

1.1.2 ORDERING INFORMATION

Part No.	Configuration	Package
H5TQ1G43AFP*(R)-**xxC	256M x 4	78ball FBGA
H5TQ1G83AFP*(R)-**xxC	128M x 8	
H5TQ1G63AFP*(R)-**xxC	64M x 16	96ball FBGA

* (R) means Halogen Free Products

** XX means Speed Bin Grade

1.1.3 OPERATING FREQUENCY

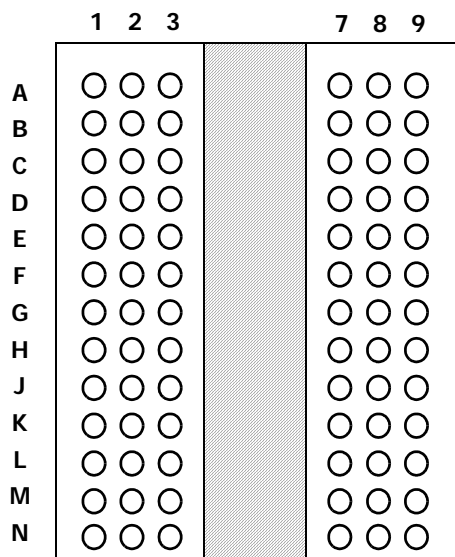
Grade	Frequency [MHz]						Remark (CL-tRCD-tRP)
	CL5	CL6	CL7	CL8	CL9	CL10	
-S6		0					DDR3-800 6-6-6
-G7		0	0	0	0		DDR3-1066 7-7-7
-H9		0	0	0	0	0	DDR3-1333 9-9-9

1.2 Package Ballout/Mechanical Dimension

1.2.1 x4 Package Ball out (Top view): 78ball FBGA Package (no support balls)

	1	2	3	4	5	6	7	8	9	
A	VSS	VDD	NC				NC	VSS	VDD	A
B	VSS	VSSQ	DQ0				DM	VSSQ	VDDQ	B
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	C
D	VSSQ	NC	$\overline{\text{DQS}}$				VDD	VSS	VSSQ	D
E	VREFDQ	VDDQ	NC				NC	NC	VDDQ	E
F	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	F
G	ODT	VDD	$\overline{\text{CAS}}$				CK	VDD	CKE	G
H	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	H
J	VSS	BA0	BA2				A15	VREFCA	VSS	J
K	VDD	A3	A0				A12/BC	BA1	VDD	K
L	VSS	A5	A2				A1	A4	VSS	L
M	VDD	A7	A9				A11	A6	VDD	M
N	VSS	$\overline{\text{RESET}}$	A13				NC	A8	VSS	N
	1	2	3	4	5	6	7	8	9	

Note: Green NC balls indicate mechanical support balls with no internal connection



(Top View: See the balls through the Package)

- Populated ball
- ⊕ Ball not populated

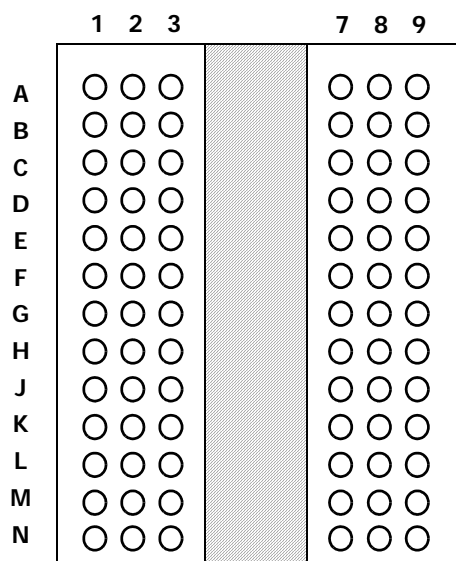
1.2 Package Ballout/Mechanical Dimension

1.2.2 x8 Package Ball out (Top view): 78ball FBGA Package (no support balls)

	1	2	3	4	5	6	7	8	9	
A	VSS	VDD	NC				NU/TDQS	VSS	VDD	A
B	VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	B
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	C
D	VSSQ	DQ6	DQS				VDD	VSS	VSSQ	D
E	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	E
F	NC	VSS	RAS				CK	VSS	NC	F
G	ODT	VDD	CAS				CK	VDD	CKE	G
H	NC	CS	WE				A10/AP	ZQ	NC	H
J	VSS	BA0	BA2				NC	VREFCA	VSS	J
K	VDD	A3	A0				A12/BC	BA1	VDD	K
L	VSS	A5	A2				A1	A4	VSS	L
M	VDD	A7	A9				A11	A6	VDD	M
N	VSS	RESET	A13				NC	A8	VSS	N

1	2	3	4	5	6	7	8	9
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Note: Green NC balls indicate mechanical support balls with no internal connection



(Top View: See the balls through the Package)

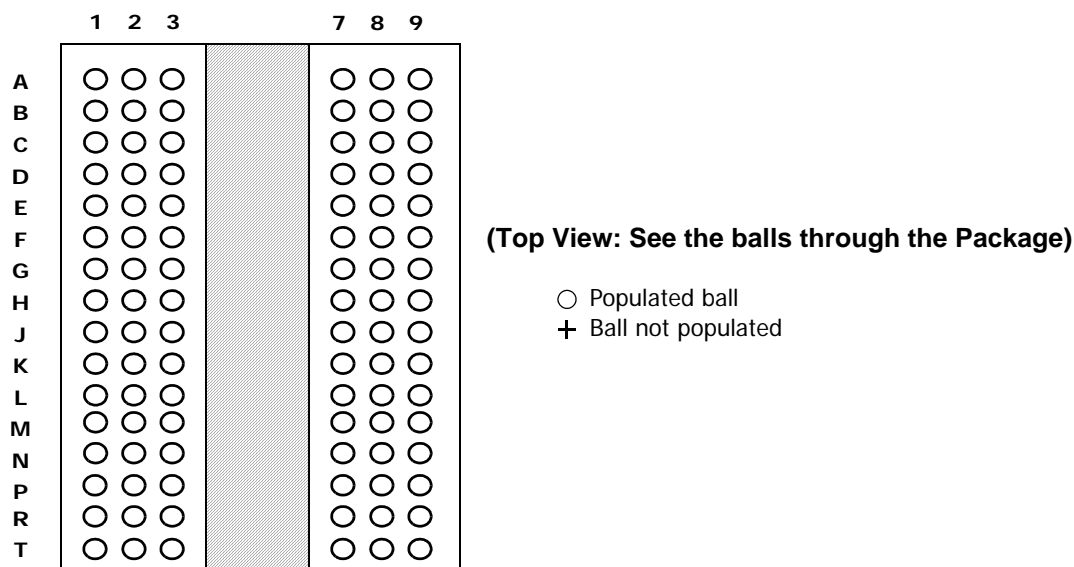
- Populated ball
- + Ball not populated

1.2 Package Ballout/Mechanical Dimension

1.2.3 x16 Package Ball out (Top view): 96ball FBGA Package (no support balls)

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				$\overline{\text{DQS}}\text{U}$	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	$\overline{\text{DQSL}}$				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	$\overline{\text{DQSL}}$				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	J
K	ODT	VDD	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	VDD	CKE	K
L	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				A15	VREFCA	VSS	M
N	VDD	A3	A0				A12/ $\overline{\text{BC}}$	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	$\overline{\text{RESET}}$	A13				NC	A8	VSS	T
	1	2	3	4	5	6	7	8	9	

Note: Green NC balls indicate mechanical support balls with no internal connection



1.3 ROW AND COLUMN ADDRESS TABLE

1Gb

Configuration	256Mb x 4	128Mb x 8	64Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC	A12/BC	A12/BC
Row Address	A0 - A13	A0 - A13	A0 - A12
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size ¹	1 KB	1 KB	2 KB

2Gb

Configuration	512Mb x 4	256Mb x 8	128Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC	A12/BC	A12/BC
Row Address	A0 - A14	A0 - A14	A0 - A13
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size ¹	1 KB	1 KB	2 KB

4Gb

Configuration	1Gb x 4	512Mb x 8	256Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC	A12/BC	A12/BC
Row Address	A0 - A15	A0 - A15	A0 - A14
Column Address	A0 - A9,A11	A0 - A9	A0 - A9
Page size ¹	1 KB	1 KB	2 KB

8Gb

Configuration	2Gb x 4	1Gb x 8	512Mb x 16
# of Banks	8	8	8
Bank Address	BA0 - BA2	BA0 - BA2	BA0 - BA2
Auto precharge	A10/AP	A10/AP	A10/AP
BL switch on the fly	A12/BC	A12/BC	A12/BC
Row Address	A0 - A15	A0 - A15	A0 - A15
Column Address	A0 - A9, A11, A13	A0 - A9, A11	A0 - A9
Page size ¹	2 KB	2 KB	2 KB

Note1: Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

$$\text{page size} = 2^{\text{COLBITS}} * \text{ORG} \div 8$$

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

1.4 Pin Functional Description

Symbol	Type	Function
CK, $\overline{\text{CK}}$	Input	Clock: CK and $\overline{\text{CK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{\text{CK}}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{\text{CK}}$, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{\text{CS}}$	Input	Chip Select: All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external Rank selection on systems with multiple Ranks. $\overline{\text{CS}}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{\text{DQS}}$ and DM/TDQS, NU/ $\overline{\text{TDQS}}$ (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$, DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Command Inputs: $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/ $\overline{\text{TDQS}}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/ $\overline{\text{BC}}$ have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{\text{BC}}$	Input	Burst Chop: A12 / $\overline{\text{BC}}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD} , i.e. 1.20V for DC high and 0.30V for DC low.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, $\overline{\text{DQL}}$, DQS, $\overline{\text{DQS}}$, DQSU, $\overline{\text{DQSU}}$, DQSL, $\overline{\text{DQSL}}$	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS, DQSL, and DQSU are paired with differential signals $\overline{\text{DQS}}$, $\overline{\text{DQSL}}$, and $\overline{\text{DQSU}}$, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, $\overline{\text{TDQS}}$	Output	Termination Data Strobe: TDQS/ $\overline{\text{TDQS}}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/ $\overline{\text{TDQS}}$ that is applied to DQS/ $\overline{\text{DQS}}$. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and $\overline{\text{TDQS}}$ is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
V _{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V _{SSQ}	Supply	DQ Ground
V _{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V _{SS}	Supply	Ground
V _{REFDQ}	Supply	Reference voltage for DQ
V _{REFCA}	Supply	Reference voltage
ZQ	Supply	Reference Pin for ZQ calibration

Note:

Input only pins (BA0-BA2, A0-A15, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$, CKE, ODT, DM, and $\overline{\text{RESET}}$) do not supply termination.

2. Command Description

2.1 Command Truth Table

(a) note 1,2,3,4 apply to the entire Command Truth Table

(b) Note 5 applies to all Read/Write command

[BA = Bank Address, RA = Rank Address, CA = Column Address, \overline{BC} = Burst Chop, X = Don't Care, V = Valid]

Function	Abbreviation	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0-BA3	A13-A15	A12-BC	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7,8,9,12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS ₄	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS ₈	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						

Function	Abbreviation	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0-BA3	A13-A15	A12-BC	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. All DDR3 SDRAM commands are defined by states of $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. $\overline{\text{RESET}}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

2.2 CKE Truth Table

- a) Notes 1-7 apply to the entire CKE Truth Table.
b) CKE low is allowed only if tMRD and tMOD are satisfied.

Current State ²	CKE		Command (N) ³ RAS, CAS, WE, CS	Action (N) ³	Notes
	Previous Cycle ¹ (N-1)	Current Cycle ¹ (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9,13,18
For more details with all signals See "2.1 Command Truth Table" on page 12..					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. tCKEmin of [TBD] clocks means CKE must be registered on [TBD] consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the [TBD] clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + [TBD] + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions see 8.1 on page 41.
14. The Power-Down does not perform any refresh operations.
15. "X" means "don't care" (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc.).

3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VIN, VOUT	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	
TSTG	Storage Temperature	-55 to +100		, 2

Notes:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

4. Operating Conditions

4.1 OPERATING TEMPERATURE CONDITION

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature (Tcase)	0 to 85	°C	2
	Extended Temperature Range	85 to 95	°C	1,3

Notes:

- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
For measurement conditions, please refer to the JEDEC document JESD51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported.
During operation, the DRAM case temperature must be maintained between 0 - 85°C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μ s.
(This double refresh requirement may not apply for some devices.) It is also possible to specify a component with 1X refresh (tREFI to 7.8 μ s) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

4.2 RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

- Under all conditions, VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

5. AC and DC Input Measurement Levels

5.1 AC and DC Logic Input Levels for Single-Ended Signals

Single Ended AC and DC Input Levels

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333		Unit	Notes
		Min	Max		
VIH(DC)	DC input logic high	$V_{ref} + 0.100$	TBD	V	1
VIL(DC)	DC input logic low	TBD	$V_{ref} - 0.100$	V	1
VIH(AC)	AC input logic high	$V_{ref} + 0.175$	-	V	1, 2
VIL(AC)	AC input logic low		$V_{ref} - 0.175$	V	1, 2
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	$0.49 * VDD$	$0.51 * VDD$	V	3, 4
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	$0.49 * VDD$	$0.51 * VDD$	V	3, 4
VTT	Termination voltage for DQ, DQS outputs	$VDDQ/2 - TBD$	$VDDQ/2 + TBD$		

Notes:

1. For DQ and DM, $V_{ref} = V_{RefDQ}$. For input any pins except \overline{RESET} , $V_{ref} = V_{RefCA}$.
2. The "t.b.d." entries might change based on overshoot and undershoot specification.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{Ref(DC)}$ by more than $\pm 1\% VDD$ (for reference: approx. ± 15 mV).
4. For reference: approx. $VDD/2 \pm 15$ mV.

The dc-tolerance limits and ac-noise limits for the reference voltages V_{RefCA} and V_{RefDQ} are illustrated in below Figure. It shows a valid reference voltage $V_{Ref}(t)$ as a function of time. (V_{Ref} stands for V_{RefCA} and V_{RefDQ} likewise).

$V_{Ref}(DC)$ is the linear average of $V_{Ref}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table.

Furthermore $V_{Ref}(t)$ may temporarily deviate from $V_{Ref}(DC)$ by no more than $\pm 1\% VDD$.

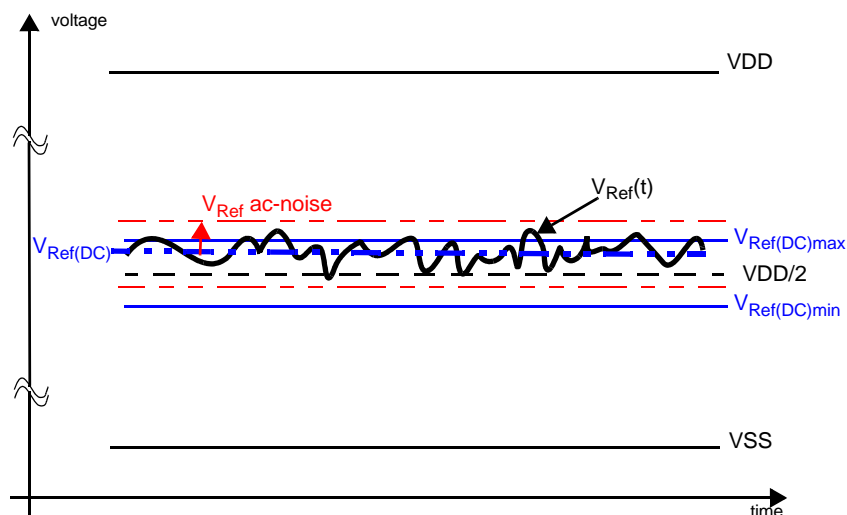


Illustration of $V_{ref}(DC)$ tolerance and V_{ref} ac-noise limits

5.2 AC and DC Logic Input Levels for Differential Signals

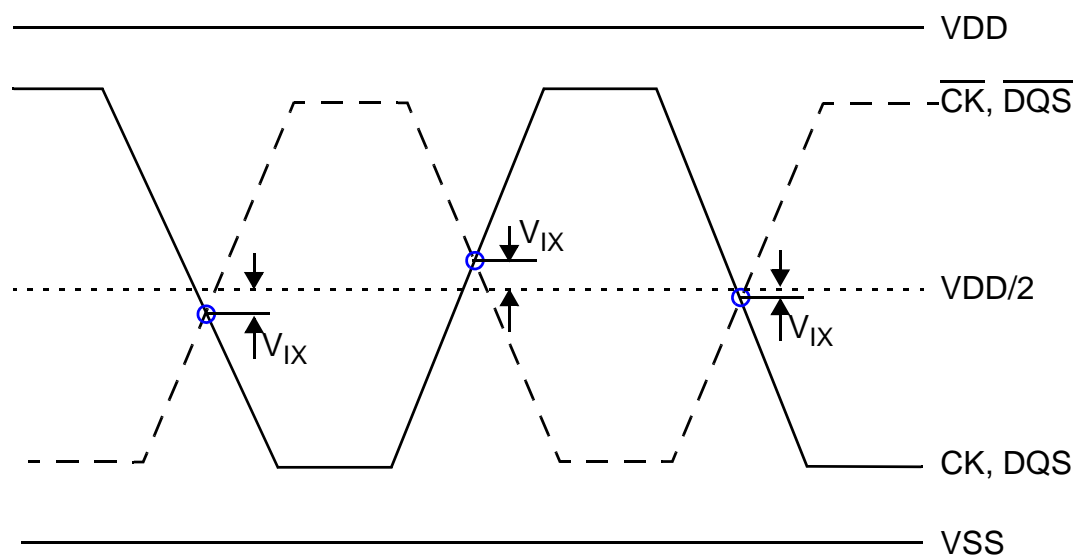
Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333		Unit	Notes
		Min	Max		
VIHdiff	Differential input logic high	+ 0.200	-	V	1
VILdiff	Differential input logic low		- 0.200	V	1

Note1.

Refer to "Overshoot and Undershoot Specification on page 25"

5.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) must meet the requirements below table. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333		Unit	Notes
		Min	Max		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$	- 150	150	mV	

5.4 Slew Rate Definitions for Single Ended Input Signals

5.4.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vref and the first crossing of VIH (AC) min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vref and the first crossing of VIL (AC) max.

5.4.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (DC) max and the first crossing of Vref. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH (DC) min and the first crossing of Vref.

Single-Ended Input Slew Rate Definition

Description	Measured		Defined by	Applicable for
	Min	Max		
Input slew rate for rising edge	Vref	VIH (AC) min	$\frac{VIH (AC) \text{ min} - Vref}{\Delta TRS}$	Setup (tIS, tDS)
Input slew rate for falling edge	Vref	VIL (AC) max	$\frac{Vref - VIL (AC) \text{ max}}{\Delta TFS}$	
Input slew rate for rising edge	VIL (DC) max	Vref	$\frac{Vref - VIL (DC) \text{ max}}{\Delta TFH}$	Hold (tIH, tDH)
Input slew rate for falling edge	VIH (DC) min	Vref	$\frac{VIH (DC) \text{ min} - Vref}{\Delta TRH}$	

Input Nominal Slew Rate Definition for Single-Ended Signals

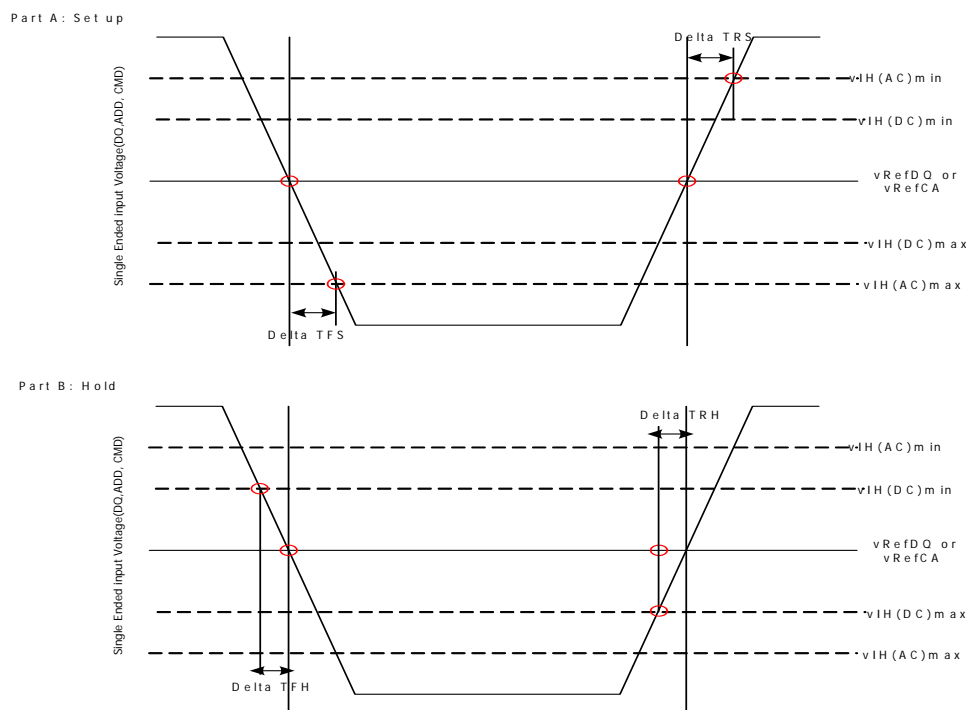


Figure 82 ? Input Nominal Slew Rate Definition for Single-Ended Signals

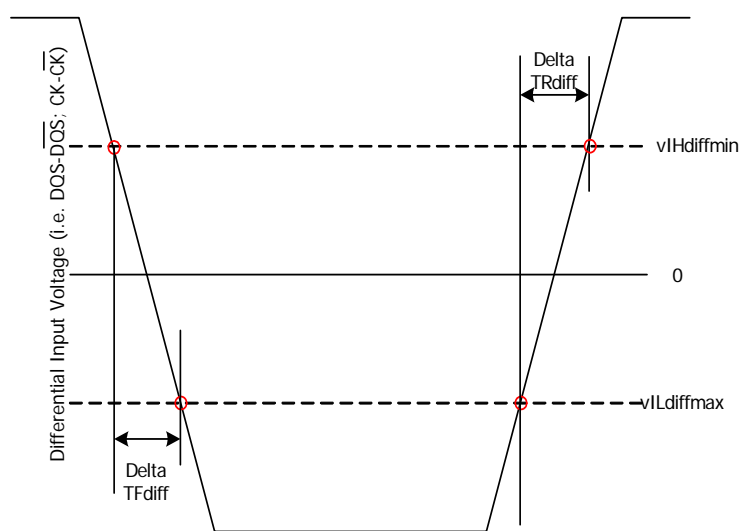
5.5 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{\text{CK}}$ and DQS, $\overline{\text{DQS}}$) are defined and measured as shown in Table and Figure .

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	VILdiffmax	VIHdiffmin	$\frac{\text{VIHdiffmin} - \text{VILdiffmax}}{\Delta \text{TRdiff}}$
Differential input slew rate for falling edge (CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$)	VIHdiffmin	VILdiffmax	$\frac{\text{VIHdiffmin} - \text{VILdiffmax}}{\Delta \text{TFdiff}}$

Note:

The differential signal (i.e. CK- $\overline{\text{CK}}$ and DQS- $\overline{\text{DQS}}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

6. AC and DC Output Measurement Levels

6.1 Single Ended AC and DC Output Levels

Table shows the output levels used for measurements of single ended signals.

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	$0.8 \times V_{DDQ}$	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	$0.5 \times V_{DDQ}$	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	$0.2 \times V_{DDQ}$	V	
VOH(AC)	AC output high measurement level (for output SR)	$V_{TT} + 0.1 \times V_{DDQ}$	V	1
VOL(AC)	AC output low measurement level (for output SR)	$V_{TT} - 0.1 \times V_{DDQ}$	V	1

1. The swing of $\pm 0.1 \times V_{DDQ}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ} / 2$.

6.1.1 Differential AC and DC Output Levels

Below table shows the output levels used for measurements of differential signals.

Symbol	Parameter	DDR3-800, 1066, 1333	Unit	Notes
VOHdiff (AC)	AC differential output high measurement level (for output SR)	$+ 0.2 \times V_{DDQ}$	V	1
VOLdiff (AC)	AC differential output low measurement level (for output SR)	$- 0.2 \times V_{DDQ}$	V	1

1. The swing of $\pm 0.2 \times V_{DDQ}$ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs.

6.2 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table and Figure.

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{\Delta t_{Rse}}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{\Delta t_{Fse}}$

Note:

Output slew rate is verified by design and characterisation, and may not be subject to production test.

Fig. Single Ended Output Slew Rate Definition

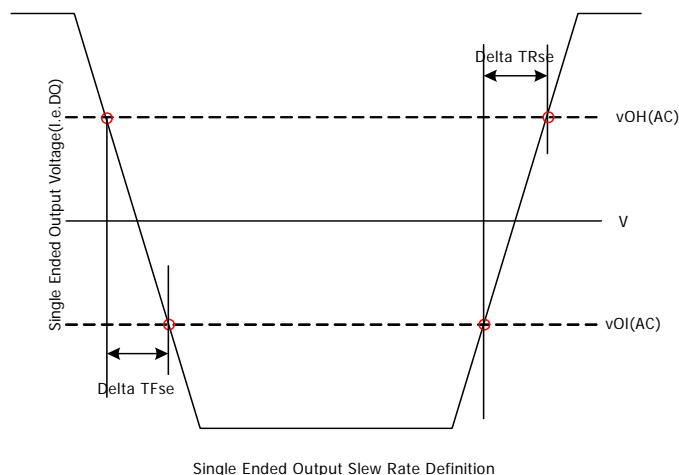


Table. Output Slew Rate (single-ended)

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Single-ended Output Slew Rate	SRQse	2.5	5	2.5	5	2.5	5	V/ns

*** For Ron = RZQ/7 setting

6.3 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff (AC) and VOHdiff (AC) for differential signals as shown in Table and Figure .

Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff (AC)	VOHdiff (AC)	VOHdiff (AC)-VOLdiff (AC) DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff (AC)	VOLdiff (AC)	VOHdiff (AC)-VOLdiff (AC) DeltaTFdiff

Note:

Output slew rate is verified by design and characterization, and may not be subject to production test.

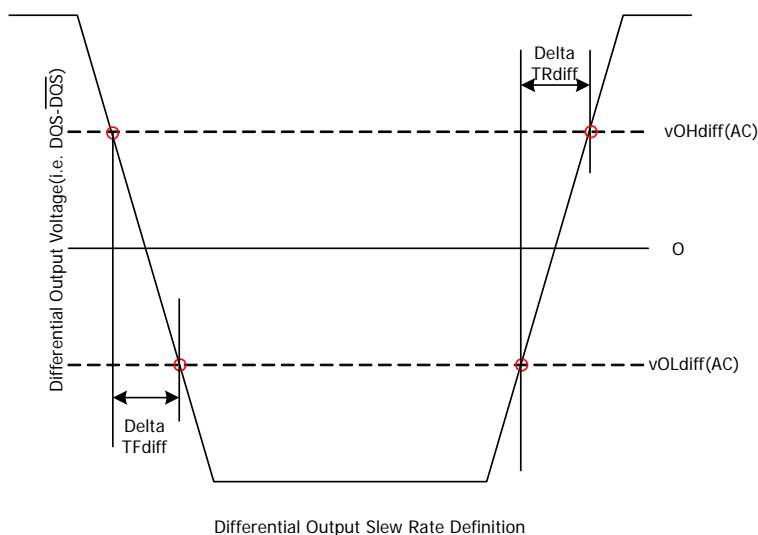


Fig. Differential Output Slew Rate Definition

Table. Differential Output Slew Rate

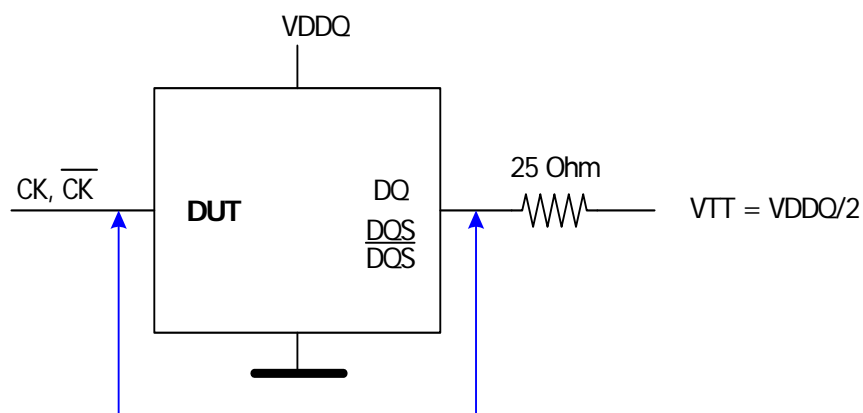
Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units
		Min	Max	Min	Max	Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	V/ns

***For Ron = RZQ/7 setting

6.4 Reference Load for AC Timing and Output Slew Rate

Figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



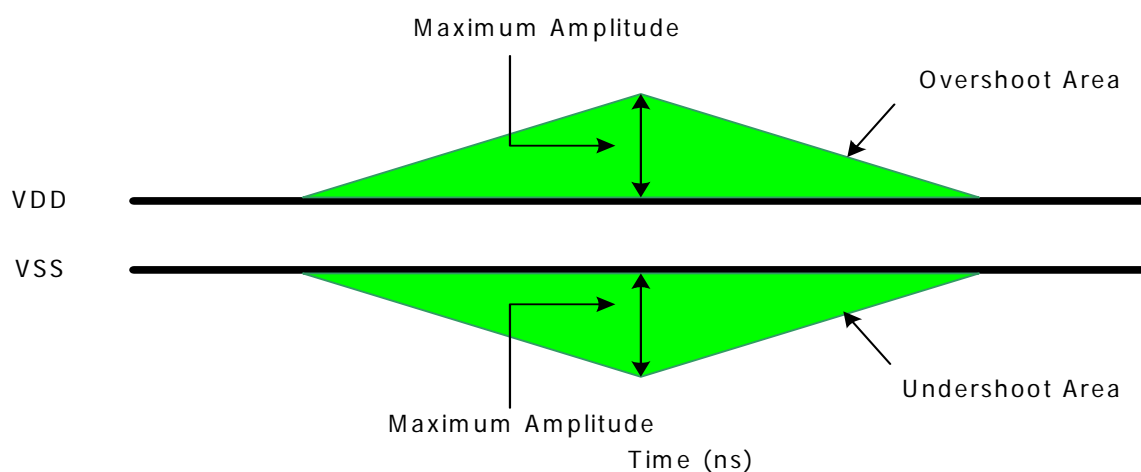
Reference Load for AC Timing and Output Slew Rate

7. Overshoot and Undershoot Specifications

7.1 Address and Control Overshoot and Undershoot Specifications

Table. AC Overshoot/Undershoot Specification for Address and Control Pins

Description	Specification		
	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns
Maximum undershoot area below VSS (See Figure)	0.67 V-ns	0.5 V-ns	0.4 V-ns

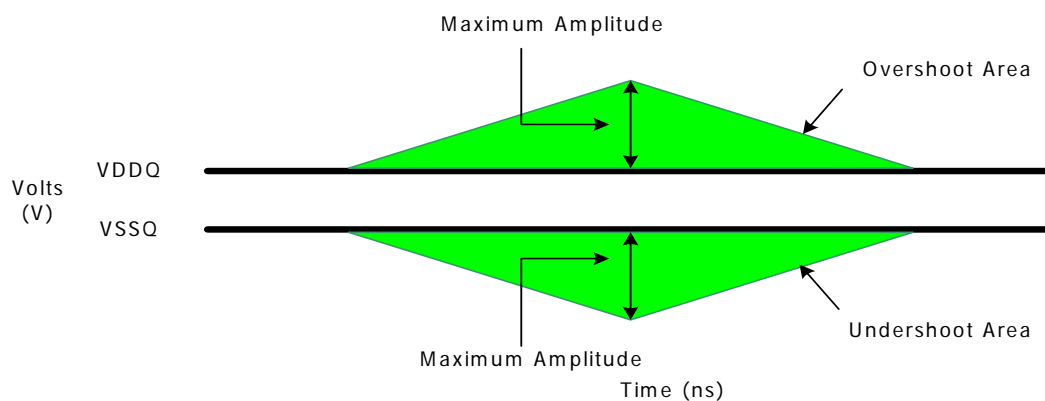


Address and Control Overshoot and Undershoot Definition

7.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

Table. AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

Description	Specification		
	DDR3-800	DDR3-1066	DDR3-1333
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns
Maximum undershoot area below VSSQ (See Figure)	0.25 V-ns	0.19 V-ns	0.15 V-ns



Clock, Data Strobe and Mask Overshoot and Undershoot Definition

7.3 34 ohm Output Driver DC Electrical Characteristics

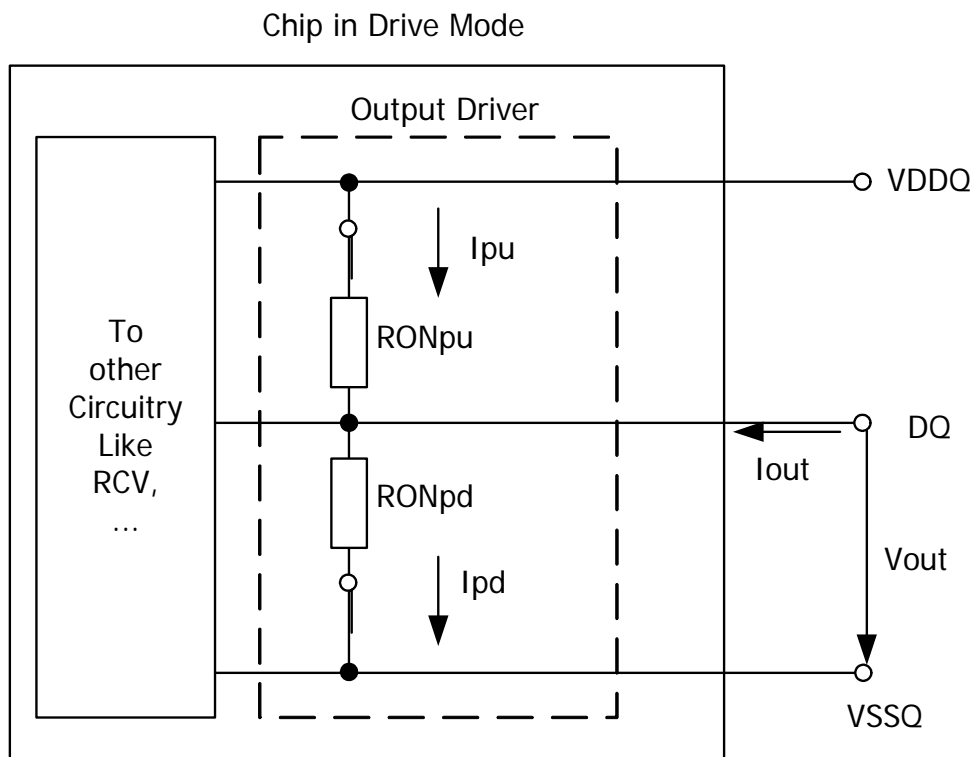
A functional representation of the output buffer is shown in Figure . Output driver impedance R_{ON} is defined by the value of the external reference resistor R_{ZQ} as follows:

$R_{ON34} = R_{ZQ} / 7$ (nominal 34.3 $\Omega \pm 10\%$ with nominal $R_{ZQ} = 240 \Omega \pm 1\%$)

The individual pull-up and pull-down resistors (R_{ONPu} and R_{ONPd}) are defined as follows:

$$R_{ONPu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|} \quad \text{under the condition that } R_{ONPd} \text{ is turned off}$$

$$R_{ONPd} = \frac{V_{Out}}{|I_{Out}|} \quad \text{under the condition that } R_{ONPu} \text{ is turned off}$$



Output Driver DC Electrical Characteristics, assuming $R_{ZQ} = 240 \Omega$;
entire operating temperature range; after proper ZQ calibration

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.6	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.9	1.0	1.4	$R_{ZQ}/7$	1, 2, 3
	RON_{34Pu}	$V_{OLdc} = 0.2 \times V_{DDQ}$	0.9	1.0	1.4	$R_{ZQ}/7$	1, 2, 3
		$V_{OMdc} = 0.5 \times V_{DDQ}$	0.9	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
		$V_{OHdc} = 0.8 \times V_{DDQ}$	0.6	1.0	1.1	$R_{ZQ}/7$	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} $0.5 \times V_{DDQ}$	-10		+10	%	1, 2, 4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
3. Pull-down and pull-up output driver impedances are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$.
4. Measurement definition for mismatch between pull-up and pull-down, MM_{PuPd} :
Measure RON_{Pu} and RON_{Pd} , both at $0.5 \times V_{DDQ}$:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} \times 100$$

7.4 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table and Table .

$DT = T - T (@calibration)$; $DV = V_{DDQ} - V_{DDQ} (@calibration)$; $V_{DD} = V_{DDQ}$

$dRONdT$ and $dRONdV$ are not subject to production test but are verified by design and characterization.

Output Driver Sensitivity Definition

	min	max	unit
$RON_{PU} @ V_{OHdc}$	$0.6 - dRONdTH^* \Delta T - dRONdVH^* \Delta V $	$1.1 + dRONdTH^* \Delta T + dRONdVH^* \Delta V $	$R_{ZQ}/7$
$RON @ V_{OMdc}$	$0.9 - dRONdTM^* \Delta T - dRONdVM^* \Delta V $	$1.1 + dRONdTM^* \Delta T + dRONdVM^* \Delta V $	$R_{ZQ}/7$
$RON_{PD} @ V_{OLdc}$	$0.6 - dRONdTL^* \Delta T - dRONdVL^* \Delta V $	$1.1 + dRONdTL^* \Delta T + dRONdVL^* \Delta V $	$R_{ZQ}/7$

Output Driver Voltage and Temperature Sensitivity

	min	max	unit
$dRONdTM$	0	1.5	%/ $^{\circ}C$
$dRONdVM$	0	0.15	%/mV
$dRONdTL$	0	1.5	%/ $^{\circ}C$
$dRONdVL$	0	TBD	%/mV

Output Driver Voltage and Temperature Sensitivity

	min	max	unit
dR _{ONdTH}	0	1.5	%/°C
dR _{ONdVH}	0	TBD	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

7.5 On-Die Termination (ODT) Levels and I-V Characteristics

7.5.1 On-Die Termination (ODT) Levels and I-V Characteristics

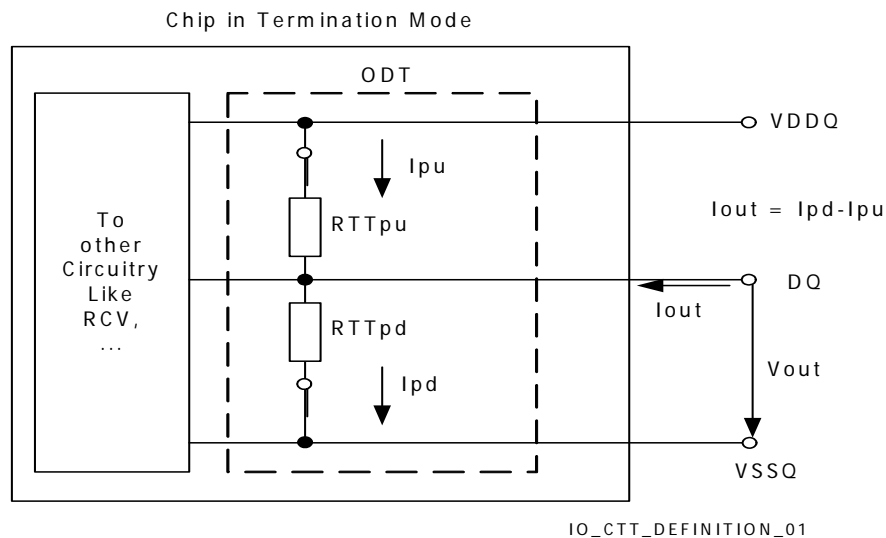
On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.

ODT is applied to the DQ, DM, DQS/ \overline{DQS} and TDQS/ \overline{TDQS} (x8 devices only) pins.

A functional representation of the on-die termination is shown in Figure . The individual pull-up and pull-down resistors ($RTTPu$ and $RTTPd$) are defined as follows:

$$RTT_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|} \quad \text{under the condition that } RTTPd \text{ is turned off}$$

$$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|} \quad \text{under the condition that } RTTPu \text{ is turned off}$$



On-Die Termination : Definition of Voltages and Currents

7.5.2 ODT DC Electrical Characteristics

A below table provides an overview of the ODT DC electrical characteristics. The values for RTT60Pd120, RTT60Pu120, RTT120Pd240, RTT120Pu240, RTT40Pd80, RTT40Pu80, RTT30Pd60, RTT30Pu60, RTT20Pd40, RTT20Pu40 are not specification requirements, but can be used as design guide lines:

ODT DC Electrical Characteristics, assuming $R_{ZQ} = 240 \Omega \pm 1\%$ entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	RTT	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 0	120 Ω	RTT _{120Pd240}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	R_{ZQ}	1) 2) 3) 4)
		RTT _{120Pu240}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	R_{ZQ}	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
		RTT ₁₂₀	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/2$	1) 2) 5)
0, 0, 1	60 Ω	RTT _{60Pd120}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/2$	1) 2) 3) 4)
		RTT _{60Pu120}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/2$	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
		RTT ₆₀	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/4$	1) 2) 5)

ODT DC Electrical Characteristics, assuming $R_{ZQ} = 240 \Omega \pm 1\%$ entire operating temperature range;
after proper ZQ calibration

MR1 A9, A6, A2	RTT	Resistor	V _{Out}	min	nom	max	Unit	Notes
0, 1, 1	40 Ω	RTT _{40Pd80}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	R _{ZQ} /3	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R _{ZQ} /3	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	R _{ZQ} /3	1) 2) 3) 4)
		RTT _{40Pu80}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	R _{ZQ} /3	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R _{ZQ} /3	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	R _{ZQ} /3	1) 2) 3) 4)
		RTT ₄₀	V _{IL(ac)} to V _{IH(ac)}	0.9	1.00	1.6	R _{ZQ} /6	1) 2) 5)
1, 0, 1	30 Ω	RTT _{30Pd60}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	R _{ZQ} /4	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R _{ZQ} /4	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	R _{ZQ} /4	1) 2) 3) 4)
		RTT _{30Pu60}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	R _{ZQ} /4	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R _{ZQ} /4	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	R _{ZQ} /4	1) 2) 3) 4)
		RTT ₃₀	V _{IL(ac)} to V _{IH(ac)}	0.9	1.00	1.6	R _{ZQ} /8	1) 2) 5)
1, 0, 0	20 Ω	RTT _{20Pd40}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	R _{ZQ} /6	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R _{ZQ} /6	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	R _{ZQ} /6	1) 2) 3) 4)
		RTT _{20Pu40}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	R _{ZQ} /6	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R _{ZQ} /6	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	R _{ZQ} /6	1) 2) 3) 4)
		RTT ₂₀	V _{IL(ac)} to V _{IH(ac)}	0.9	1.00	1.6	R _{ZQ} /12	1) 2) 5)
Deviation of V _M w.r.t. V _{DDQ} /2, D V _M				-5		+5	%	1) 2) 5) 6)

The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.

Pull-down and pull-up ODT resistors are recommended to be calibrated at $0.5 \times V_{DDQ}$. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at $0.2 \times V_{DDQ}$ and $0.8 \times V_{DDQ}$.

Not a specification requirement, but a design guide line.

Measurement definition for RTT:

Apply $V_{IH}(ac)$ to pin under test and measure current $I(V_{IH}(ac))$, then apply $V_{IL}(ac)$ to pin under test and measure current $I(V_{IL}(ac))$ respectively.

$$R_{TT} = \frac{V_{IH}(ac) - V_{IL}(ac)}{I(V_{IH}(ac)) - I(V_{IL}(ac))}$$

Measurement definition for VM and DVM:

Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \cdot V_M}{V_{DDQ}} - 1 \right) \cdot 100$$

7.5.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table and Table .

$DT = T - T (@calibration)$; $DV = V_{DDQ} - V_{DDQ} (@calibration)$; $VDD = V_{DDQ}$

ODT Sensitivity Definition

	min	max	unit
R_{TT}	$0.9 - dR_{TT}dT* \Delta T - dR_{TT}dV* \Delta V $	$1.6 + dR_{TT}dT* \Delta T + dR_{TT}dV* \Delta V $	RZQ/2,4,6,8,12

ODT Voltage and Temperature Sensitivity

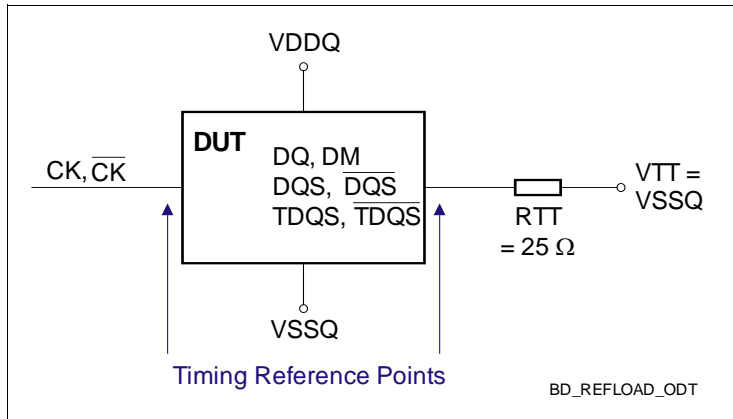
	min	max	unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

These parameters may not be subject to production test. They are verified by design and characterization

7.6 ODT Timing Definitions

7.6.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure .



7.6.2 ODT Timing Reference Load

ODT Timing Definitions

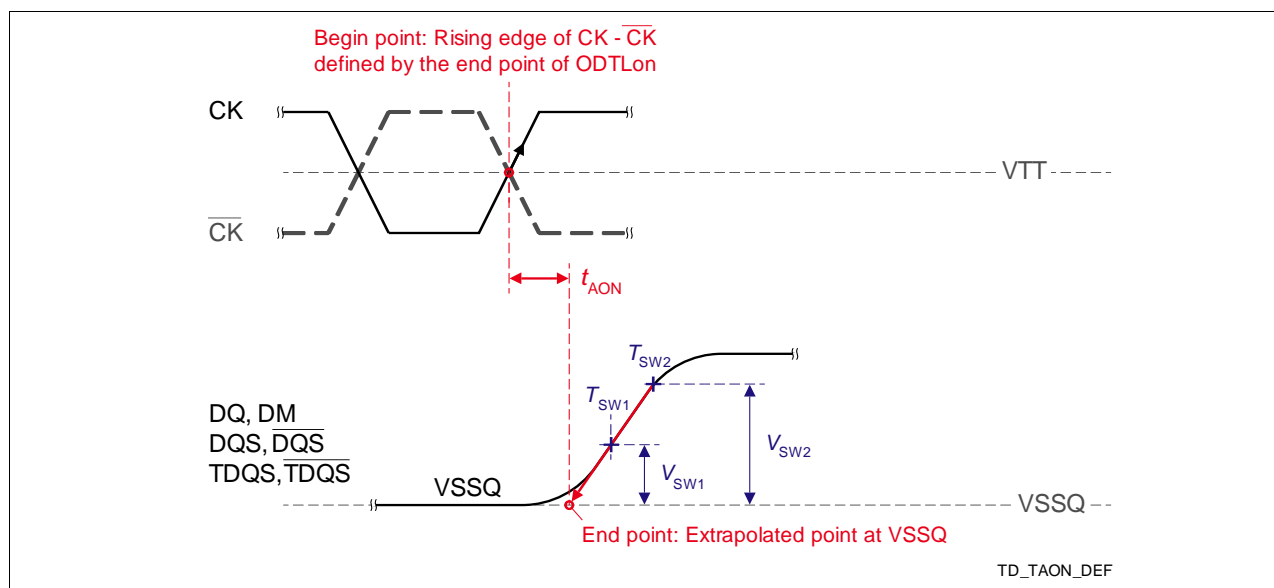
Definitions for t_{AON} , t_{AONPD} , t_{AOF} , t_{AOFPD} and t_{ADC} are provided in the table and subsequent figures. Measurement reference settings are provided in the table.

ODT Timing Definitions

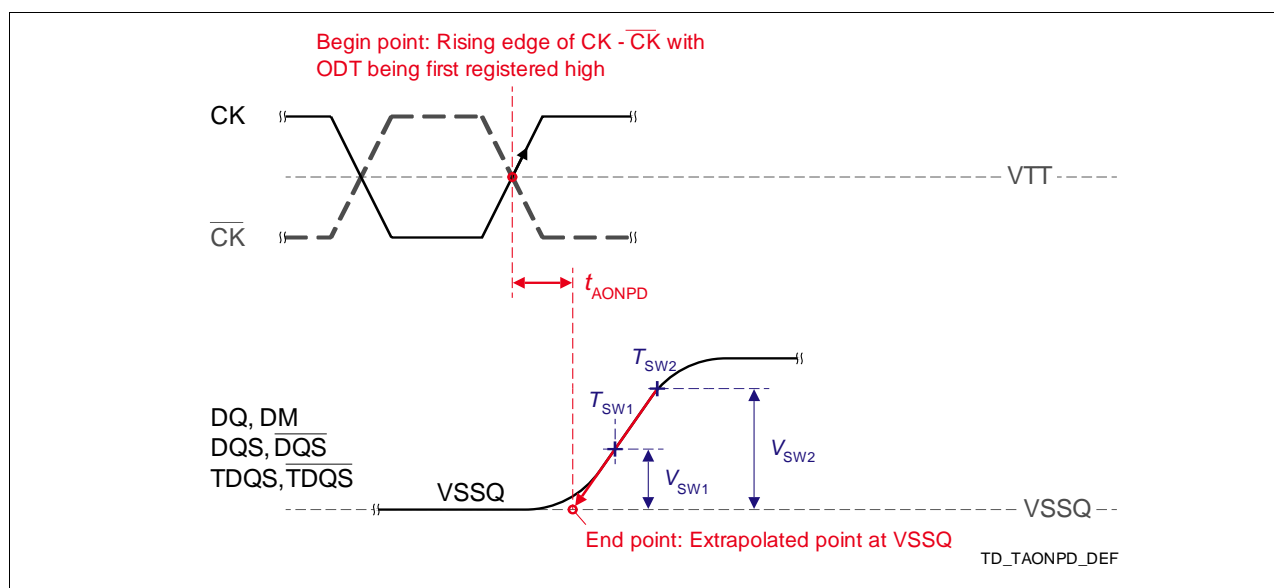
Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK - \overline{CK} defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure
t_{AONPD}	Rising edge of CK - \overline{CK} with ODT being first registered high	Extrapolated point at VSSQ	Figure
t_{AOF}	Rising edge of CK - \overline{CK} defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure
t_{AOFPD}	Rising edge of CK - \overline{CK} with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure
t_{ADC}	Rising edge of CK - \overline{CK} defined by the end point of ODTLcwn, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure

Reference Settings for ODT Timing Measurements

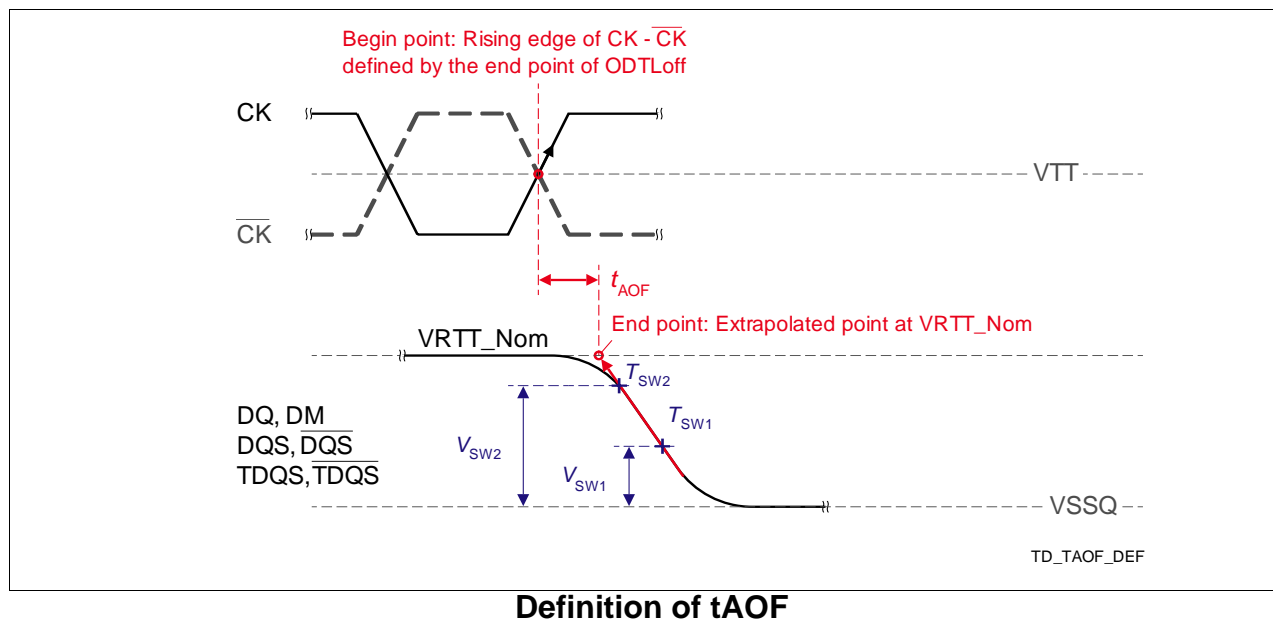
Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1} [V]	V_{SW2} [V]	Note
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{ADC}	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30	



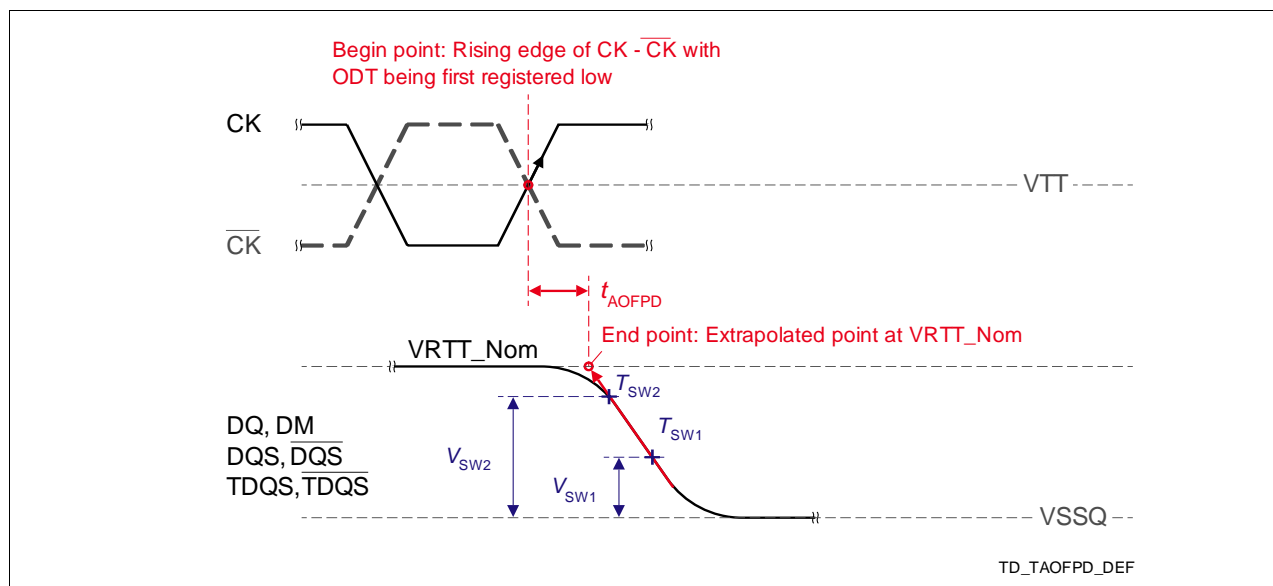
Definition of t_{AON}



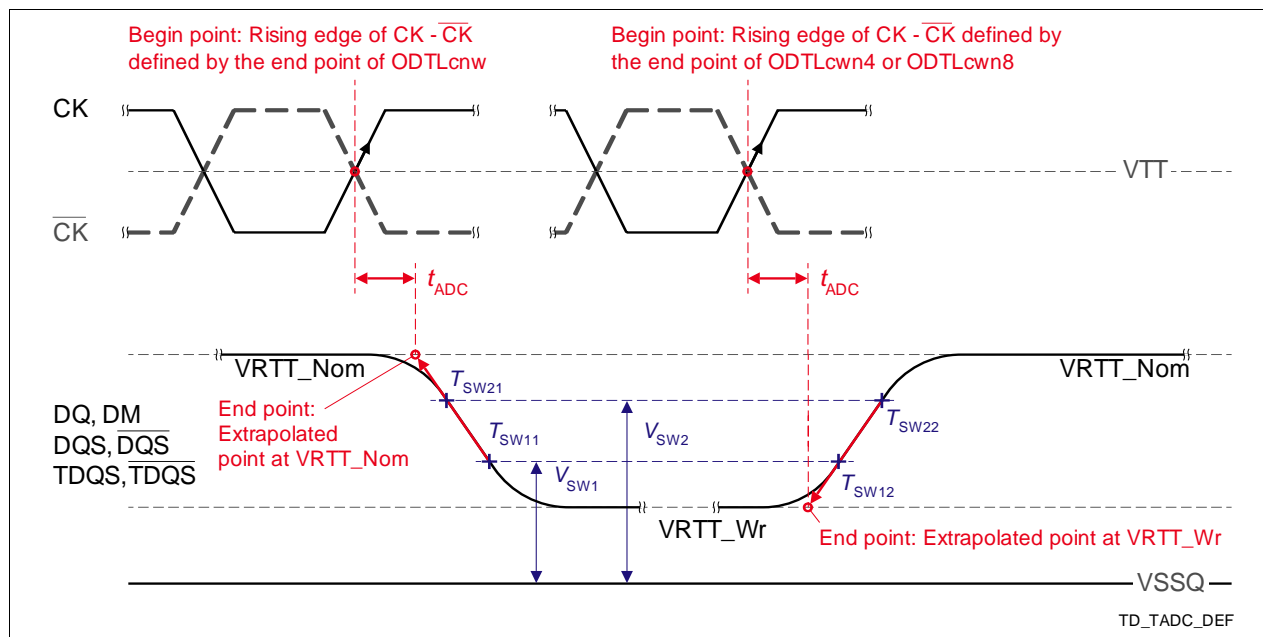
Definition of t_{AONPD}



Definition of tAOF



Definition of tAOFPD



Definition of t_{ADC}

8. IDD and IDDQ Specification Parameters and Test Conditions

8.1 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- "0" and "LOW" is defined as $V_{IN} \leq V_{ILAC(max)}$.
- "1" and "HIGH" is defined as $V_{IN} \geq V_{IHAC(max)}$.
- "FLOATING" is defined as inputs are $V_{REF} - V_{DD}/2$.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1 on Page 39.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2 on page 42.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 on page 42 through Table 10 on page 47.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
 $R_{ON} = R_{ZQ}/7$ (34 Ohm in MR1);
 $Q_{off} = 0_B$ (Output Buffer enabled in MR1);
 $R_{TT_Nom} = R_{ZQ}/6$ (40 Ohm in MR1);
 $R_{TT_Wr} = R_{ZQ}/2$ (120 Ohm in MR2);
 TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define $\overline{D} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{HIGH, LOW, LOW, LOW\}$
- Define $\overline{\overline{D}} = \{\overline{CS}, \overline{RAS}, \overline{CAS}, \overline{WE}\} = \{HIGH, HIGH, HIGH, HIGH\}$

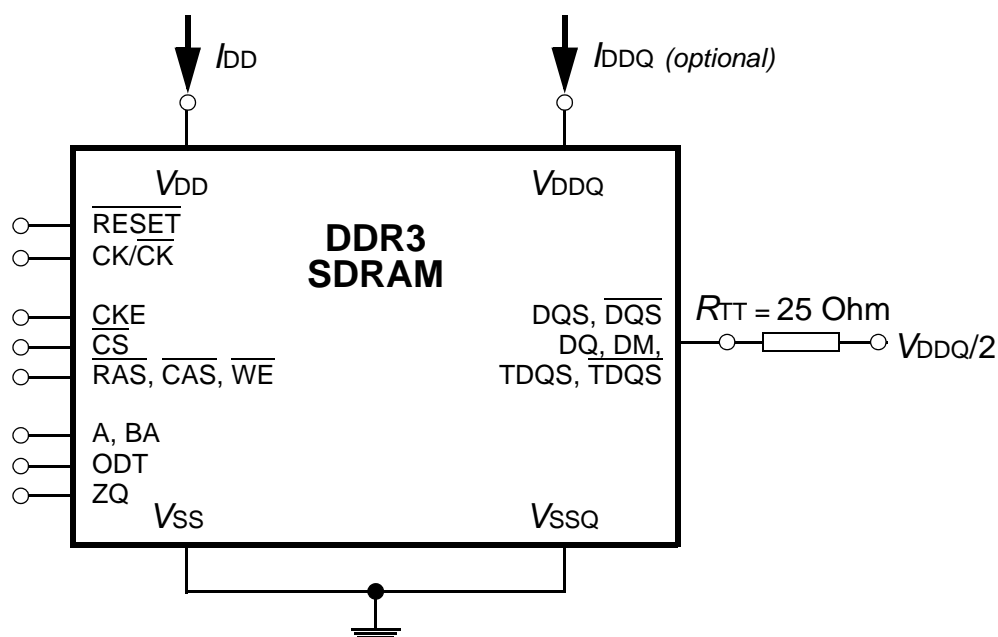


Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements
[Note: DIMM level Output test load condition may be different from above]

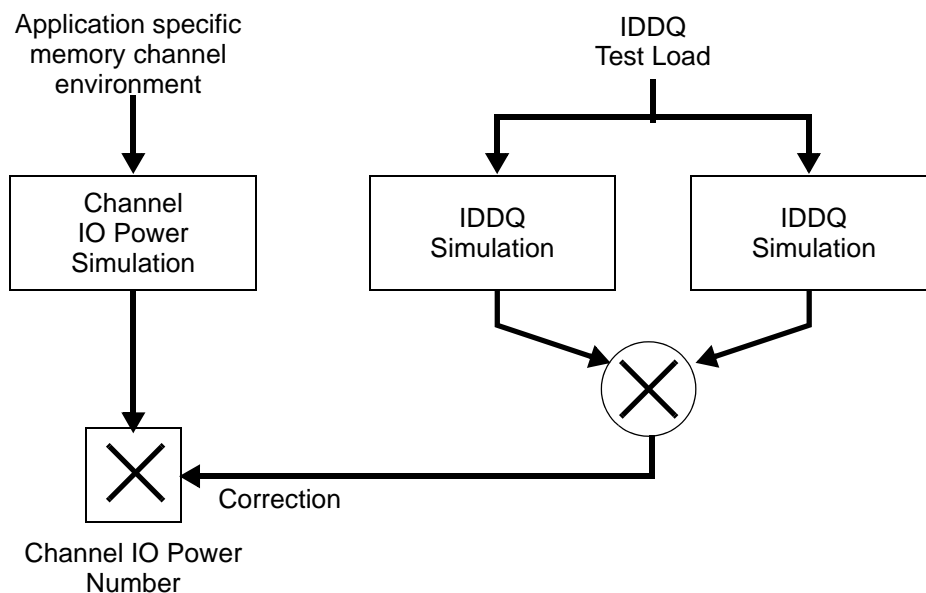


Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		DDR3-800	DDR3-1066	DDR3-1333	Unit
		5-5-5	7-7-7	9-9-9	
t_{CK}		2.5	1.875	1.5	ns
CL		5	7	9	nCK
η_{RCD}		5	7	9	nCK
η_{RC}		20	27	33	nCK
η_{RAS}		15	20	24	nCK
η_{RP}		5	7	9	nCK
η_{FAW}	x4/x8	16	20	20	nCK
	x16	20	27	30	nCK
η_{RRD}	x4/x8	4	4	4	nCK
	x16	4	6	5	nCK
η_{RFC} -512Mb		36	48	60	nCK
η_{RFC} -1 Gb		44	59	74	nCK
η_{RFC} - 2 Gb		64	86	107	nCK
η_{RFC} - 4 Gb		120	160	200	nCK
η_{RFC} - 8 Gb		140	187	234	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	Description
I_{DD0}	<p>Operating One Bank Active-Precharge Current</p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1 on page 39; BL: 8^a); AL: 0; \overline{CS}: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3 on page 42; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3 on page 42); Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: stable at 0; Pattern Details: see Table 3 on page 42</p>
I_{DD1}	<p>Operating One Bank Active-Precharge Current</p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1 on page 39; BL: 8^a); AL: 0; \overline{CS}: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO: partially toggling according to Table 4 on page 43; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4 on page 43); Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: stable at 0; Pattern Details: see Table 4 page 43</p>
I_{DD2N}	<p>Precharge Standby Current</p> <p>CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^a); AL: 0; \overline{CS}: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 44; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: stable at 0; Pattern Details: see Table 5 on page 44</p>

I_{DD2NT}	<p>Precharge Standby ODT Current</p> <p>CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^{a)}; AL: 0; \overline{CS}: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6 on page 44; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers^{b)}; ODT Signal: toggling according to Table 6 on page 44; Pattern Details: see Table 6 on page 44</p>
I_{DDQ2NT} (optional)	<p>Precharge Standby ODT IDDQ Current</p> <p>Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current</p>
I_{DD2P0}	<p>Precharge Power-Down Current Slow Exit</p> <p>CKE: Low; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^{a)}; AL: 0; \overline{CS}: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers^{b)}; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit^{c)}</p>
I_{DD2P1}	<p>Precharge Power-Down Current Fast Exit</p> <p>CKE: Low; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^{a)}; AL: 0; \overline{CS}: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers^{b)}; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit^{c)}</p>
I_{DD2Q}	<p>Precharge Quiet Standby Current</p> <p>CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^{a)}; AL: 0; \overline{CS}: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers^{b)}; ODT Signal: stable at 0</p>
I_{DD3N}	<p>Active Standby Current</p> <p>CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^{a)}; AL: 0; \overline{CS}: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 44; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers^{b)}; ODT Signal: stable at 0; Pattern Details: see Table 5 on page 44</p>
I_{DD3P}	<p>Active Power-Down Current</p> <p>CKE: Low; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^{a)}; AL: 0; \overline{CS}: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers^{b)}; ODT Signal: stable at 0</p>
I_{DDQ4R} (optional)	<p>Operating Burst Read IDDQ Current</p> <p>Same definition like for IDD4R, however measuring IDDQ current instead of IDD current</p>

I_{DD4R}	<p>Operating Burst Read Current</p> <p>CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^a; AL: 0; \overline{CS}: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7 on page 45; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7 on page 45; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7 on page 45); Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: stable at 0; Pattern Details: see Table 7 on page 45</p>
I_{DD4W}	<p>Operating Burst Write Current</p> <p>CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8^a; AL: 0; \overline{CS}: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8 on page 45; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8 on page 45; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8 on page 45); Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: stable at HIGH; Pattern Details: see Table 8 on page 45</p>
I_{DD5B}	<p>Burst Refresh Current</p> <p>CKE: High; External clock: On; tCK, CL, nRFC: see Table 1 on page 38; BL: 8^a; AL: 0; \overline{CS}: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9 on page 45; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9 on page 45); Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: stable at 0; Pattern Details: see Table 9 on page 45</p>
I_{DD6}	<p>Self-Refresh Current: Normal Temperature Range</p> <p>T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled^d); Self-Refresh Temperature Range (SRT): Normal^e);</p> <p>CKE: Low; External clock: Off; CK and \overline{CK}: LOW; CL: see Table 1 on page 4; BL: 8^a; AL: 0; \overline{CS}, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: FLOATING</p>
I_{DD6ET}	<p>Self-Refresh Current: Extended Temperature Range (optional)^f</p> <p>T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled^d); Self-Refresh Temperature Range (SRT): Extended^e);</p> <p>CKE: Low; External clock: Off; CK and \overline{CK}: LOW; CL: see Table 1 on page 4; BL: 8^a; AL: 0; \overline{CS}, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: FLOATING</p>
I_{DD6TC}	<p>Auto Self-Refresh Current (optional)^f</p> <p>T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Enabled^d); Self-Refresh Temperature Range (SRT): Normal^e); CKE: Low; External clock: Off; CK and \overline{CK}: LOW; CL: see Table 1 on page 39; BL: 8^a; AL: 0; \overline{CS}, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers^b); ODT Signal: FLOATING</p>

I_{DD7}	<p>Operating Bank Interleave Read Current</p> <p>CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1 on page 39; BL: 8^{a)}; AL: CL-1; \overline{CS}: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10 on page 47; Data IO: read data burst with different data between one burst and the next one according to Table 10 on page 47; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, see Table 10 on page 47; Output Buffer and RTT: Enabled in Mode Registers^{b)}; ODT Signal: stable at 0; Pattern Details: see Table 10 on page 47</p>
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a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B

b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B

c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit

d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature

e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range

f) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device

Table 3 - IDD0 Measurement-Loop Pattern^{a)}

\overline{CK} , CK	CKE	Sub-Loop	Cycle Number	Command	\overline{CS}	RAS	CAS	\overline{WE}	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	\overline{D} , \overline{D}	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	00	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, \overline{DQS} are FLOATING.

b) DQ signals are FLOATING.

Table 4 - IDD1 Measurement-Loop Pattern^{a)}

CK, CK	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are used according to RD Commands, otherwise FLOATING.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

Table 5 - IDD2N and IDD3N Measurement-Loop Pattern^{a)}

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are FLOATING.

b) DQ signals are FLOATING.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern^{a)}

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	F	0	-
			3	$\overline{\text{D}}$	1	1	1	1	0	0	0	0	0	F	0	00000000
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are FLOATING.

b) DQ signals are FLOATING.

Table 7 - IDD4R and IDDQ24R Measurement-Loop Pattern^{a)}

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
		5	5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. $\overline{\text{DQS}}$, $\overline{\text{DQS}}$ are used according to RD Commands, otherwise FLOATING.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

Table 8 - IDD4W Measurement-Loop Pattern^{a)}

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
		5	5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. $\overline{\text{DQS}}$, $\overline{\text{DQS}}$ are used according to WR Commands, otherwise FLOATING.

b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are FLOATING.

Table 9 - IDD5B Measurement-Loop Pattern^{a)}

CK, $\overline{\text{CK}}$	CKE	Sub-Loop	Cycle Number	Command	$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	$\overline{\text{D}}, \overline{\text{D}}$	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necessary.												

a) DM must be driven LOW all the time. DQS, $\overline{\text{DQS}}$ are FLOATING.

b) DQ signals are FLOATING.

Table 10 - IDD7 Measurement-Loop Pattern^{a)}

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data ^{b)}
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00	0	0	F	0	-
			...	Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
			...	Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
			...	Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
			...	Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		14	3*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, \overline{DQS} are used according to RD Commands, otherwise FLOATING.

b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

8.2 IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

I_{DD} Specification

Speed Grade Bin	DDR3 - 800 6-6-6	DDR3 - 1066 7-7-7	DDR3 - 1333 9-9-9	Unit	Notes
Symbol	Max.	Max.	Max.		
I_{DD0}	80	92	100	mA	x4/x8
	100	110	125	mA	x16
I_{DD1}	100	115	125	mA	x4/x8
	130	140	160	mA	x16
I_{DD2N}	55	65	75	mA	x4/x8
	55	70	82	mA	x16
I_{DD2NT}	60	70	80	mA	x4/x8
	60	72	85	mA	x16
I_{DDQ2NT}	82	82	82	mA	x4/x8
	150	150	150	mA	x16
I_{DD2P0}	10	10	10	mA	x4/x8/x16
I_{DD2P1}	26	28	30	mA	x4/x8
	26	28	35	mA	x16
I_{DD2Q}	55	65	75	mA	x4/x8
	55	70	85	mA	x16
I_{DD3N}	65	75	85	mA	x4/x8
	60	75	90	mA	x16
I_{DD3P}	30	40	45	mA	x4/x8
	35	45	55	mA	x16
I_{DD4R}	140	170	210	mA	x4/x8
	200	230	280	mA	x16
I_{DDQ4R}	60	60	60	mA	x4/x8
	130	130	130	mA	x16
I_{DD4W}	160	200	230	mA	x4/x8
	210	260	300	mA	x16
I_{DD5B}	190	200	210	mA	x4/x8
	200	210	230	mA	x16
I_{DD6}	10	10	10	mA	x4/x8/x16
I_{DD6ET}	12	12	12	mA	x4/x8/x16
I_{DD6TC}	12	12	12	mA	x4/x8/x16
I_{DD7}	210	250	300	mA	x4/x8
	250	280	370	mA	x16

9. Input/Output Capacitance

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Input/output capacitance (DQ, DM, DQS, $\overline{\text{DQS}}$, TDQS, $\overline{\text{TDQS}}$)	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	pF	1,2,3
Input capacitance, CK and $\overline{\text{CK}}$	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	pF	2,3
Input capacitance delta CK and $\overline{\text{CK}}$	C_{DCK}	0	0.15	0	0.15	0	0.15	pF	2,3,4
Input capacitance (All other input-only pins)	C_{I}	0.75	1.5	0.75	1.5	0.75	1.3	pF	2,3,6
Input capacitance delta, DQS and $\overline{\text{DQS}}$	C_{DDQS}	0	0.20	0	0.20	0	0.15	pF	2,3,5
Input capacitance delta (All CTRL input-only pins)	$C_{\text{DI_CTRL}}$	-0.5	0.3	-0.5	0.3	-0.4	0.2	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{\text{DI_ADD_CMD}}$	-0.5	0.5	-0.5	0.5	-0.4	0.4	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{\text{DQS}}$)	C_{DIO}	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2,3,11

Notes:

- Although the DM, TDQS and $\overline{\text{TDQS}}$ pins have different functions, the loading matches DQ and DQS.
- This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, $\overline{\text{RESET}}$ and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
- This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
- Absolute value of $C_{\text{CK}} - C_{\overline{\text{CK}}}$.
- The minimum C_{CK} will be equal to the minimum C_{I} .
- Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$.
- CTRL pins defined as ODT, CS and CKE.
- $C_{\text{DI_CTRL}} = C_{\text{I}}(\text{CNTL}) - 0.5 * C_{\text{I}}(\text{CLK}) + C_{\text{I}}(\overline{\text{CLK}})$
- ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$.
- $C_{\text{DI_ADD_CMD}} = C_{\text{I}}(\text{ADD_CMD}) - 0.5 * (C_{\text{I}}(\text{CLK}) + C_{\text{I}}(\overline{\text{CLK}}))$
- $C_{\text{DIO}} = C_{\text{IO}}(\text{DQ}) - 0.5 * (C_{\text{IO}}(\text{DQS}) + C_{\text{IO}}(\overline{\text{DQS}}))$

10. Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

DDR3-800 Speed Bins

For specific Notes See “Speed Bin Table Notes” on page 53..						
Speed Bin			DDR3-800E		Unit	Notes
CL - nRCD - nRP			6-6-6			
Parameter	Symbol	min	max			
Internal read command to first data	t_{AA}	15	20		ns	
ACT to internal read or write delay time	t_{RCD}	15	—		ns	
PRE command period	t_{RP}	15	—		ns	
ACT to ACT or REF command period	t_{RC}	52.5	—		ns	
ACT to PRE command period	t_{RAS}	37.5	9 * tREFI		ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1)2)3)
Supported CL Settings			6		n_{CK}	
Supported CWL Settings			5		n_{CK}	

DDR3-1066 Speed Bins

For specific Notes See “Speed Bin Table Notes” on page 53.

Speed Bin			DDR3-1066F		Unit	Note
CL - nRCD - nRP			7-7-7			
Parameter	Symbol	min	max			
Internal read command to first data	t_{AA}	13.125	20		ns	
ACT to internal read or write delay time	t_{RCD}	13.125	—		ns	
PRE command period	t_{RP}	13.125	—		ns	
ACT to ACT or REF command period	t_{RC}	50.625	—		ns	
ACT to PRE command period	t_{RAS}	37.5	9 * tREFI		ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	4)
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1)2)3)6)
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1)2)3)4)
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1)2)3)4)
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4)
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1)2)3)
Supported CL Settings			6, 7, 8		n_{CK}	
Supported CWL Settings			5, 6		n_{CK}	

DDR3-1333 Speed Bins

For specific Notes See “Speed Bin Table Notes” on page 53.

Speed Bin			DDR3-1333H		Unit	Note
CL - nRCD - nRP			9-9-9			
Parameter	Symbol	min	max			
Internal read command to first data	t_{AA}	13.5	20		ns	
ACT to internal read or write delay time	t_{RCD}	13.5	—		ns	
PRE command period	t_{RP}	13.5	—		ns	
ACT to ACT or REF command period	t_{RC}	49.5	—		ns	
ACT to PRE command period	t_{RAS}	36	9 * tREFI		ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,4,7
			(Optional) Note 9.10			
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	< 2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	<1.875	ns	1,2,3
			(Optional)		ns	5
Supported CL Settings			6,(7), 8, 9		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

Speed Bin Table Notes

Absolute Specification (T_{OPER} ; $V_{\text{DDQ}} = V_{\text{DD}} = 1.5\text{V} \pm 0.075\text{V}$);

Notes:

1. The CL setting and CWL setting result in $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ and $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ requirements. When making a selection of $t_{\text{CK}}(\text{AVG})$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{\text{CK}}(\text{AVG})_{\text{MIN}}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{\text{CK}}(\text{AVG})$ value (2.5, 1.875, 1.5, or 1.25 ns) when calculating $\text{CL}[\text{nCK}] = t_{\text{AA}}[\text{ns}] / t_{\text{CK}}(\text{AVG})[\text{ns}]$, rounding up to the next 'Supported CL'.
3. $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ limits: Calculate $t_{\text{CK}}(\text{AVG}) = t_{\text{AA}}_{\text{MAX}} / \text{CL}_{\text{SELECTED}}$ and round the resulting $t_{\text{CK}}(\text{AVG})$ down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is $t_{\text{CK}}(\text{AVG})_{\text{MAX}}$ corresponding to $\text{CL}_{\text{SELECTED}}$.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. It is not a mandatory bin. Refer to supplier's data sheet and/or the DIMM SPD information.
10. If it's supported, the minimum $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RP}}$ that this device support is 13.125ns. Therefore, In Module application, $t_{\text{AA}}/t_{\text{RCD}}/t_{\text{RP}}$ should be programed with minimum supported values. For example, DDR3-1333H supporting down-shift to DDR3-1066F should program SPD as 13.125ns for $t_{\text{AAmin}}(\text{Byte16})/t_{\text{RCDmin}}(\text{Byte18})/t_{\text{RP}}(\text{Byte20})$. DDR3-1600K supporting down-shift to DDR3-1333H and/or DDR3-1066F should program SPD as 13.125ns for $t_{\text{AAmin}}(\text{Byte16})/t_{\text{RCDmin}}(\text{Byte18})/t_{\text{RP}}(\text{Byte20})$.

11. Electrical Characteristics and AC Timing

Timing Parameters by Speed Bin

Note: The following general notes from page 61 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	$t_{\text{CK}}(\text{DLL_OFF})$	8	-	8	-	8	-	ns	6
Average Clock Period	$t_{\text{CK}}(\text{avg})$	See "10. Standard Speed Bins" on page 50.						ps	f
Average high pulse width	$t_{\text{CH}}(\text{avg})$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{\text{CK}}(\text{avg})$	f
Average low pulse width	$t_{\text{CL}}(\text{avg})$	0.47	0.53	0.47	0.53	0.47	0.53	$t_{\text{CK}}(\text{avg})$	f
Absolute Clock Period	$t_{\text{CK}}(\text{abs})$	$t_{\text{CK}}(\text{avg})_{\text{min}} + t_{\text{JIT}}(\text{per})_{\text{min}}$	$t_{\text{CK}}(\text{avg})_{\text{max}} + t_{\text{JIT}}(\text{per})_{\text{max}}$	$t_{\text{CK}}(\text{avg})_{\text{min}} + t_{\text{JIT}}(\text{per})_{\text{min}}$	$t_{\text{CK}}(\text{avg})_{\text{max}} + t_{\text{JIT}}(\text{per})_{\text{max}}$	$t_{\text{CK}}(\text{avg})_{\text{min}} + t_{\text{JIT}}(\text{per})_{\text{min}}$	$t_{\text{CK}}(\text{avg})_{\text{max}} + t_{\text{JIT}}(\text{per})_{\text{max}}$	ps	

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

		DDR3-800		DDR3-1066		DDR3-1333			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Units	Notes
Absolute clock HIGH pulse width	tCH (abs)	0.43	-	0.43	-	0.43	-	tCK (avg)	25
Absolute clock LOW pulse width	tCL (abs)	0.43	-	0.43	-	0.43	-	tCK (avg)	26
Clock Period Jitter	JIT (per)	- 100	100	- 90	90	- 80	80	ps	
Clock Period Jitter during DLL locking period	tJIT (per, lck)	- 90	90	- 80	80	- 70	70	ps	
Cycle to Cycle Period Jitter	tJIT (cc)	200		180		160		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	180		160		140		ps	
Duty Cycle jitter	tJIT (duty)	-	-	-	-	-	-	ps	
Cumulative error across 2 cycles	tERR (2per)	-147	147	-132	132	-118	118	ps	
Cumulative error across 3 cycles	tERR (3per)	-175	175	-157	157	-140	140	ps	
Cumulative error across 4 cycles	tERR (4per)	-194	194	-175	175	-155	155	ps	
Cumulative error across 5 cycles	tERR (5per)	-209	209	-188	188	-168	168	ps	
Cumulative error across 6 cycles	tERR (6per)	-222	222	-200	200	-177	177	ps	
Cumulative error across 7 cycles	tERR (7per)	-232	232	-209	209	-186	186	ps	
Cumulative error across 8 cycles	tERR (8per)	-241	241	-217	217	-193	193	ps	
Cumulative error across 9 cycles	tERR (9per)	-249	249	-224	224	-200	200	ps	
Cumulative error across 10 cycles	tERR (10per)	-257	257	-231	231	-205	205	ps	
Cumulative error across 11 cycles	tERR (11per)	-263	263	-237	237	-210	210	ps	
Cumulative error across 12 cycles	tERR (12per)	-269	269	-242	242	-215	215	ps	
Cumulative error across n = 13, 14,.....49, 50 cycles	tERR (nper)	tERR (nper) min = (1 + 0.68ln(n)) * JIT (per) min tERR (nper) max = (1 + 0.68ln(n)) * JIT (per) max						ps	24
Data Timing									
DQS, \overline{DQS} to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	ps	13
DQ output hold time from DQS, \overline{DQS}	tQH	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQ low-impedance time from CK, \overline{CK}	tLZ (DQ)	- 800	400	- 600	300	- 500	250	ps	13, 14, a

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
DQ high impedance time from CK, $\overline{\text{CK}}$	tHZ (DQ)	-	400	-	300	-	250	ps	13, 14, a
Data setup time to DQS, $\overline{\text{DQS}}$ referenced to Vih (ac) / Vil (ac) levels	tDS (base)	75		25		TBD		ps	d, 17
Data hold time from DQS, $\overline{\text{DQS}}$ referenced to Vih (dc) / Vil (dc) levels	tDH (base)	150		100		TBD		ps	d, 17
Data Strobe Timing									
DQS, $\overline{\text{DQS}}$ differential READ Preamble	tRPRE	0.9	Note	0.9	Note	0.9	Note	tCK (avg)	13, 19 b
DQS, $\overline{\text{DQS}}$ differential READ Postamble	tRPST	0.3	Note	0.3	Note	0.3	Note	tCK (avg)	11, 13, b
DQS, $\overline{\text{DQS}}$ differential output high time	tQSH	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, $\overline{\text{DQS}}$ differential output low time	tQSL	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, $\overline{\text{DQS}}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK (avg)	
DQS, $\overline{\text{DQS}}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK (avg)	
DQS, $\overline{\text{DQS}}$ rising edge output access time from rising CK, $\overline{\text{CK}}$	tDQSK	- 400	400	- 300	300	- 255	255	ps	13, a
DQS and $\overline{\text{DQS}}$ low-impedance time (Referenced from RL - 1)	tLZ(DQS)	- 800	400	- 600	300	- 500	250	ps	13, 14, a
DQS and $\overline{\text{DQS}}$ high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	400	-	300	-	250	ps	13, 14 a
DQS, $\overline{\text{DQS}}$ differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, $\overline{\text{DQS}}$ differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, $\overline{\text{DQS}}$ rising edge to CK, $\overline{\text{CK}}$ rising edge	tDQSS	- 0.25	0.25	- 0.25	0.25	- 0.25	0.25	tCK (avg)	c

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, $\overline{\text{CK}}$ rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK (avg)	c
DQS, $\overline{\text{DQS}}$ falling edge hold time from CK, $\overline{\text{CK}}$ rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK (avg)	c
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 7.5ns)	-		e, 18
WRITE recovery time	tWR	15	-	15	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max (12nCK, 15ns)	-	max (12nCK, 15ns)	-	max (12nCK, 15ns)	-		
ACT to internal read or write delay time	tRCD	Refer to Table on pages 50 to pages 53							e
PRE command period	tRP	Refer to Table on pages 50 to pages 53							e
ACT to ACT or REF command period	tRC	Refer to Table on pages 50 to pages 53							e
CAS to CAS command delay	tCCD	4	-	4	-	4	-	nCK	
Auto precharge write recovery + precharge time	tDAL (min)	WR + roundup (tRP / tCK (avg))						nCK	
End of MPR Read burst to MSR for MPR (exit)	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	See "10. Standard Speed Bins" on page 50.							e
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4nCK, 10ns)	-	max (4nCK, 7.5ns)	-	max (4nCK, 6ns)	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4nCK, 10ns)	-	max (4nCK, 10ns)	-	max (4nCK, 7.5ns)	-		e
Four activate window for 1KB page size	tFAW	40	-	37.5	-	30	-	ns	e

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Four activate window for 2KB page size	tFAW	50	-	50	-	45	-	ns	e
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to Vih (ac) / Vil (ac) levels	tIS (base)	200		125		65		ps	b, 16
Command and Address hold time from CK, $\overline{\text{CK}}$ referenced to Vih (dc) / Vil (dc) levels	tIH (base)	275		200		140		ps	b, 16
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to Vih (ac) / Vil (ac) levels	tIS (base) AC150	-	-	-	-	65+125		ps	b, 16, 27
Calibration Timing									
Power-up and RESET calibration time	tZQinit	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-		
Self Refresh Timings									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-	max (5nCK, tRFC (min) + 10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK (min)	-	tDLLK (min)	-	tDLLK (min)	-	nCK	
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE (min) + 1 nCK	-	tCKE (min) + 1 nCK	-	tCKE (min) + 1 nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-		

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-	max (5 nCK, 10 ns)	-		
Power Down Timings									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3nCK, 7.5ns)	-	max (3nCK, 7.5ns)	-	max (3nCK, 6ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-	max (10nCK, 24ns)	-		2
CKE minimum pulse width	tCKE	max (3nCK 7.5ns)	-	max (3nCK, 5.625ns)	-	max (3nCK, 5.625ns)	-		
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE (min)	9 * tREFI	tCKE (min)	9 * tREFI	tCKE (min)	9 * tREFI		15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 + 1	-	RL + 4 + 1	-	RL + 4 + 1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+ (tWR / tCK (avg))	-	WL4+ (tWR / tCK (avg))	-	WL+4 + (tWR / tCK (avg))	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+ WR + 1	-	WL+4+ WR+ 1	-	WL+4 + WR + 1	-	nCK	10

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+ (tWR / tCK (avg))	-	WL+2+ (tWR / tCK (avg))	-	WL+2 + (tWR / tCK (avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2 + WR + 1	-	WL + 2 + WR + 1	-	WL + 2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	nCK	,
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-		
ODT Timings									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	1	9	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	1	9	1	9	ns	
RTT turn-on	tAON	-400	400	-300	300	-250	250	ps	7, a
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	8, a
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	a
Write Leveling Timings									
First DQS/DQS rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	3
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	3

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		Units	Notes
		Min	Max	Min	Max	Min	Max		
Write leveling setup time from rising CK, CK crossing to rising DQS, $\overline{\text{DQS}}$ crossing	tWLS	325	-	245	-	195	-	ps	
Write leveling hold time from rising DQS, $\overline{\text{DQS}}$ crossing to rising CK, CK crossing	tWLH	325	-	245	-	195	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

0.1 Jitter Notes

- Specific Note a When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR}(mper)$, act of the input clock, where $2 \leq m \leq 12$. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR-800 SDRAM has $t_{ERR}(mper)$, act, min = -172 ps and $t_{ERR}(mper)$, act, max = +193 ps, then t_{DQSCK} , min (derated) = t_{DQSCK} , min - $t_{ERR}(mper)$, act, max = -400 ps - 193 ps = -593 ps and t_{DQSCK} , max (derated) = t_{DQSCK} , max - $t_{ERR}(mper)$, act, min = 400 ps + 172 ps = +572 ps. Similarly, $t_{LZ}(DQ)$ for DDR3-800 derates to $t_{LZ}(DQ)$, min (derated) = -800 ps - 193 ps = -993 ps and $t_{LZ}(DQ)$, max (derated) = 400 ps + 172 ps = +572 ps. (Caution on the min/max usage!) Note that $t_{ERR}(mper)$, act, min is the minimum measured value of $t_{ERR}(nper)$ where $2 \leq n \leq 12$, and $t_{ERR}(mper)$, act, max is the maximum measured value of $t_{ERR}(nper)$ where $2 \leq n \leq 12$.
- Specific Note b When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT}(per)$, act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has $t_{CK}(avg)$, act = 2500 ps, $t_{JIT}(per)$, act, min = -72 ps and $t_{JIT}(per)$, act, max = +93 ps, then t_{RPRE} , min (derated) = t_{RPRE} , min + $t_{JIT}(per)$, act, min = $0.9 \times t_{CK}(avg)$, act + $t_{JIT}(per)$, act, min (derated) = t_{RPRE} , min + $t_{JIT}(per)$, act, min = $0.9 \times t_{CK}(avg)$, act + $t_{JIT}(per)$, act, min = 0.9×2500 ps - 72 ps = +2178 ps. Similarly, t_{QH} , min (derated) = t_{QH} , min + $t_{JIT}(per)$, act, min = $0.38 \times t_{CK}(avg)$, act + $t_{JIT}(per)$, act, min = 0.38×2500 ps - 72 ps = +878 ps. (Caution on the min/max usage!)
- Specific Note c These parameters are measured from a data strobe signal ($DQS(L/U)$, $\overline{DQS(L/U)}$) crossing to its respective clock signal (CK , \overline{CK}) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. $t_{JIT}(per)$, $t_{JIT}(cc)$, etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.
- Specific Note d These parameters are measured from a data signal ($DM(L/U)$, $\overline{DQ(L/U)0}$, $\overline{DQ(L/U)1}$, etc.) transition edge to its respective data strobe signal ($DQS(L/U)$, $\overline{DQS(L/U)}$) crossing.
- Specific Note e For these parameters, the DDR3 SDRAM device supports $tnPARAM[nCK] = RU \{tPARAM[ns] / tCK(avg)[ns]\}$, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support $tnRP = RU \{tRP / tCK(avg)\}$, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which $tRP = 15ns$, the device will support $tnRP = RU \{tRP / tCK(avg)\} = 6$, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at $Tm+6$ is valid even if $(Tm+6 - Tm)$ is less than 15ns due to input clock jitter.
- Specific Note f These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in Table .

Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
8. WR in clock cycles as programmed in MR0.
9. The maximum postamble is bound by tHZDQS (max)
10. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
11. Value is only valid for RON34
12. Single ended signal parameter. Refer to chapter <t.b.d.> for definition and measurement method.
13. tREFI depends on TOPER
14. tIS (base) and tIH (base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, \overline{CK} differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ (DC). For input only pins except \overline{RESET} , VRef (DC) = VRefCA (DC). See "Address / Command Setup, Hold and Derating" on page 63.
15. tDS (base) and tDH (base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, \overline{DQS} differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ (DC). For input only pins except \overline{RESET} , VRef (DC) = VRefCA (DC). See "Data Setup, Hold and Slew Rate Derating" on page 70..
16. Start of internal write transaction is defined as follows:
 - For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
 - For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
 - For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
17. The maximum preamble is bound by tLZDQS (min)
18. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
19. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN (min) is satisfied, there are cases where additional time such as tXPDLL (min) is also required.
20. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
21. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula.

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times Vdriftrate)}$$

where TSens = max (dRTTdT, dRONdTM) and VSens = max (dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities. For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 = 128ms$$

22. n = from 13 cycles to 50 cycles.
23. tCH (abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL (abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. The tIS (base) AC150 specifications are adjusted from the tIS (base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns].

Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS (base) and tIH (base) value (see Table 11) to the ΔtIS and ΔtIH derating value (see Table 12) respectively. Example: tIS (total setup time) = tIS (base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$ min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of V_{IL} (ac) max. If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 4). If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 6).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of V_{IL} (dc) max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of V_{IH} (dc) min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 5). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 6).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 14).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 12, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 11 - ADD/CMD Setup and Hold Base-Values for 1V/ns

unit [ps]	DDR3-800	DDR3-1066	DDR3-1333	reference
tIS (base)	200	125	65	$V_{IH/L(ac)}$
tIH (base)	275	200	140	$V_{IH/L(dc)}$
tIH(base)AC150	-	-	65 + 125	$V_{IH/L(dc)}$

Note: - (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

- The tIS (base) AC150 specifications are adjusted from the tIS (base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns]

Table 12 - Derating values DDR3-800/1066/1333 tIS/tIH - ac/dc based

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based AC175 Threshold -> $V_{IH}(ac) = V_{REF}(dc) + 175mV$, $V_{IL}(ac) = V_{REF}(dc) - 175mV$																	
		CK,CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD / ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

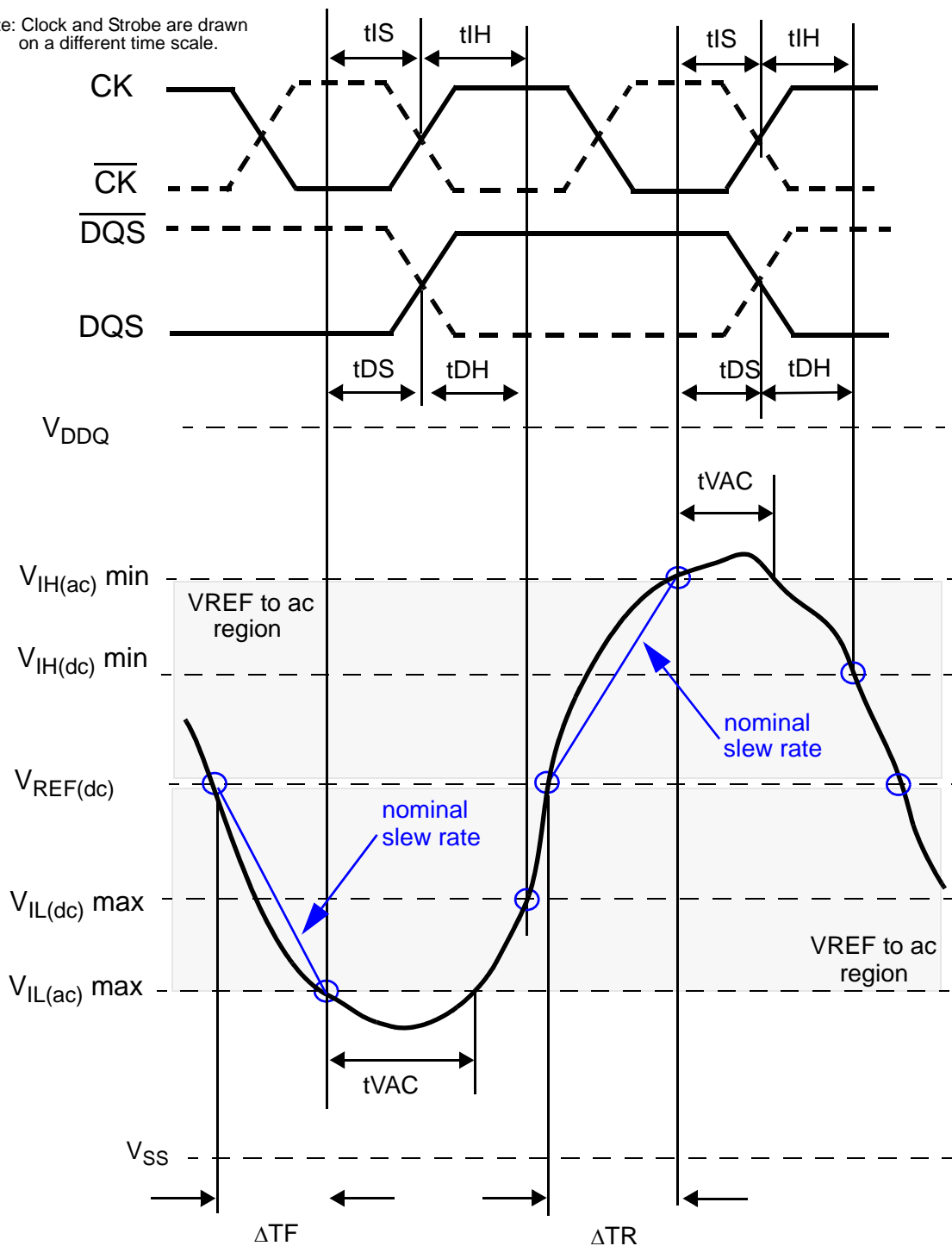
Table 13 - Derating values DDR3-800/1066/1333 tIS/tIH - ac/dc based

$\Delta tIS, \Delta tIH$ derating in [ps] AC/DC based Alternate AC150 Threshold $\rightarrow V_{IH}(ac) = V_{REF}(dc) + 150mV, V_{IL}(ac) = V_{REF}(dc) - 150mV$																	
		CK,CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD / ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Table 14 - Required time t_{VAC} above $V_{IH}(ac)$ {below $V_{IL}(ac)$ } for valid transition

Slew Rate [V/ns]	t_{VAC} @ 175 mV [ps]		t_{VAC} @ 150 mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

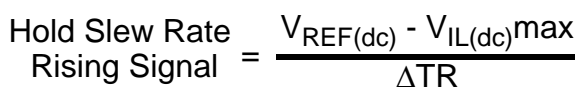
Note: Clock and Strobe are drawn on a different time scale.



$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)max}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)min} - V_{REF(dc)}}{\Delta TR}$$

Figure 3 - Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)min} - V_{REF(dc)}}{\Delta T_F}$$

Figure 4 - Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

Note: Clock and Strobe are drawn on a different time scale.

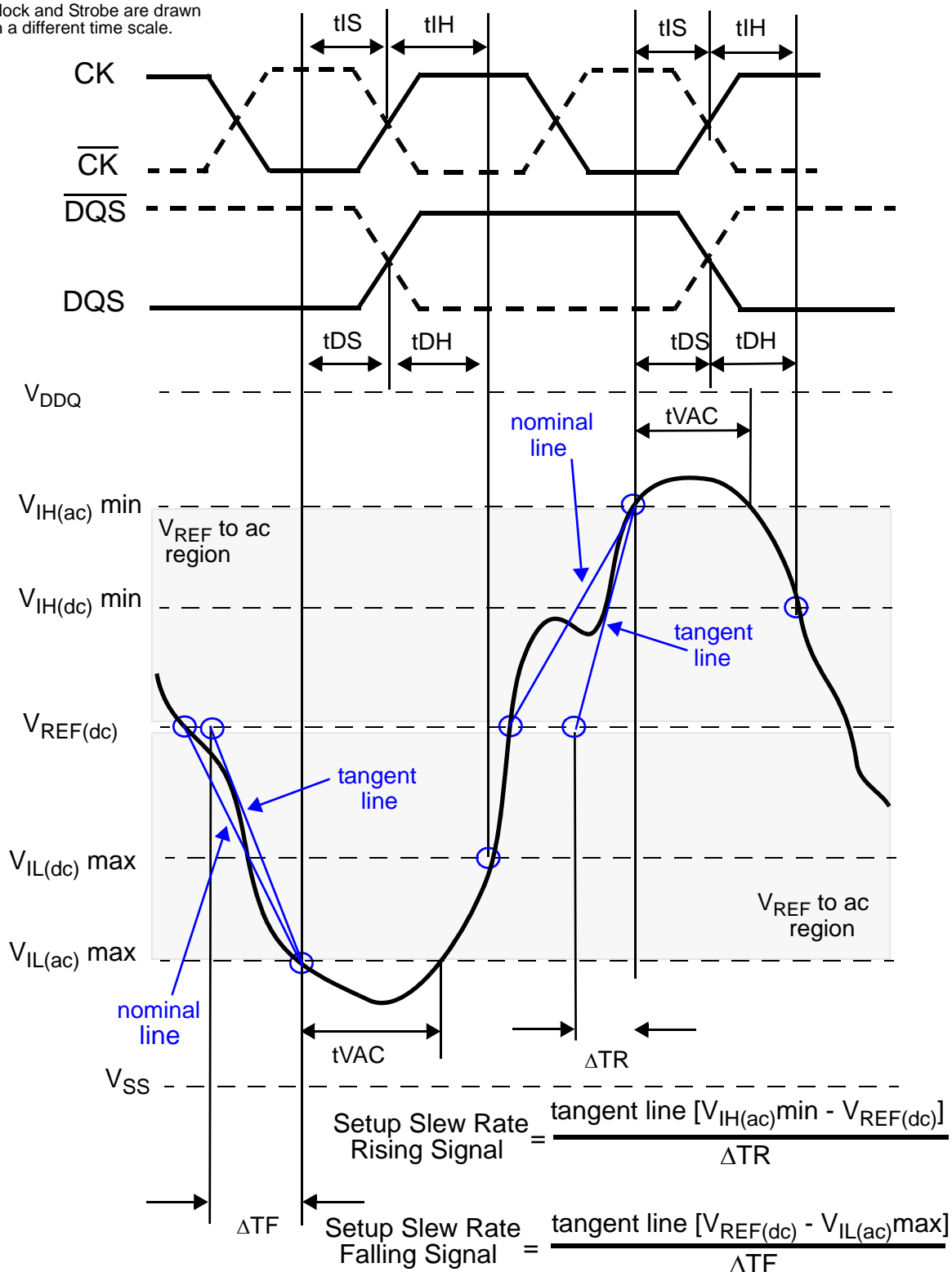


Figure 5 - Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

Note: Clock and Strobe are drawn on a different time scale.

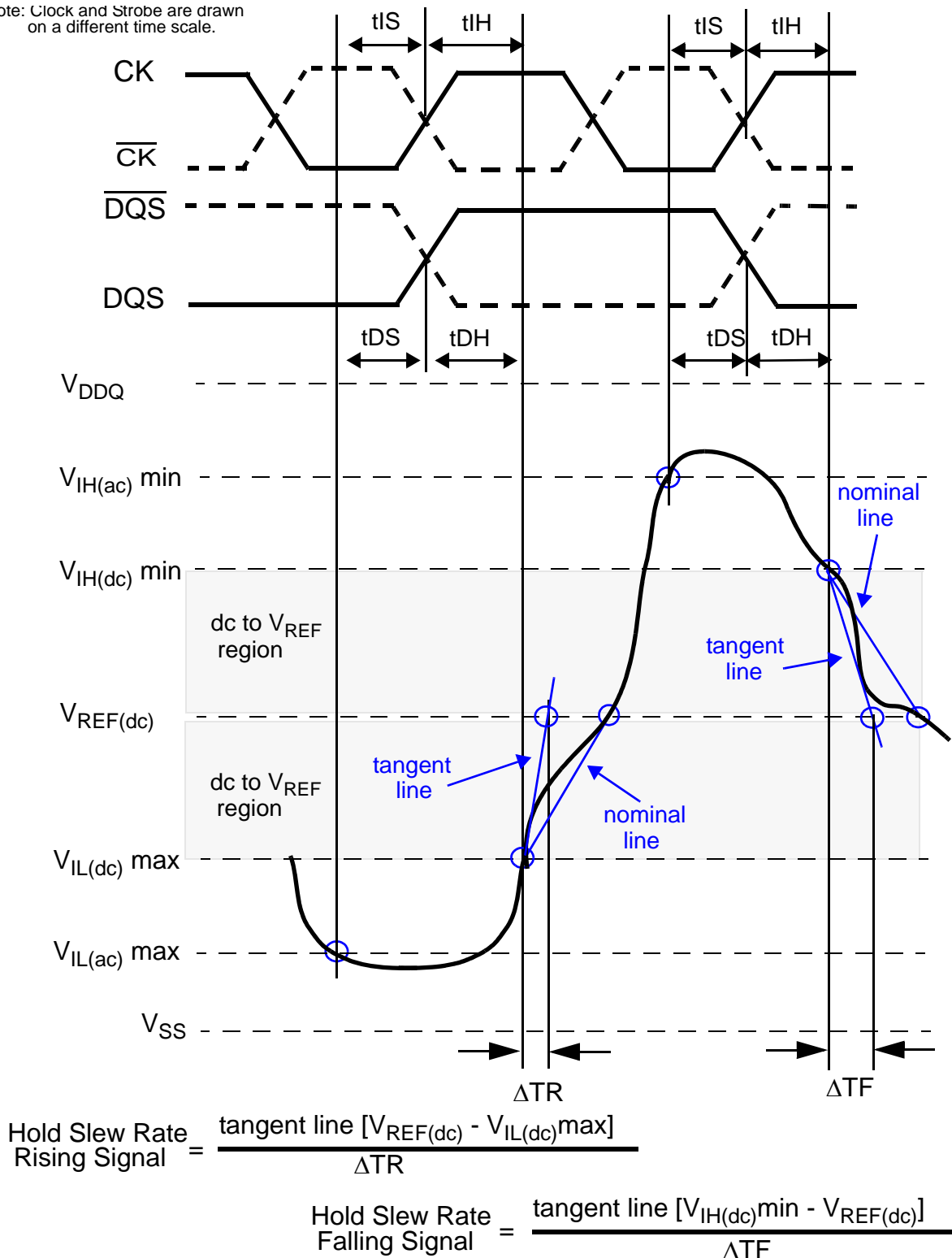


Figure 6 - Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS (base) and tDH (base) value (see Table 15) to the DtDS and DtDH (see Table 16) derating value respectively. Example: tDS (total setup time) = tDS (base) + DtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}min$. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}max$ (see Figure 7). If the actual signal is always earlier than the nominal slew rate line between shaded ' $V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded ' $V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 9).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}max$ and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}min$ and the first crossing of $V_{REF(dc)}$ (see Figure 8). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see figure 9).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 17).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 15 - Data Setup and Hold Base-Values

Units [ps]	DDR3-800	DDR3-1066	DDR3-1333	reference
tDS (base)	75	25	-10	$V_{IH/L(ac)}$
tDH (base)	150	100	65	$V_{IH/L(dc)}$

Note: (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS-slew rate)

Table 16 - Derating values DDR3-800/1066 tDS/tDH - ac/dc based

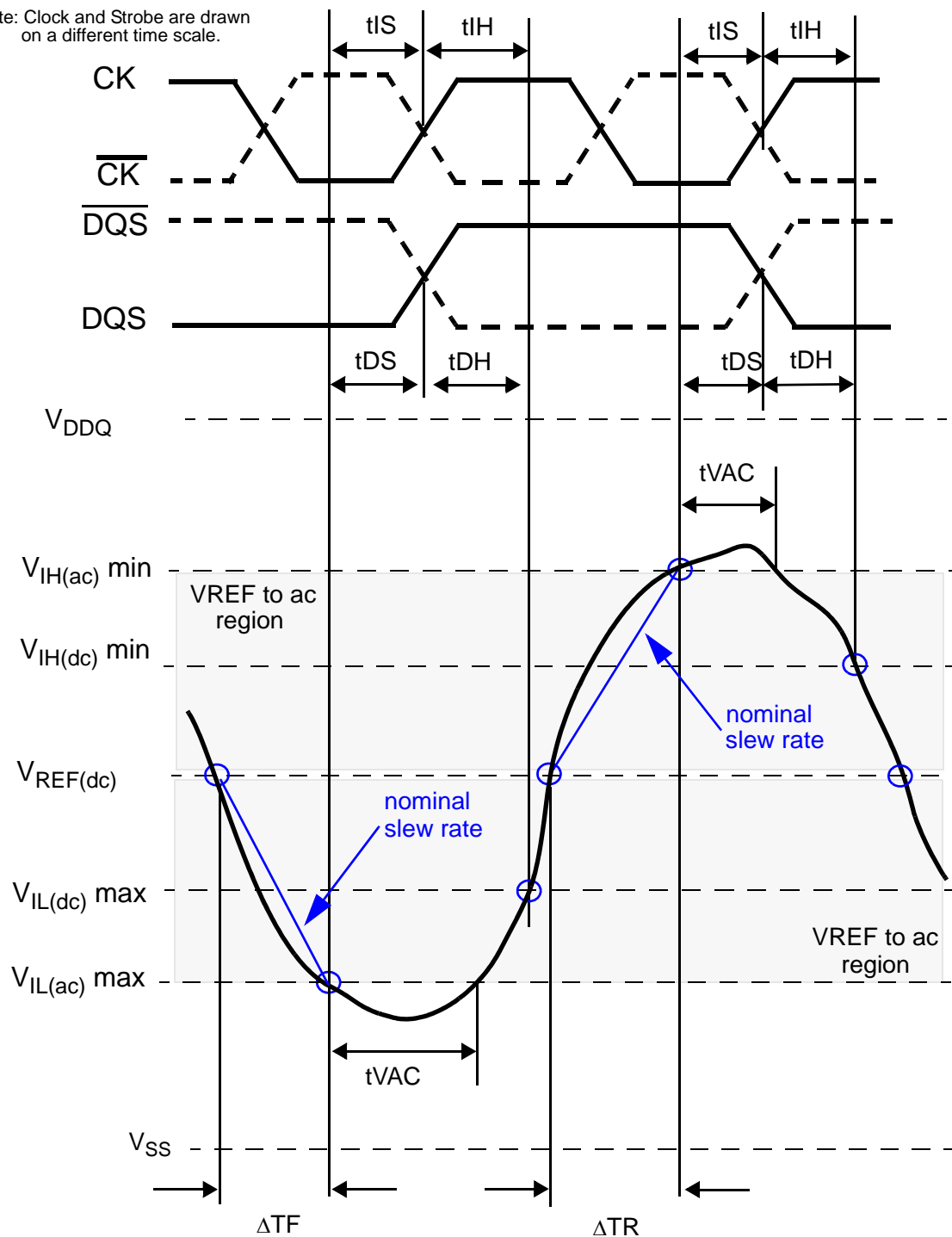
Δt_{DS} , Δt_{DH} derating in [ps] AC/DC based ^a																	
		DQS, DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}	Δt_{DS}	Δt_{DH}
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

a. Cell contents shaded in red are defined as 'not supported'.

Table 17 - Required time t_{VAC} above V_{IH} (ac) {below V_{IL} (ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} [ps]	
	min	max
> 2.0	75	-
2.0	57	-
1.5	50	-
1.0	38	-
0.9	34	-
0.8	29	-
0.7	22	-
0.6	13	-
0.5	0	-
< 0.5	0	-

Note: Clock and Strobe are drawn on a different time scale.

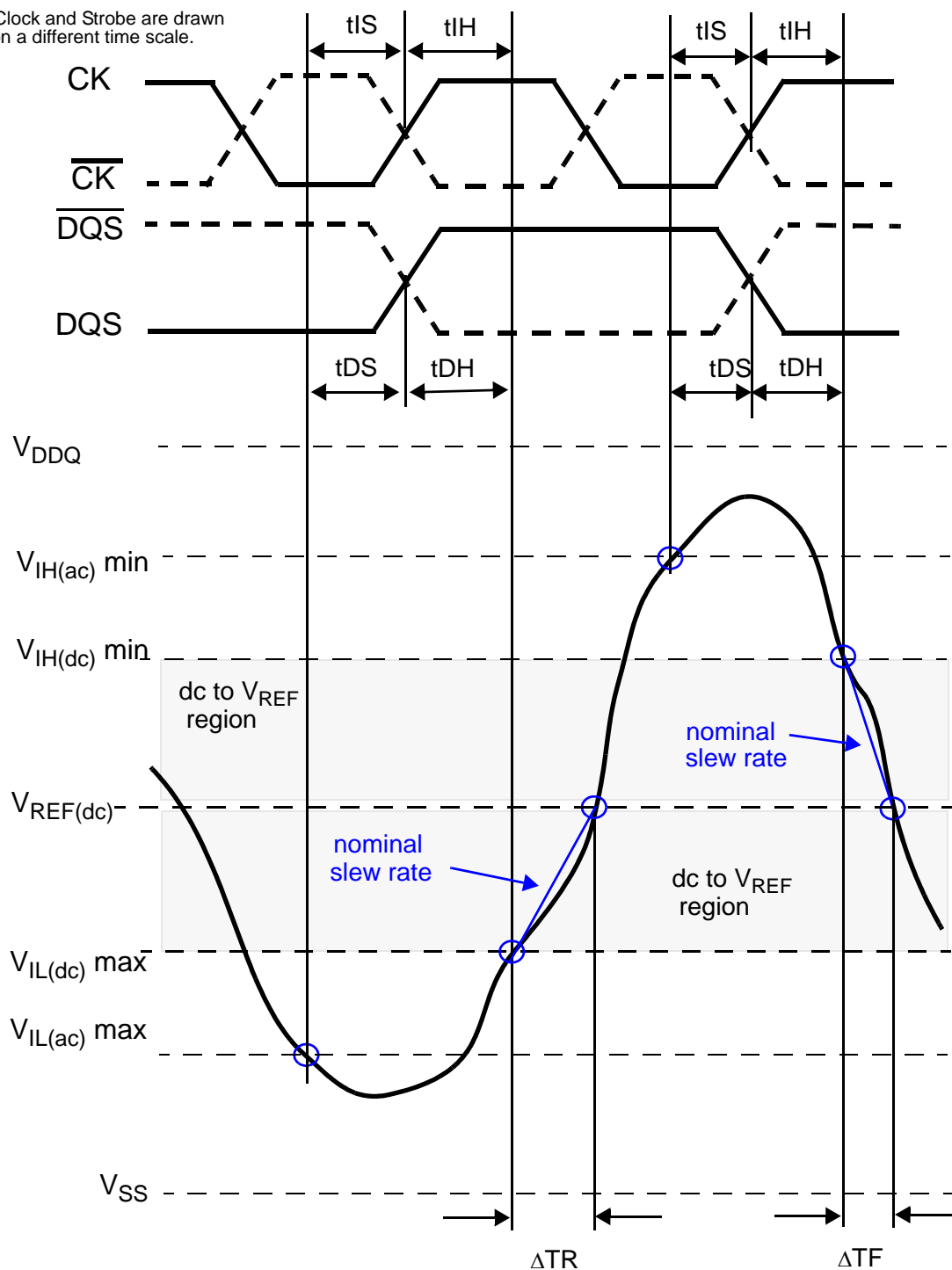


$$\text{Setup Slew Rate Falling Signal} = \frac{V_{\text{REF}(dc)} - V_{\text{IL}(ac)\text{max}}}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{\text{IH}(ac)\text{min}} - V_{\text{REF}(dc)}}{\Delta TR}$$

Figure 7 - Illustration of nominal slew rate and t_{VAC} for hold setup t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

Note: Clock and Strobe are drawn on a different time scale.



$$\text{Hold Slew Rate Rising Signal} = \frac{V_{\text{REF}(dc)} - V_{\text{IL}(dc)\text{max}}}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{\text{IH}(dc)\text{min}} - V_{\text{REF}(dc)}}{\Delta TF}$$

Figure 8 - Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

Note: Clock and Strobe are drawn on a different time scale.

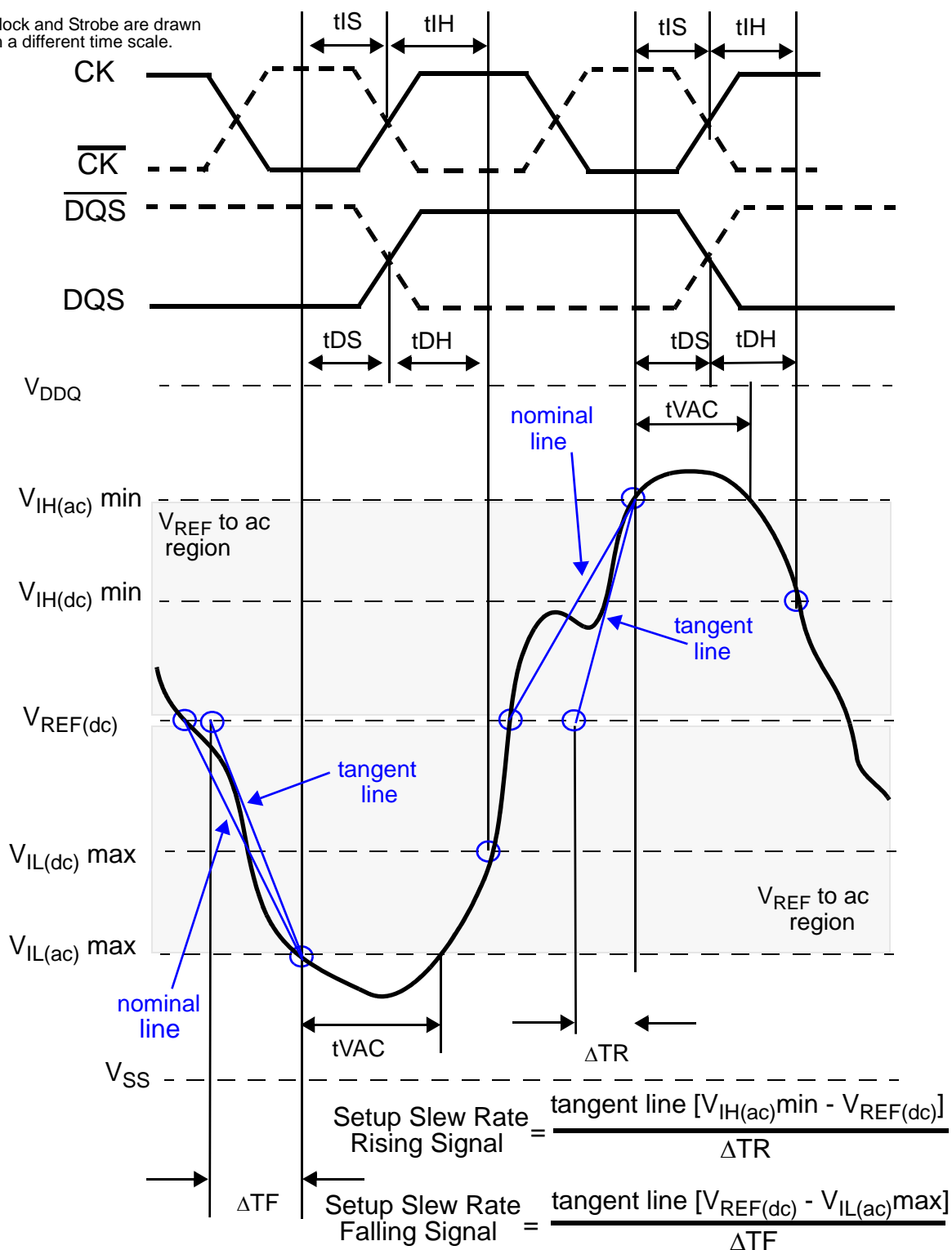


Figure 9 - Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

Note: Clock and Strobe are drawn on a different time scale.

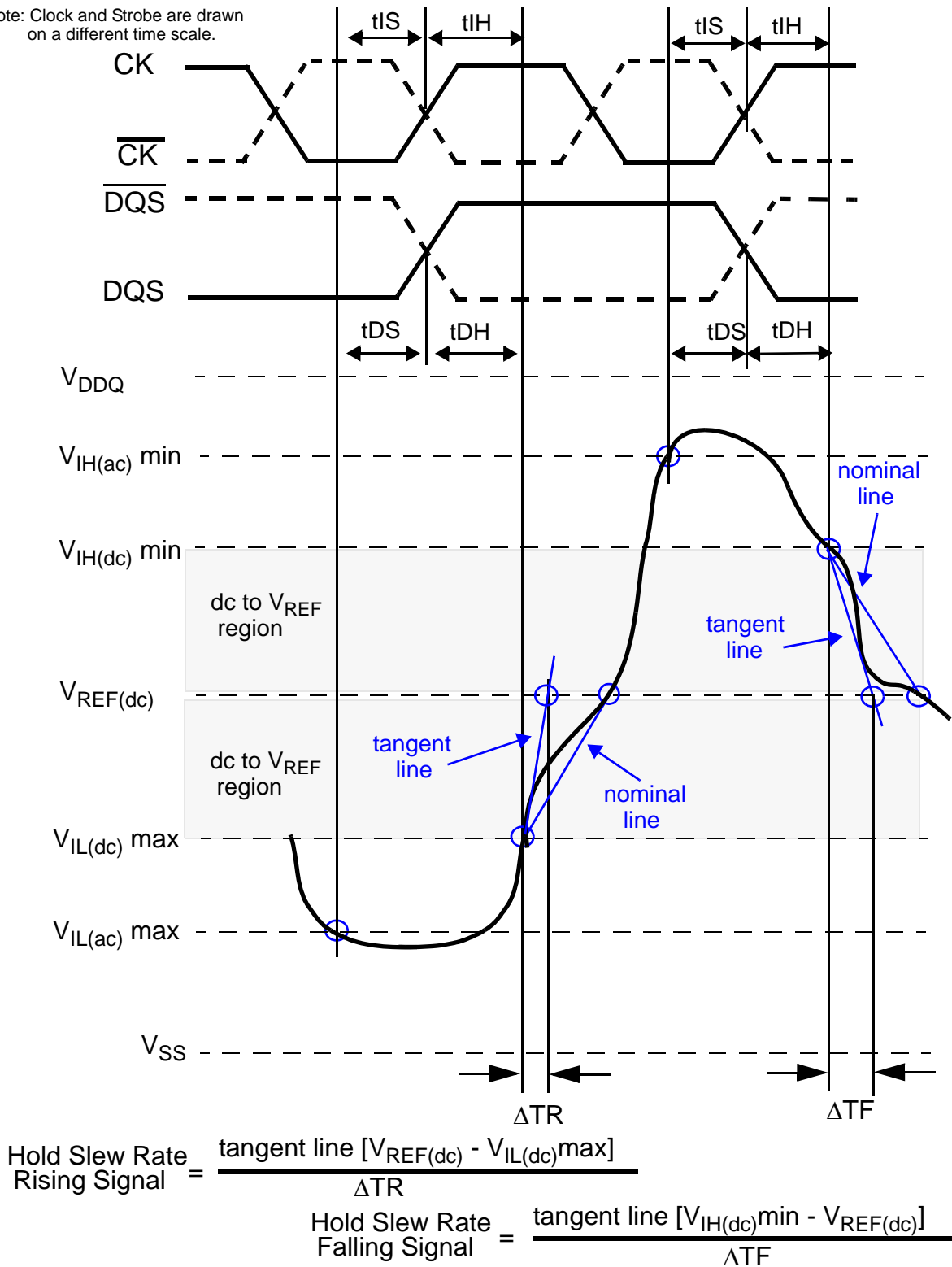
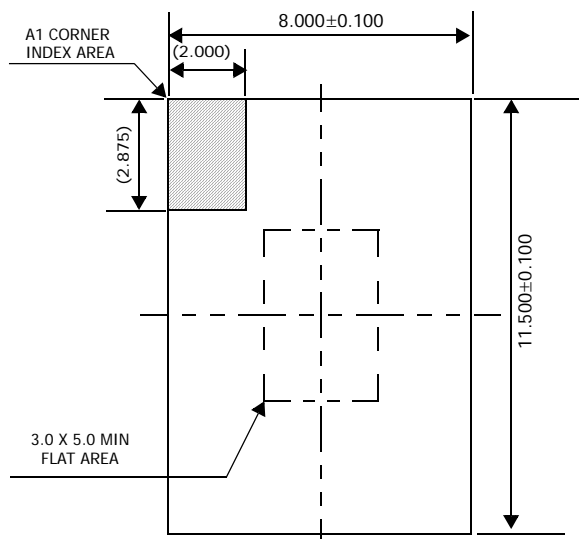


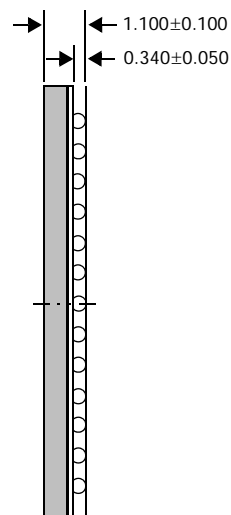
Figure 10 - Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

12. Package Dimensions

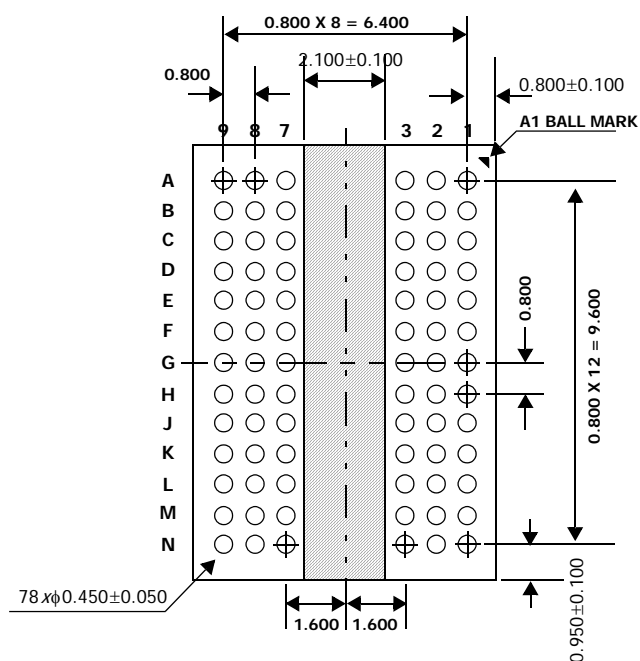
12.1 Package Dimension(x4/x8); 78Ball Fine Pitch Ball Grid Array Outline



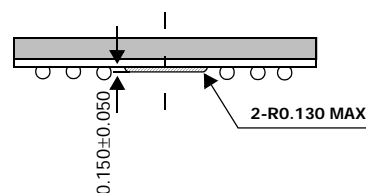
TOP VIEW



SIDE VIEW



BOTTOM VIEW



12.2 Package Dimension(x16); 96Ball Fine Pitch Ball Grid Array Outline

