

HAF2007(L), HAF2007(S)

Silicon N Channel MOS FET Series
Power Switching

REJ03G1137-0400
(Previous: ADE-208-706B)
Rev.4.00
Sep 07, 2005

Description

This FET has the over temperature shut-down capability sensing to the junction temperature.

This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

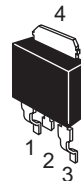
Features

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shut-down circuit
- Latch type shut-down operation (Need 0 voltage recovery)

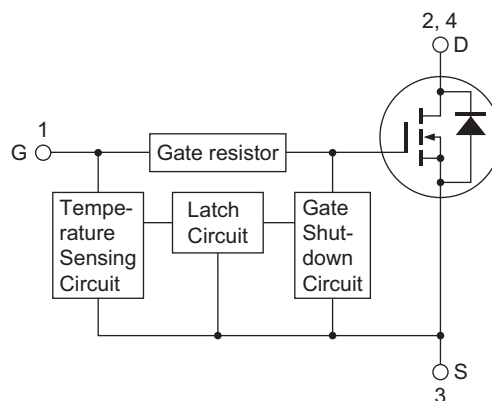
Outline

RENESAS Package code: PRSS0004ZD-B
(Package name: DPAK (L)-(2))

RENESAS Package code: PRSS0004ZD-C
(Package name: DPAK (S))



1. Gate
2. Drain
3. Source
4. Drain



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DS}	60	V
Gate to source voltage	V_{GS}	16	V
	V_{GS}	-2.5	V
Drain current	I_D	5	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	10	A
Body-drain diode reverse drain current	I_{DR}	5	A
Channel dissipation	P_{ch} ^{Note 2}	20	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. Value at $T_c = 25^\circ C$

Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	100	μA	$V_i = 8 V, V_{DS} = 0$
	I_{IH2}	—	—	50	μA	$V_i = 3.5 V, V_{DS} = 0$
	I_{IL}	—	—	1	μA	$V_i = 1.2 V, V_{DS} = 0$
Input current (Gate shut down)	$I_{IH(sd)1}$	—	0.8	—	mA	$V_i = 8 V, V_{DS} = 0$
	$I_{IH(sd)2}$	—	0.35	—	mA	$V_i = 3.5 V, V_{DS} = 0$
Shut down temperature	T_{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V_{OP}	3.5	—	12	V	

Electrical Characteristics

(Ta = 25°C)

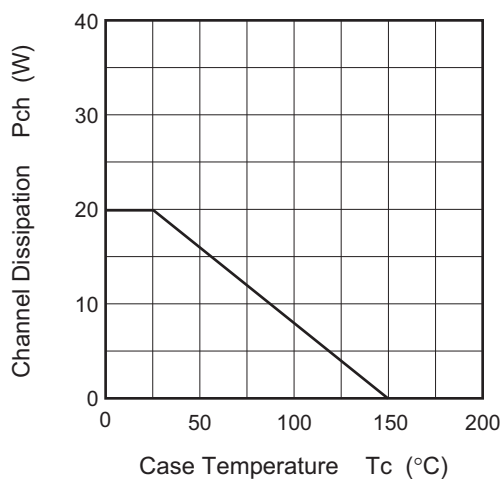
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	4	—	—	A	$V_{GS} = 3.5 \text{ V}$, $V_{DS} = 2 \text{ V}$
	I_{D2}	—	—	10	mA	$V_{GS} = 1.2 \text{ V}$, $V_{DS} = 2 \text{ V}$
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	16	—	—	V	$I_G = 300 \mu\text{A}$, $V_{DS} = 0$
	$V_{(BR)GSS}$	-2.5	—	—	V	$I_G = -100 \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS1}	—	—	100	μA	$V_{GS} = 8 \text{ V}$, $V_{DS} = 0$
	I_{GSS2}	—	—	50	μA	$V_{GS} = 3.5 \text{ V}$, $V_{DS} = 0$
	I_{GSS3}	—	—	1	μA	$V_{GS} = 1.2 \text{ V}$, $V_{DS} = 0$
	I_{GSS4}	—	—	-100	μA	$V_{GS} = -2.4 \text{ V}$, $V_{DS} = 0$
Input current (shut down)	$I_{GS(op)1}$	—	0.8	—	mA	$V_{GS} = 8 \text{ V}$, $V_{DS} = 0$
	$I_{GS(op)2}$	—	0.35	—	mA	$V_{GS} = 3.5 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 60 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}$
Forward transfer admittance	$ y_{fs} $	4	7.5	—	S	$I_D = 2.5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 3}
Static drain to source on state resistance	$R_{DS(on)}$	—	73	120	m Ω	$I_D = 2.5 \text{ A}$, $V_{GS} = 4 \text{ V}$ ^{Note 3}
	$R_{DS(on)}$	—	55	75	m Ω	$I_D = 2.5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 3}
Output capacitance	C_{OSS}	—	270	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$ $f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	2.8	—	μs	$I_D = 2.5 \text{ A}$ $V_{GS} = 5 \text{ V}$ $R_L = 12 \Omega$
Rise time	t_r	—	12.4	—	μs	
Turn-off delay time	$t_{d(off)}$	—	15	—	μs	
Fall time	t_f	—	11	—	μs	
Body-drain diode forward voltage	V_{DF}	—	0.9	—	V	$I_F = 5 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	140	—	ns	$I_F = 5 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu\text{s}$
Over load shut down operation time ^{Note4}	t_{OS1}	—	1.1	—	ms	$V_{GS} = 5 \text{ V}$, $V_{DD} = 16 \text{ V}$
	t_{OS2}	—	0.57	—	ms	$V_{GS} = 5 \text{ V}$, $V_{DD} = 24 \text{ V}$

Notes: 3. Pulse test

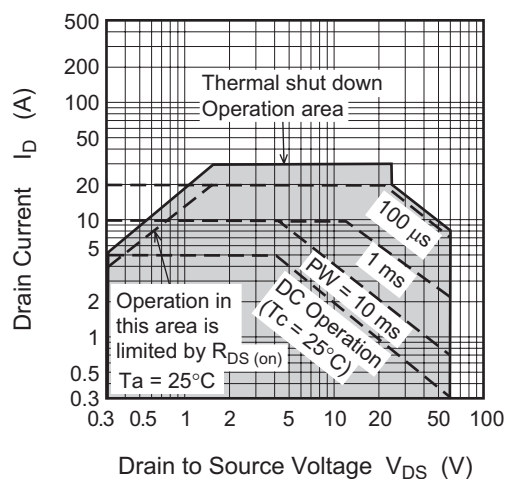
4. Including the junction temperature rise of the over loaded condition.

Main Characteristics

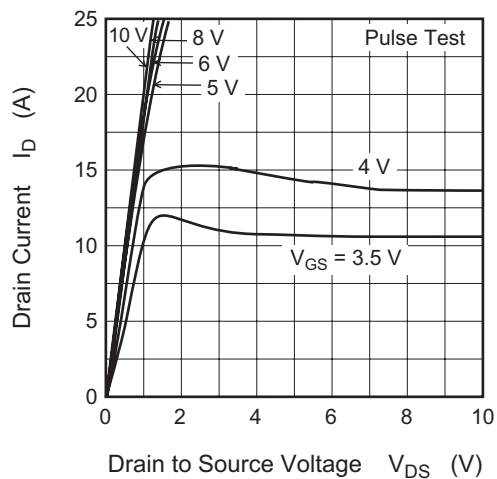
Power vs. Temperature Derating



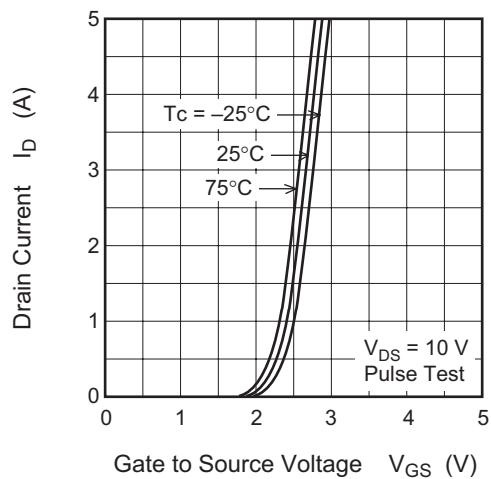
Maximum Safe Operation Area



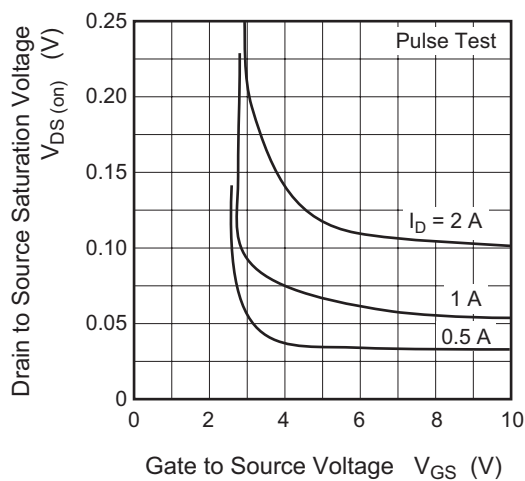
Typical Output Characteristics



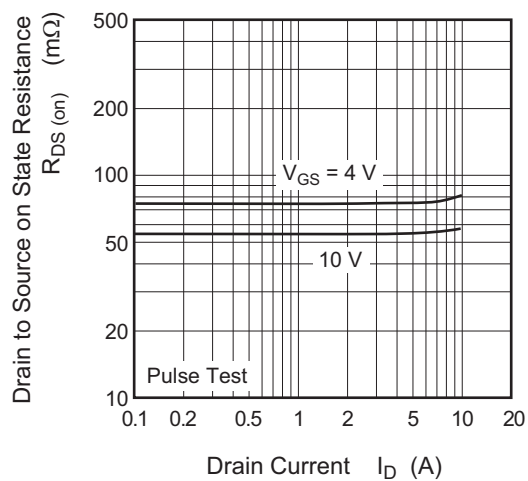
Typical Transfer Characteristics



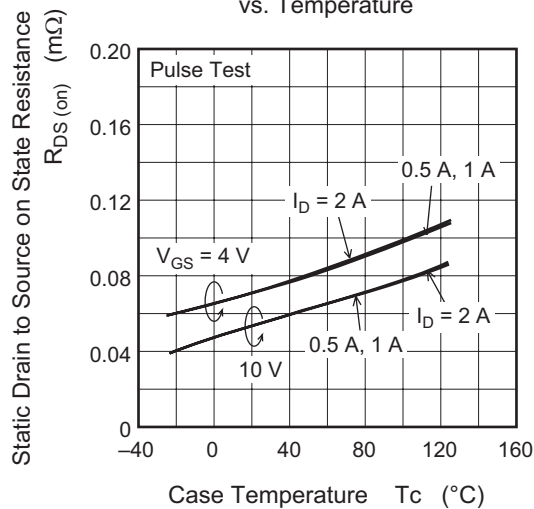
Drain to Source Saturation Voltage vs. Gate to Source Voltage



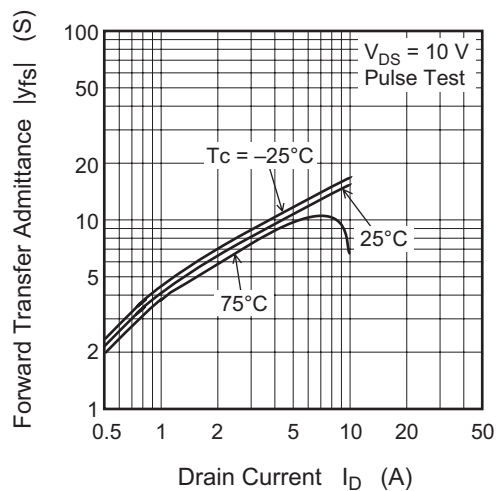
Static Drain to Source on State Resistance vs. Drain Current



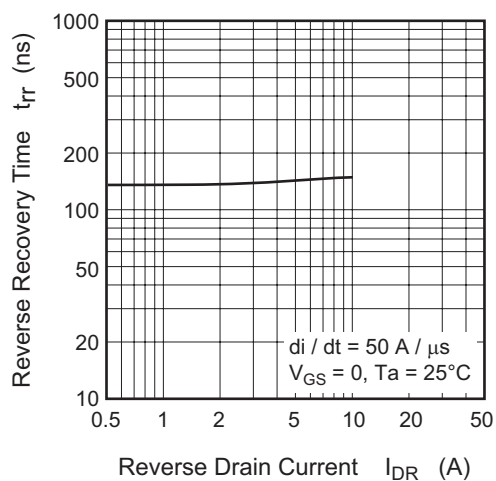
Static Drain to Source on State Resistance vs. Temperature



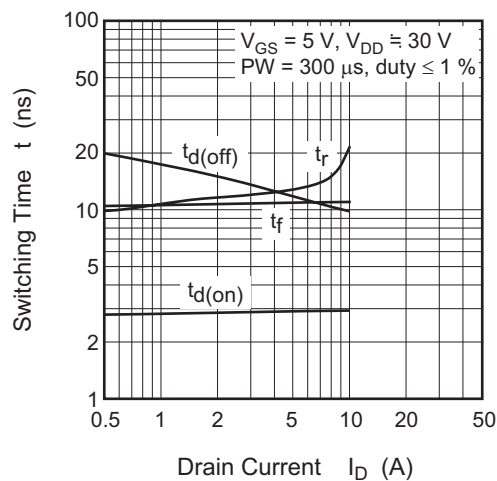
Forward Transfer Admittance vs. Drain Current



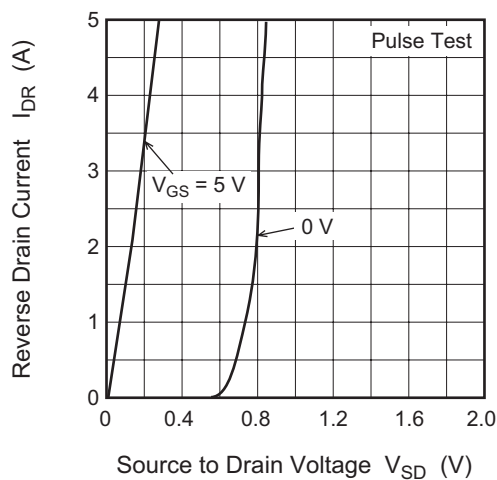
Body-Drain Diode Reverse Recovery Time



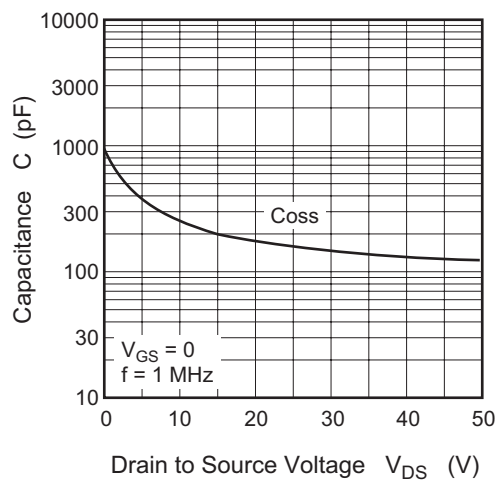
Switching Characteristics

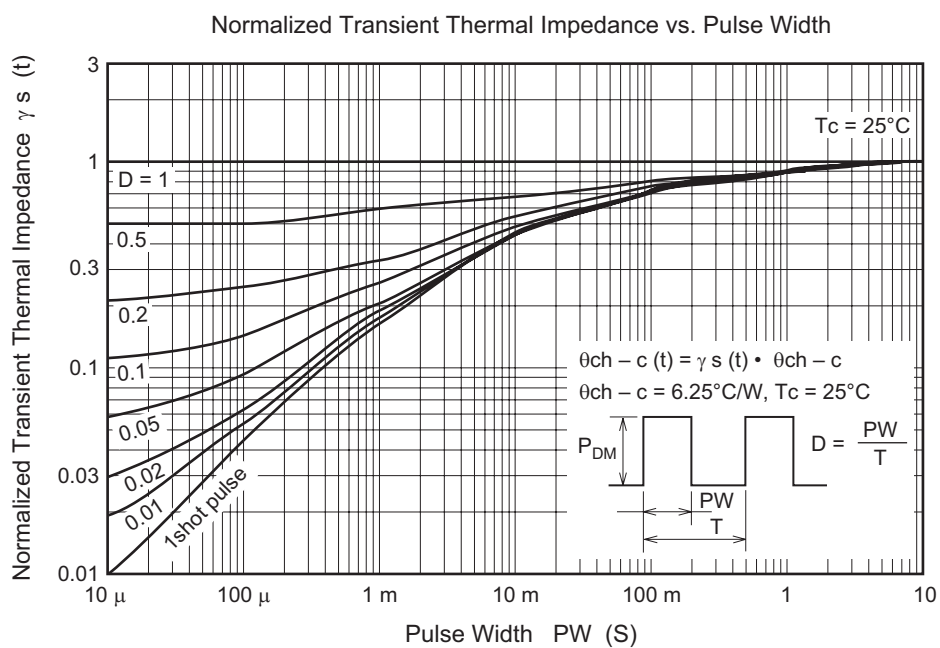
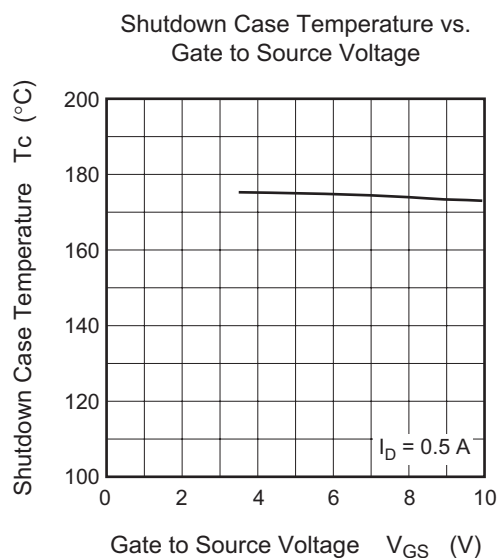
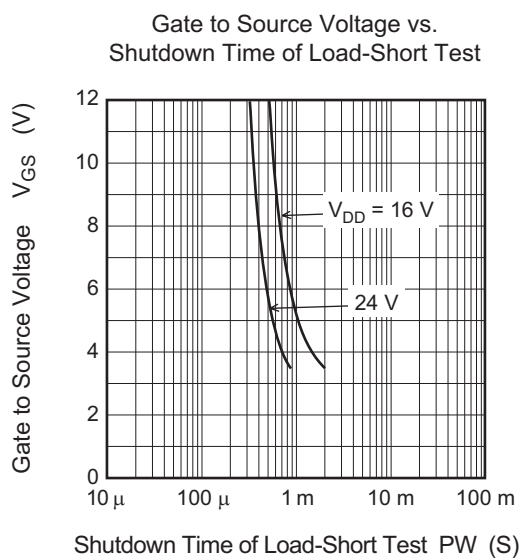


Reverse Drain Current vs. Source to Drain Voltage

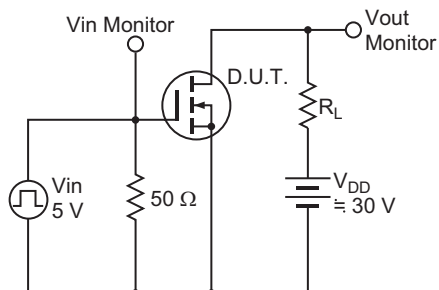


Typical Capacitance vs. Drain to Source Voltage

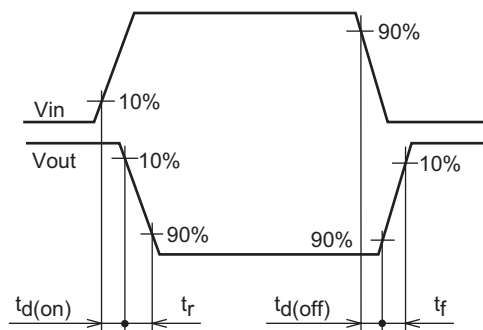




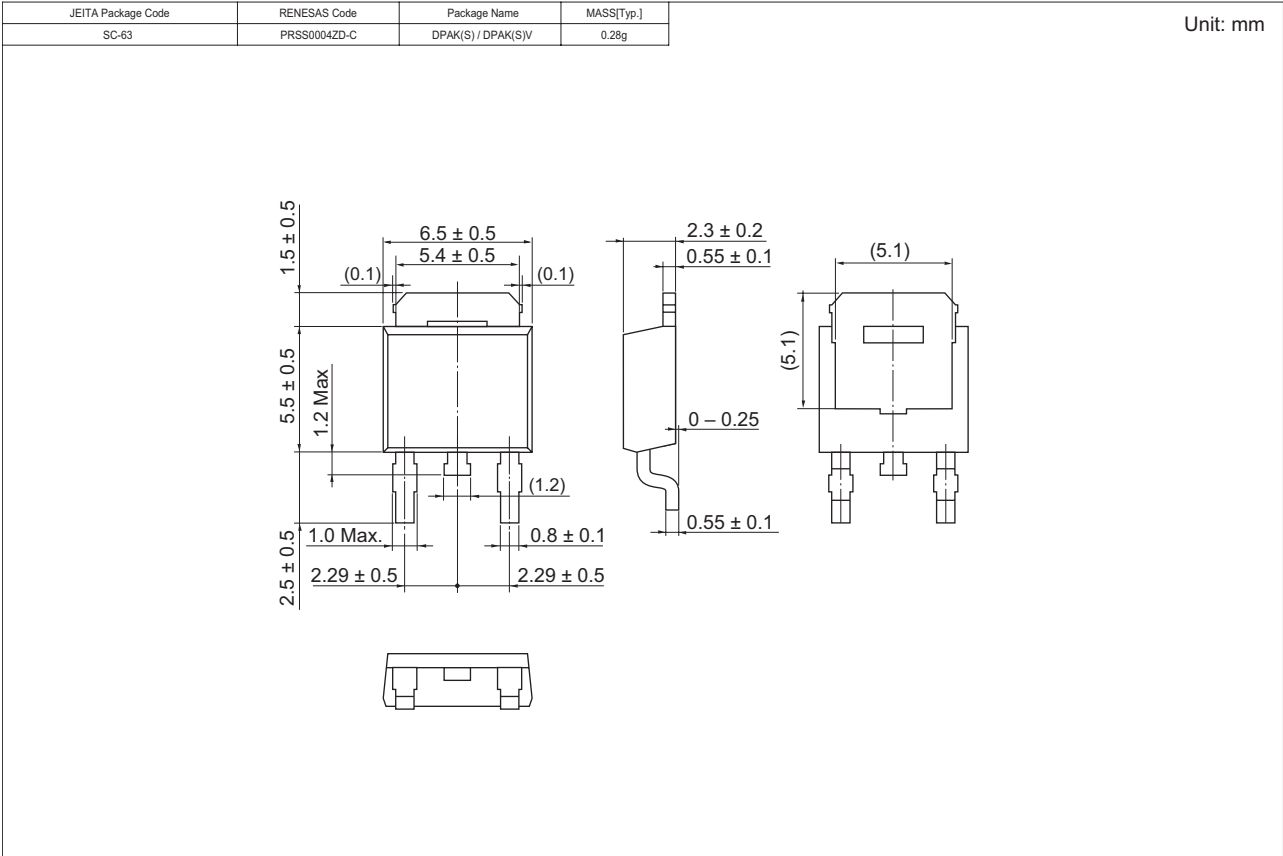
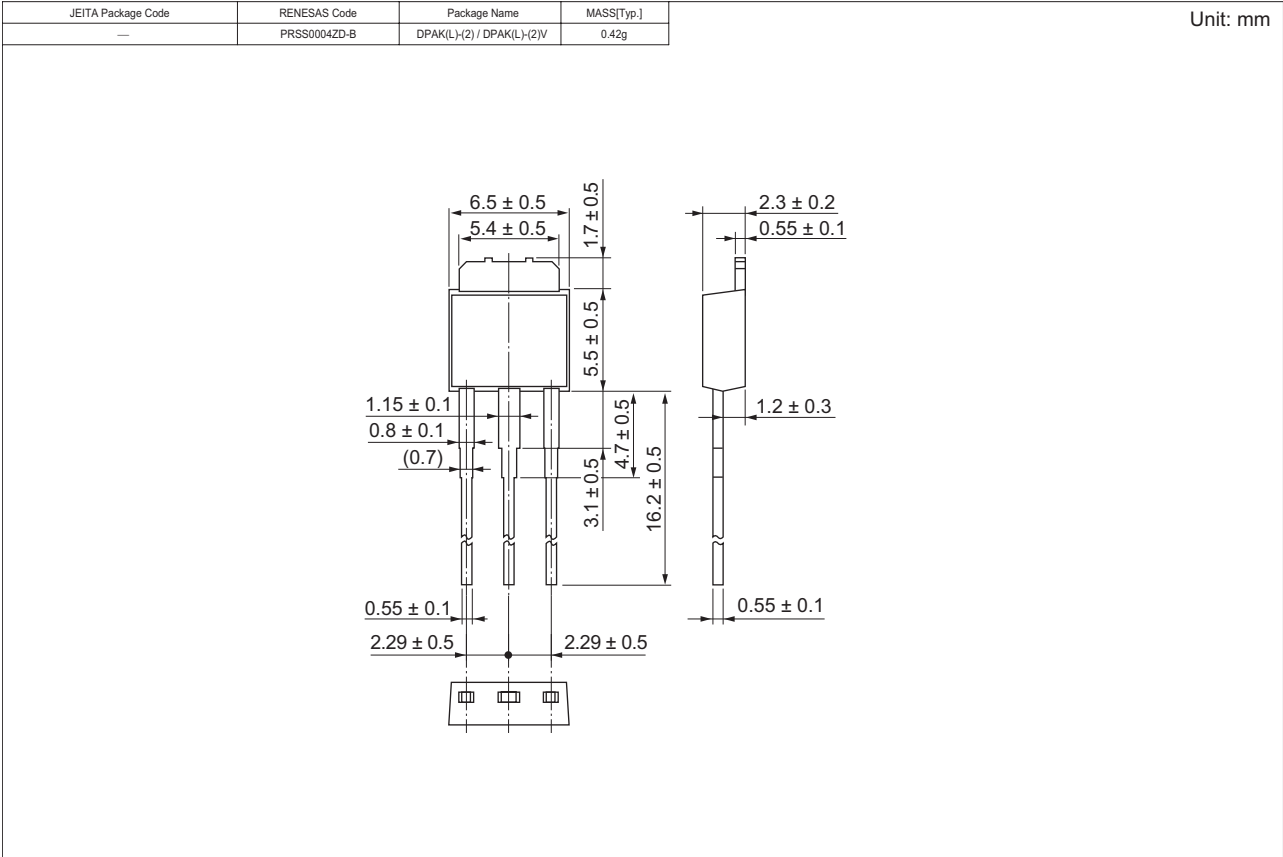
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAF2007-90L	Max: 100 pcs/sack	Sack
HAF2007-90S	Max: 100 pcs/sack	Sack
HAF2007-90STL	3000 pcs/Reel	Embossed tape
HAF2007-90STR	3000 pcs/Reel	Embossed tape

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