

HAT2142H

Silicon N Channel Power MOS FET Power Switching

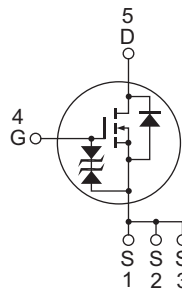
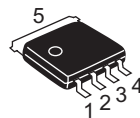
REJ03G1194-0700
(Previous: ADE-208-1583E)
Rev.7.00
Sep 07, 2005

Features

- Capable of 7 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 35 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LPAK)



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DS}	100	V
Gate to source voltage	V_{GS}	±20	V
Drain current	I_D	10	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	40	A
Body-drain diode reverse drain current	I_{DR}	10	A
Avalanche current	I_{AP} ^{Note 3}	10	A
Avalanche energy	E_{AR} ^{Note 3}	10	mJ
Channel dissipation	P_{ch} ^{Note 2}	15	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. $T_c = 25^\circ C$ 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

Electrical Characteristics

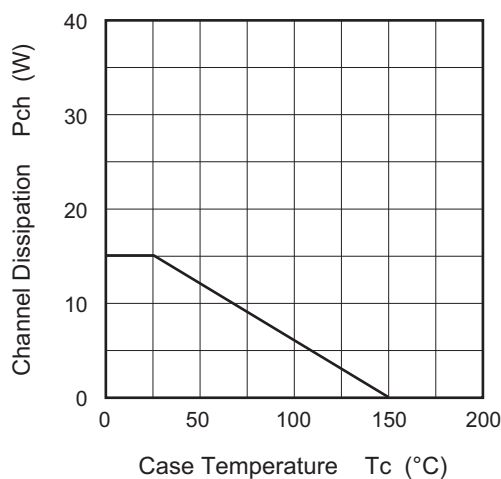
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	3.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	35	44	mΩ	$I_D = 5 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
	$R_{DS(on)}$	—	38	51	mΩ	$I_D = 5 \text{ A}$, $V_{GS} = 7 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	9	15	—	S	$I_D = 5 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	2000	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	175	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	90	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	32	—	nC	$V_{DD} = 50 \text{ V}$
Gate to source charge	Q_{gs}	—	8.0	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	7.5	—	nC	$I_D = 10 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	18	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 5 \text{ A}$
Rise time	t_r	—	11	—	ns	$V_{DD} \cong 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	60	—	ns	$R_L = 6 \Omega$
Fall time	t_f	—	9	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.82	1.07	V	$I_F = 10 \text{ A}$, $V_{GS} = 0$ ^{Note 4}
Body-drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 10 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu s$

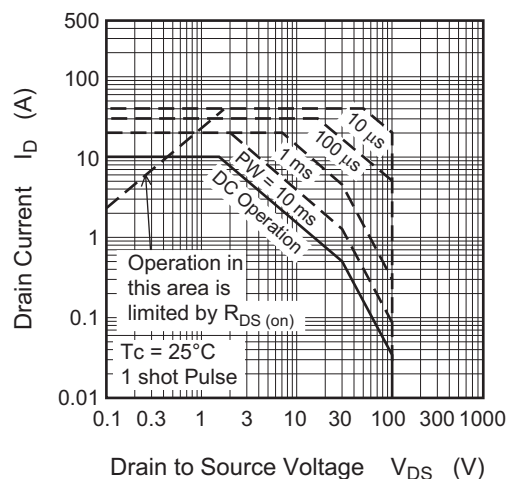
Note: 4. Pulse test

Main Characteristics

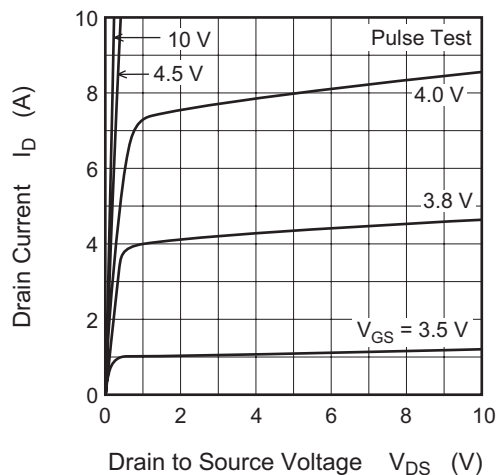
Power vs. Temperature Derating



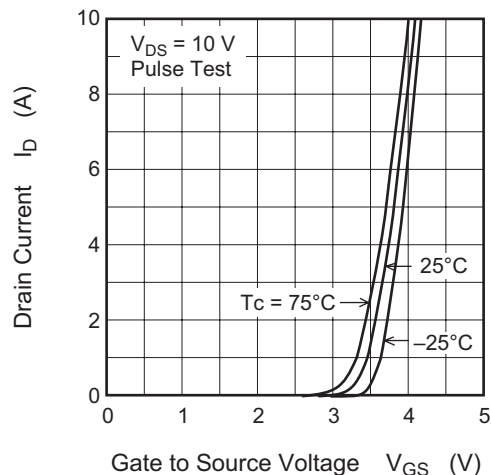
Maximum Safe Operation Area



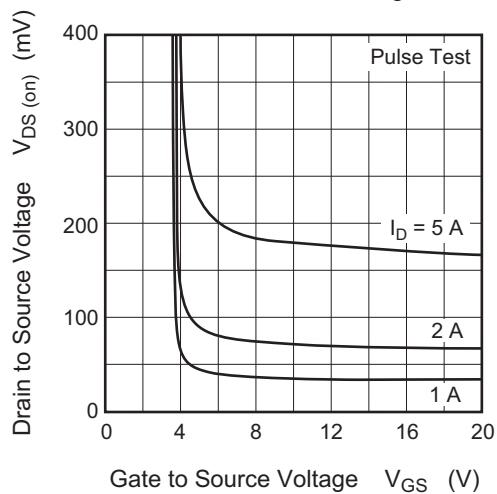
Typical Output Characteristics



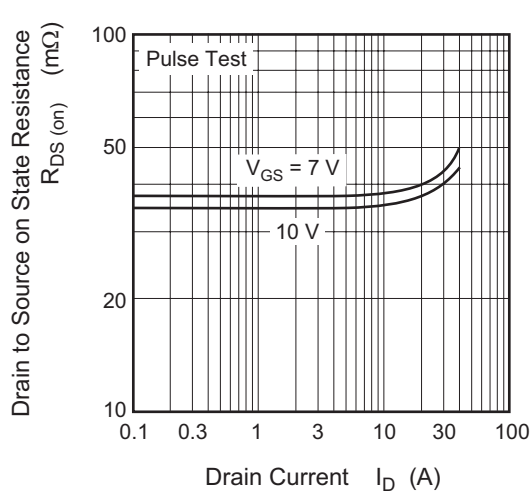
Typical Transfer Characteristics



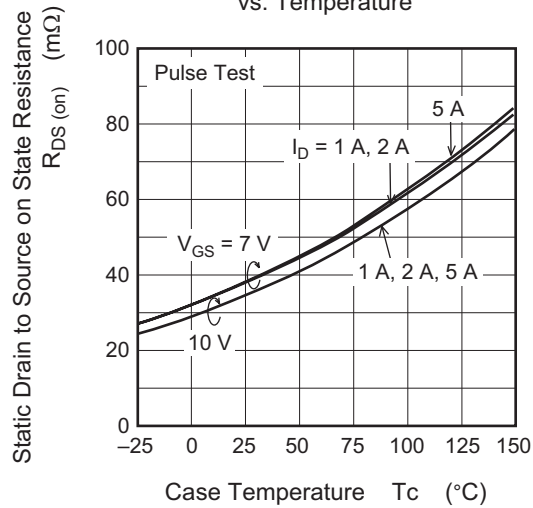
Drain to Source Saturation Voltage vs. Gate to Source Voltage



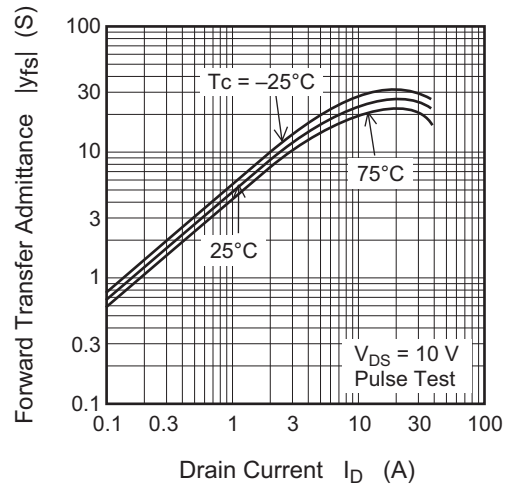
Static Drain to Source on State Resistance vs. Drain Current



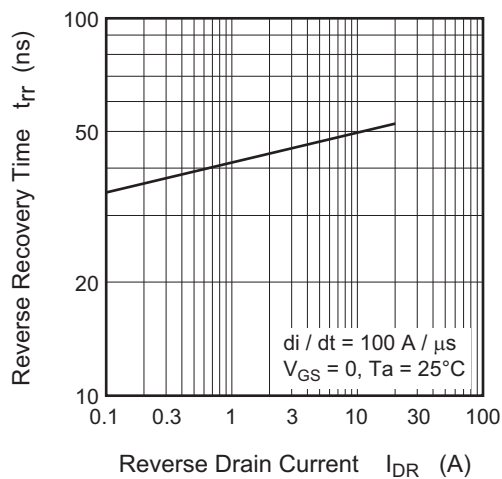
Static Drain to Source on State Resistance vs. Temperature



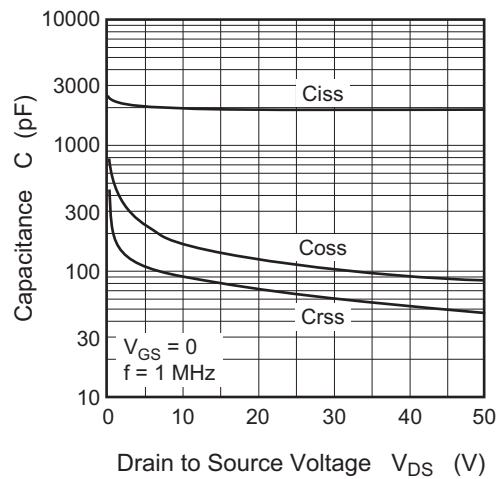
Forward Transfer Admittance vs. Drain Current



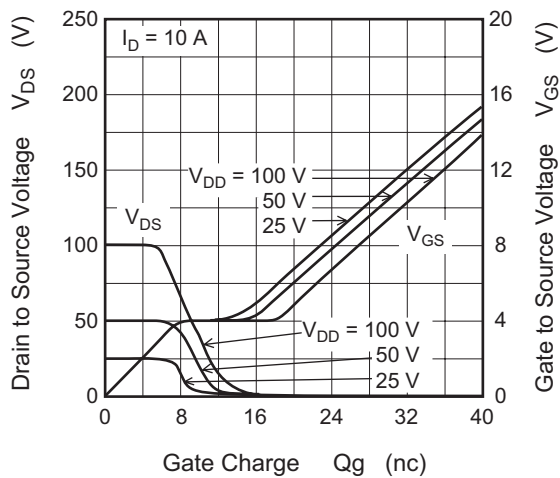
Body-Drain Diode Reverse Recovery Time



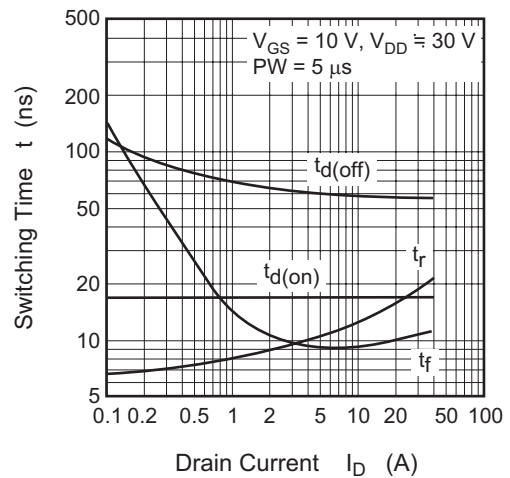
Typical Capacitance vs. Drain to Source Voltage

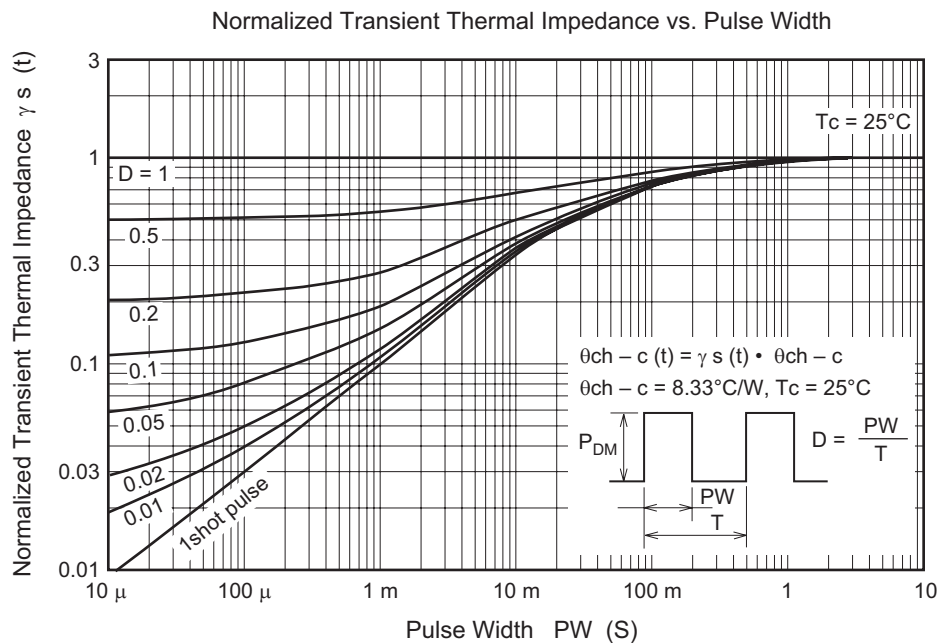
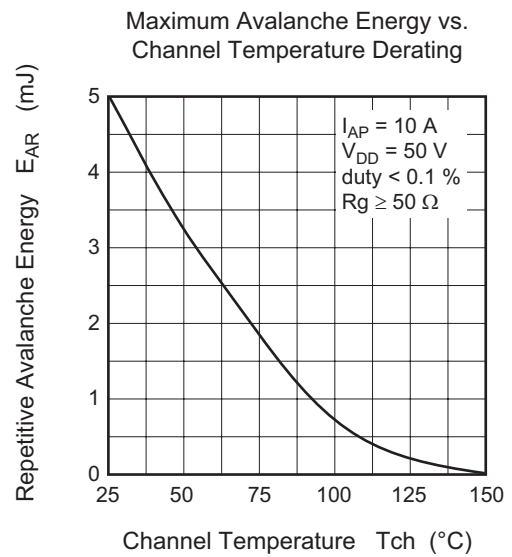
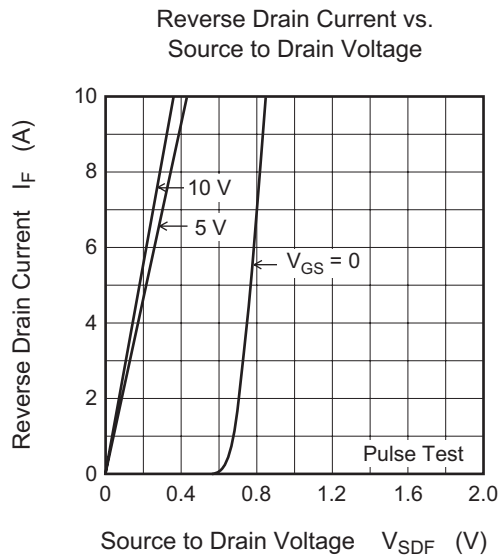


Dynamic Input Characteristics

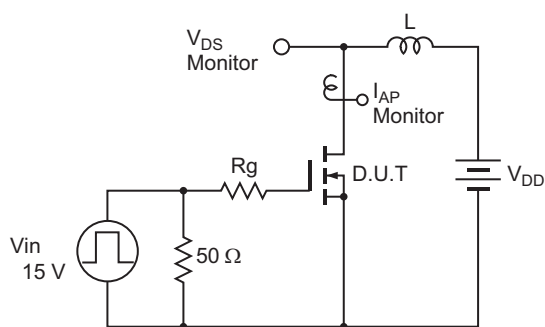


Switching Characteristics



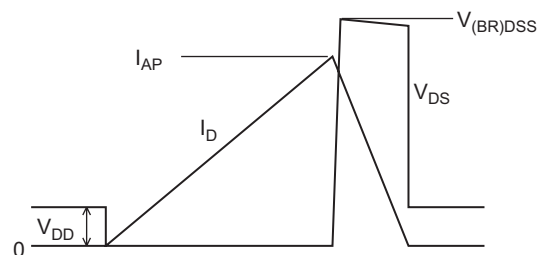


Avalanche Test Circuit

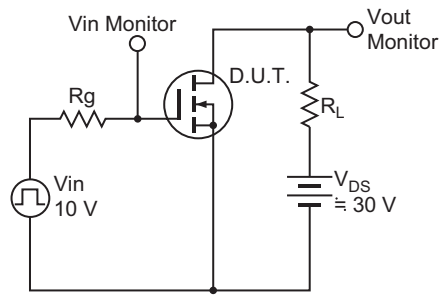


Avalanche Waveform

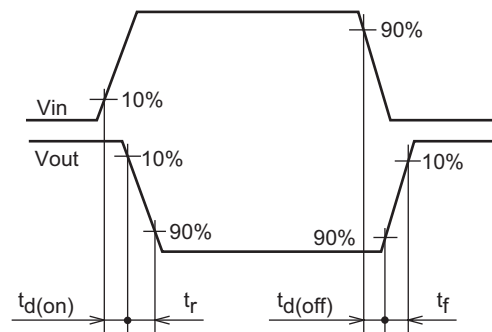
$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

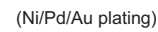


Switching Time Test Circuit



Switching Time Waveform



Unit: mm

Note: For some grades, production may be terminated. Please contact the Renesas sales office to check the state of production before ordering the product.

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Renesas Technology Europe Limited

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Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

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Renesas Technology Singapore Pte. Ltd.

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Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510