

HAT2143H

Silicon N Channel Power MOS FET Power Switching

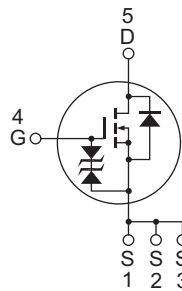
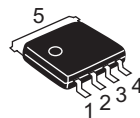
REJ03G1195-0300
(Previous: ADE-208-1584A)
Rev.3.00
Sep 07, 2005

Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 4.9 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

RENESAS Package code: PTZZ0005DA-A
(Package name: LFAK)



1, 2, 3 Source
4 Gate
5 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DS}	30	V
Gate to source voltage	V_{GS}	±20	V
Drain current	I_D	40	A
Drain peak current	$I_{D(pulse)}$ ^{Note 1}	160	A
Body-drain diode reverse drain current	I_{DR}	40	A
Avalanche current	I_{AP} ^{Note 3}	16	A
Avalanche energy	E_{AR} ^{Note 3}	25	mJ
Channel dissipation	P_{ch} ^{Note 2}	20	W
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$ 2. $T_c = 25^\circ C$ 3. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$

Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \mu A$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.9	6.1	mΩ	$I_D = 20 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note 4}
	$R_{DS(on)}$	—	7.9	11.5	mΩ	$I_D = 20 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note 4}
Forward transfer admittance	$ y_{fs} $	30	50	—	S	$I_D = 20 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	C_{iss}	—	2450	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	540	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	280	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Q_g	—	40	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	8	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	7	—	nC	$I_D = 40 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	20	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 20 \text{ A}$
Rise time	t_r	—	56	—	ns	$V_{DD} \cong 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	76	—	ns	$R_L = 0.5 \Omega$
Fall time	t_f	—	15	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.11	V	$I_F = 40 \text{ A}$, $V_{GS} = 0$ ^{Note 4}
Body-drain diode reverse recovery time	t_{rr}	—	60	—	ns	$I_F = 40 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 50 \text{ A}/\mu s$

Note: 4. Pulse test

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