

HAT2172N

Silicon N Channel Power MOS FET Power Switching

REJ03G1683-0100

Rev.1.00

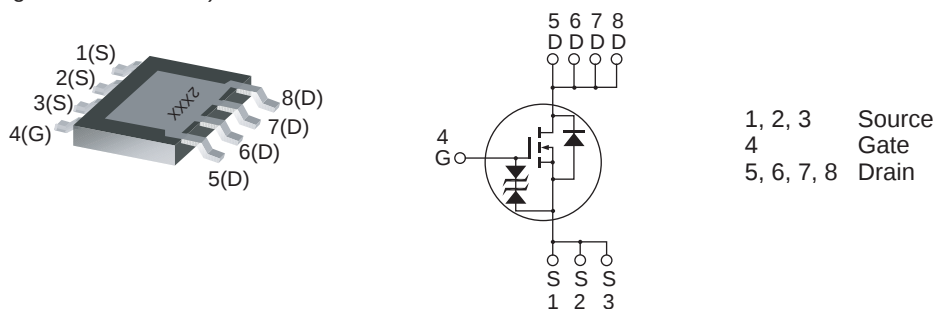
May 28, 2008

Features

- High speed switching
 - Capable of 7 V gate drive
 - Low drive current
 - High density mounting
 - Low on-resistance
- $R_{DS(on)} = 6.1 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)

Outline

RENESAS Package code: PTSP0008DC-A
(Package name: LFPAK-i)



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	40	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	30	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	120	A
Body-drain diode reverse drain current	I_{DR}	30	A
Avalanche current	I_{AP} ^{Note 2}	20	A
Avalanche energy	E_{AR} ^{Note 2}	20	mJ
Channel dissipation	P_{ch} ^{Note3}	20	W
Channel to case thermal resistance	θ_{ch-C}	6.25	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

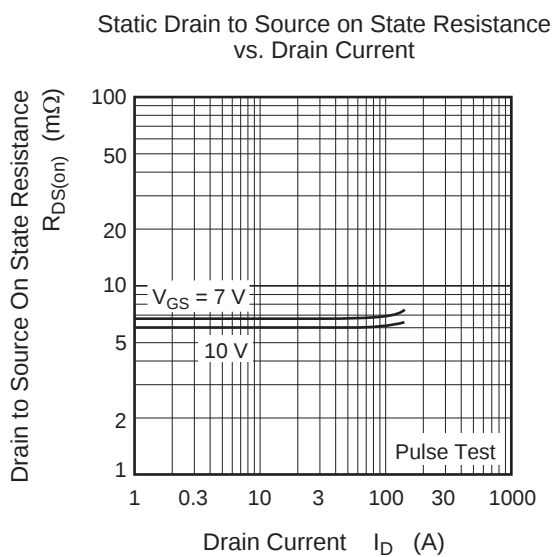
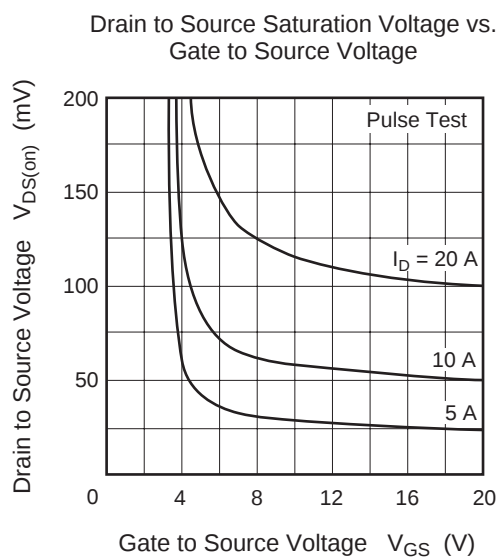
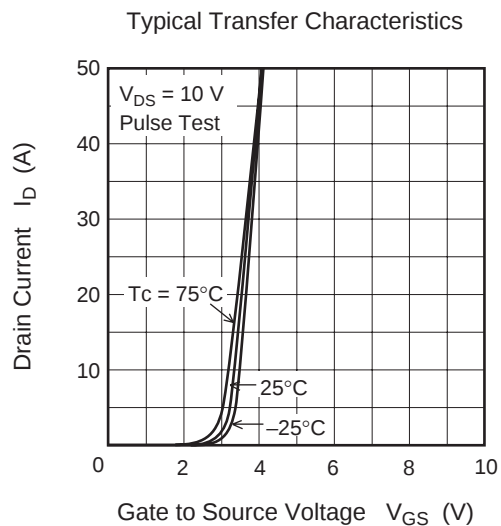
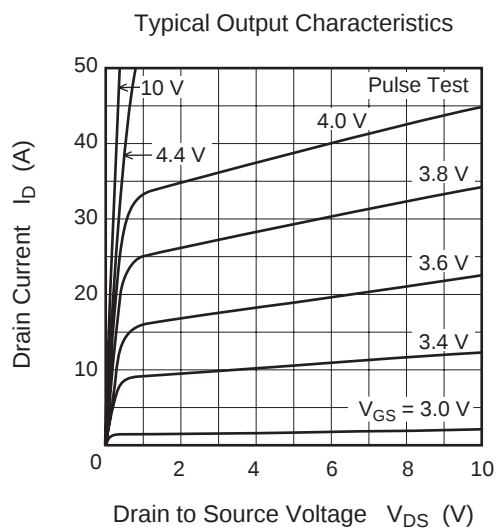
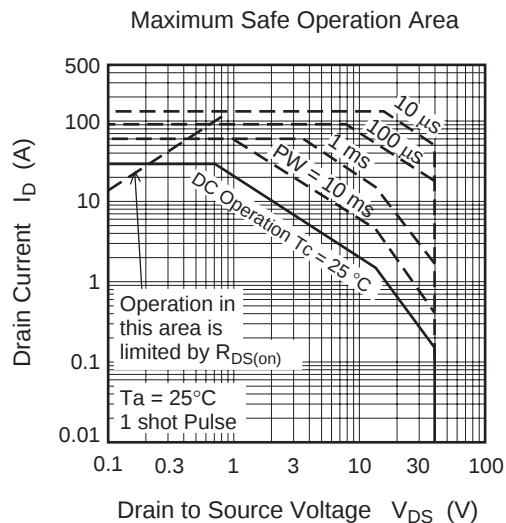
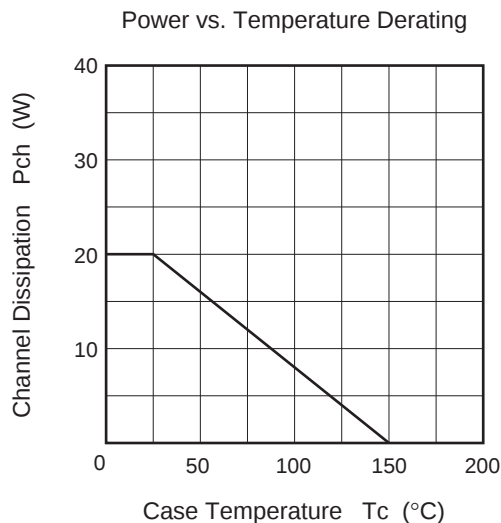
Electrical Characteristics

(Ta = 25°C)

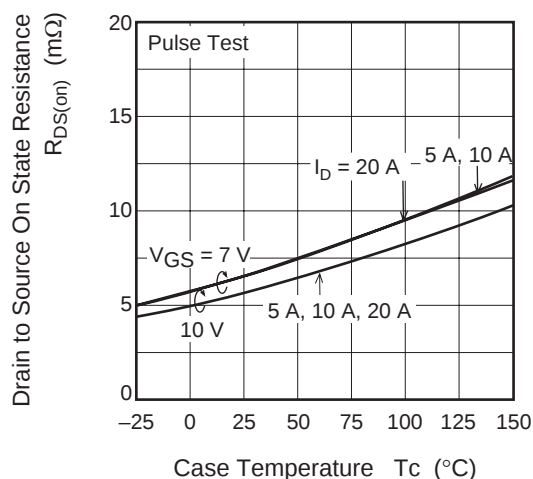
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	40	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 40 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.5	—	3.0	V	$V_{DS} = 10 \text{ V}$, $I_D = 10 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	6.1	7.8	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	6.9	9.5	$\text{m}\Omega$	$I_D = 15 \text{ A}$, $V_{GS} = 7 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	27	45	—	S	$I_D = 15 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	2420	—	pF	$V_{DS} = 10 \text{ V}$, $V_{GS} = 0$, $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	480	—	pF	
Reverse transfer capacitance	C_{rss}	—	150	—	pF	
Gate resistance	R_g	—	0.5	—	Ω	
Total gate charge	Q_g	—	32	—	nC	$V_{DD} = 10 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 30 \text{ A}$
Gate to source charge	Q_{gs}	—	9	—	nC	
Gate to drain charge	Q_{gd}	—	4.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 15 \text{ A}$, $V_{DD} \cong 10 \text{ V}$, $R_L = 0.67 \text{ }\Omega$, $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	20	—	ns	
Turn-off delay time	$t_{d(off)}$	—	38	—	ns	
Fall time	t_f	—	4.5	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.84	1.10	V	$I_F = 30 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	32	—	ns	$I_F = 30 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

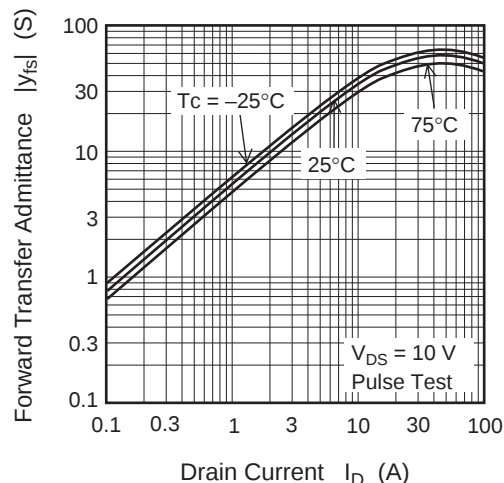
Main Characteristics



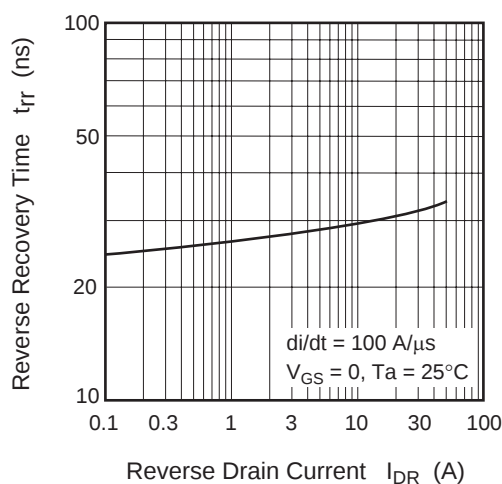
Static Drain to Source on State Resistance vs. Temperature



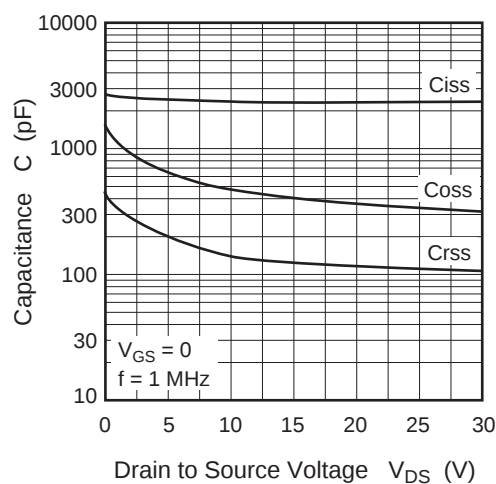
Forward Transfer Admittance vs. Drain Current



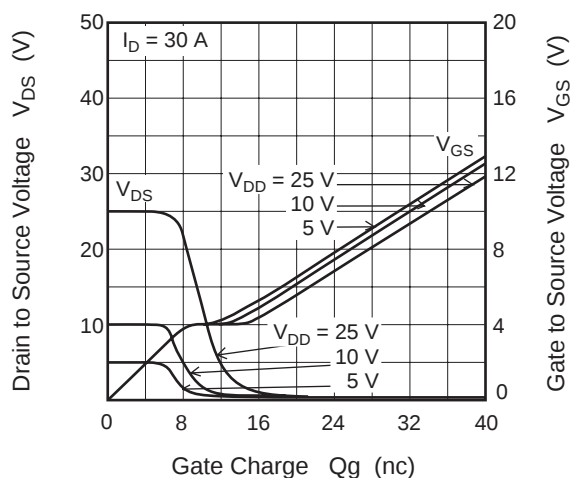
Body-Drain Diode Reverse Recovery Time



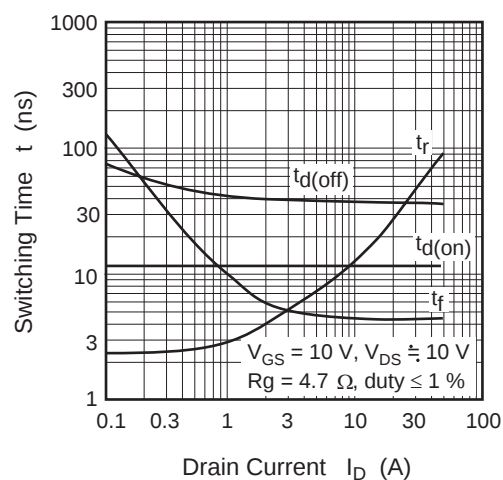
Typical Capacitance vs. Drain to Source Voltage

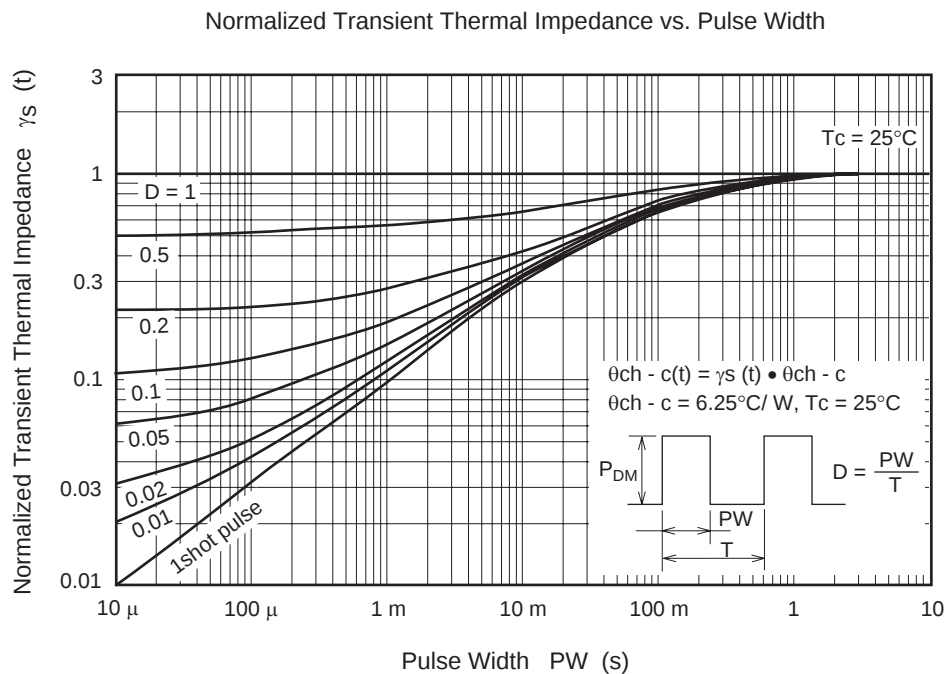
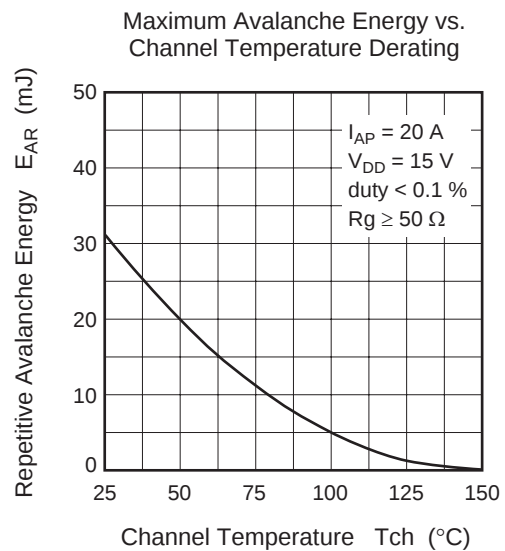
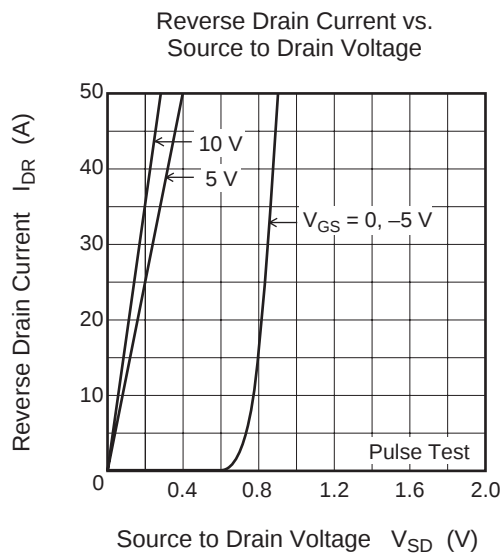


Dynamic Input Characteristics

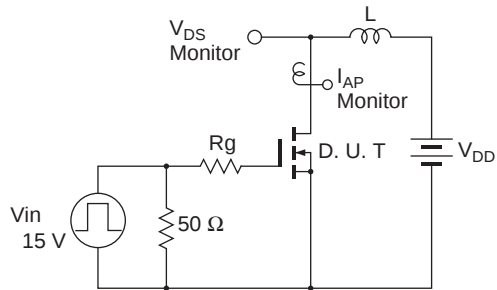


Switching Characteristics

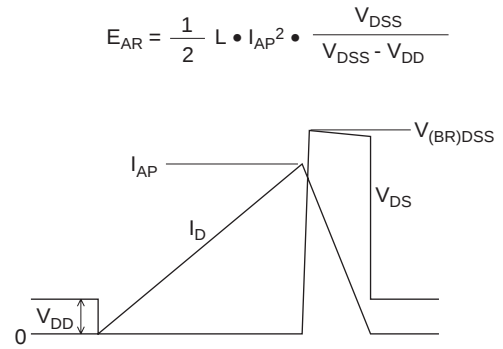




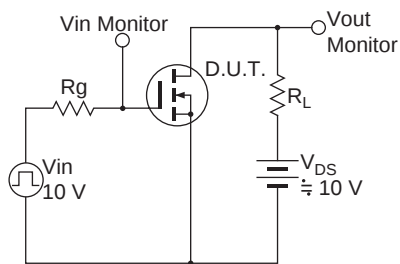
Avalanche Test Circuit



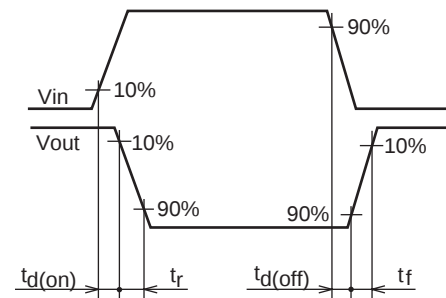
Avalanche Waveform



Switching Time Test Circuit



Switching Time Waveform



Notes:

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