

# HM64YLB36512 Series

16M Synchronous Late Write Fast Static RAM  
(512-kword  $\times$  36-bit)

REJ03C0270-0300

Rev.3.00

Jan.13.2006

## Description

The HM64YLB36512 is a synchronous fast static RAM organized as 512-kword  $\times$  36-bit. It has realized high speed access time by employing the most advanced CMOS process and high speed circuit designing technology. It is most appropriate for the application which requires high speed, high density memory and wide bit width configuration, such as cache and buffer memory in system. It is packaged in standard 119-bump BGA.

Note: All power supply and ground pins must be connected for proper operation of the device.

## Features

- 2.5 V  $\pm$  5% operation and 1.5 V ( $V_{DDQ}$ )
- 16M bit density
- Byte write control (4 byte write selects, one for each 9-bit)
- Optional  $\times 18$  configuration
- HSTL compatible I/O
- Programmable impedance output drivers
- Asynchronous  $\overline{G}$  output control
- Asynchronous sleep mode
- FC-BGA 119pin package with SRAM JEDEC standard pinout
- Limited set of boundary scan JTAG IEEE 1149.1 compatible
- Mode selectable among late write, associative late write (late select) and register-latch
- Late select mode:
  - Synchronous register to register operation
  - Late SAS select, selects which half of 72-bit core data to return on reads
  - SAS serves as way select
  - Differential HSTL clock inputs
- Late write mode:
  - Synchronous register to register operation
  - Differential HSTL clock inputs
- Register-latch mode:
  - Synchronous register to latch operation
  - Differential pseudo-HSTL clock inputs

## Ordering Information

Type No.	Organization	Modes	Access time	Cycle time	Package
HM64YLB36512BP-28	512k × 36	Late select mode Late write mode	1.6 ns	2.8 ns	119-bump 1.27 mm 14 mm × 22 mm BGA PRBG0119DB-A (BP-119E)
HM64YLB36512BP-33	512k × 36	Late select mode Late write mode	1.6 ns	3.3 ns	
		Register-latch mode	5.5 ns	6.5 ns	

Note: HM: Hitachi Memory prefix, 64: External Cache SRAM, Y:  $V_{DD} = 2.5\text{ V}$ , L: Dual Mode SRAM, B:  $V_{DDQ} = 1.5\text{ V}$

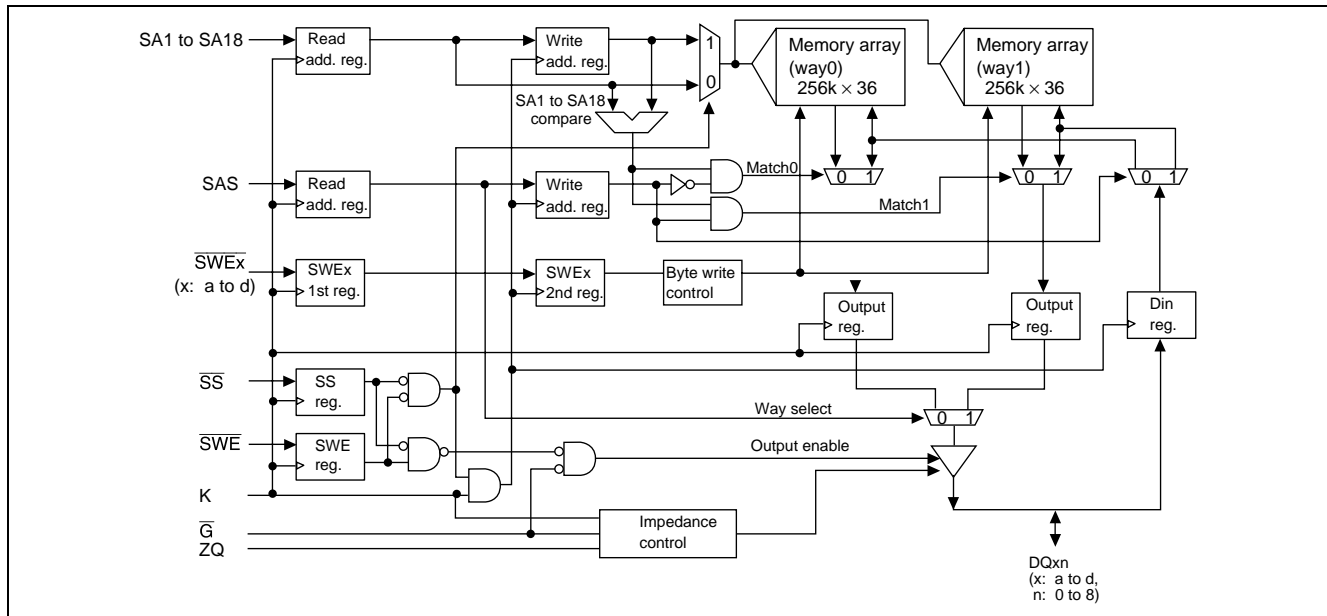
## Pin Arrangement

	1	2	3	4	5	6	7
A	$V_{DDQ}$	SA14	SA13	NC	SA6	SA7	$V_{DDQ}$
B	NC	SA15	SA12	NC	SA5	SA9	NC
C	NC	SA16	SA11	$V_{DD}$	SA4	SA8	NC
D	DQc7	DQc8	$V_{SS}$	ZQ	$V_{SS}$	DQb8	DQb7
E	DQc5	DQc6	$V_{SS}$	$\overline{SS}$	$V_{SS}$	DQb6	DQb5
F	$V_{DDQ}$	DQc4	$V_{SS}$	$\overline{G}$	$V_{SS}$	DQb4	$V_{DDQ}$
G	DQc3	DQc2	$\overline{SWEc}$	NC	$\overline{SWEb}$	DQb2	DQb3
H	DQc1	DQc0	$V_{SS}$	NC	$V_{SS}$	DQb0	DQb1
J	$V_{DDQ}$	$V_{DD}$	$V_{REF}$	$V_{DD}$	$V_{REF}$	$V_{DD}$	$V_{DDQ}$
K	DQd1	DQd0	$V_{SS}$	K	$V_{SS}$	DQa0	DQa1
L	DQd3	DQd2	$\overline{SWEd}$	$\overline{K}$	$\overline{SWEa}$	DQa2	DQa3
M	$V_{DDQ}$	DQd4	$V_{SS}$	SWE	$V_{SS}$	DQa4	$V_{DDQ}$
N	DQd5	DQd6	$V_{SS}$	SA17	$V_{SS}$	DQa6	DQa5
P	DQd7	DQd8	$V_{SS}$	SAS/SA0	$V_{SS}$	DQa8	DQa7
R	NC	SA10	M1	$V_{DD}$	M2	SA1	NC
T	NC	NC	SA18	SA3	SA2	NC	ZZ
U	$V_{DDQ}$	TMS	TDI	TCK	TDO	NC	$V_{DDQ}$

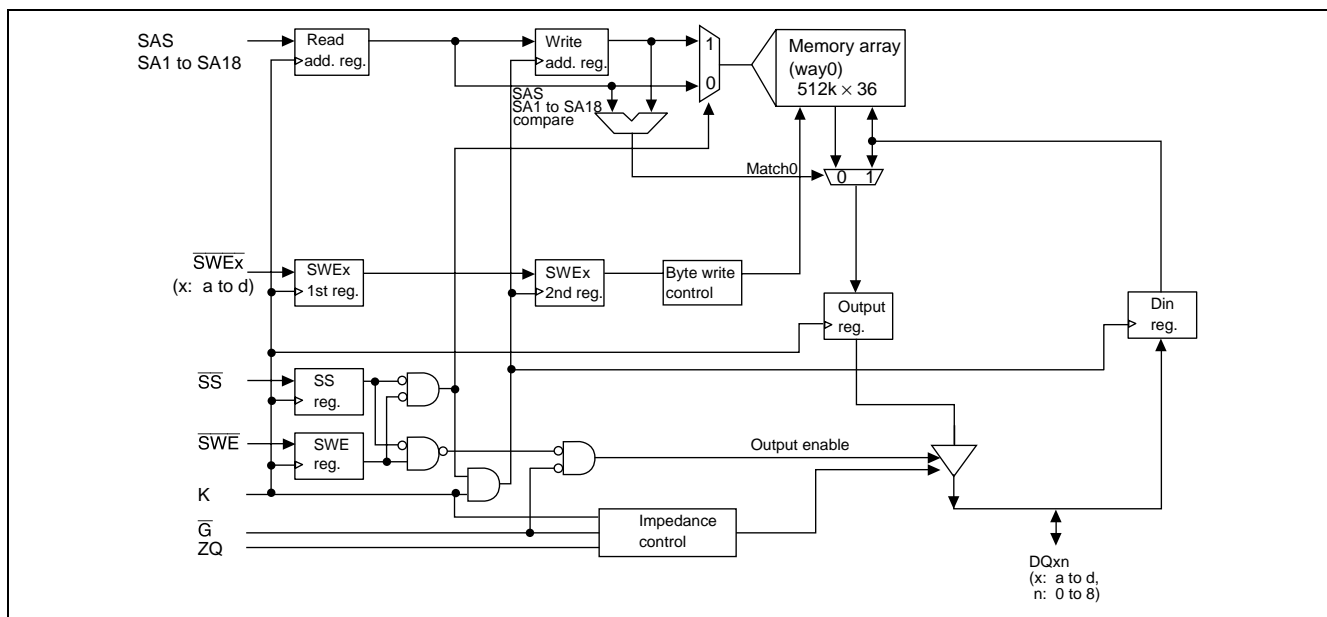
(Top view)

Note: 4P pin is SAS in both the late select mode and the late write mode, or is SA0 in the register-latch mode.

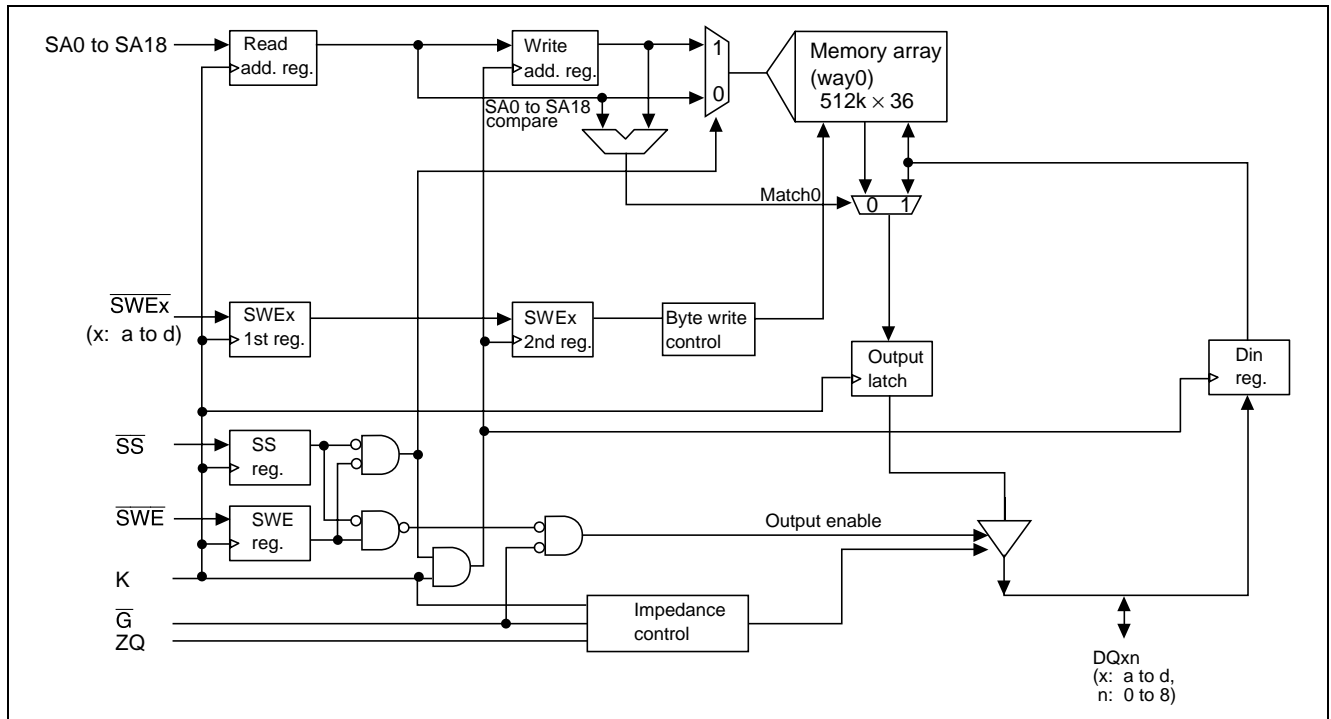
## Block Diagram (Late Select Mode)



## Block Diagram (Late Write Mode)



## Block Diagram (Register-Latch Mode)



## Pin Descriptions

Name	I/O type	Descriptions	Notes
V <sub>DD</sub>	Supply	Core power supply	
V <sub>SS</sub>	Supply	Ground	
V <sub>DDQ</sub>	Supply	Output power supply	
V <sub>REF</sub>	Supply	Input reference, provides input reference voltage	
K	Input	Clock input, active high	
$\bar{K}$	Input	Clock input, active low	
$\bar{SS}$	Input	Synchronous chip select	
SWE	Input	Synchronous write enable	
SAn	Input	Synchronous address input	n: 1 to 18 (Late select mode) (Late write mode) n: 0 to 18 (Register-latch mode)
SAS	Input	Late select: Synchronous way select Late write: Synchronous address input	SA0 in the register-latch mode
SWEx	Input	Synchronous byte write enables	x: a to d
$\bar{G}$	Input	Asynchronous output enable	
ZZ	Input	Power down mode select	
ZQ	Input	Output impedance control	1
DQxn	I/O	Synchronous data input/output	x: a to d n: 0 to 8
M1, M2	Input	Output protocol mode select	
TMS	Input	Boundary scan test mode select	
TCK	Input	Boundary scan test clock	
TDI	Input	Boundary scan test data input	
TDO	Output	Boundary scan test data output	
NC	—	No connection	

M1	M2	Protocol	Notes
V <sub>SS</sub>	V <sub>SS</sub>	Synchronous register to register operation (late select mode)	2
V <sub>SS</sub>	V <sub>DD</sub>	Synchronous register to register operation (late write mode)	3
V <sub>DD</sub>	V <sub>SS</sub>	Synchronous register to latch operation (register-latch mode)	2

- Notes:
1. ZQ is to be connected to V<sub>SS</sub> via a resistance R<sub>Q</sub> where  $175\ \Omega \leq R_Q \leq 300\ \Omega$ . If ZQ = V<sub>DDQ</sub> or open, output buffer impedance will be maximum.
  2. Mode control pins M1 and M2 are used to select different read protocols. These mode control input pins are set at power-up and will not change the states during the SRAM operates.  
Late select mode: Single clock, late SAS select, pipelined read protocol  
Late write mode: Single clock, pipelined read protocol  
Register-latch mode: Single differential clock register-latch mode protocol
  3. Mode control pin M2 can be set to V<sub>DDQ</sub> instead of V<sub>DD</sub>.

## Truth Table

ZZ	SS	G	SWE	SWEa	SWEb	SWEc	SWE $\bar{d}$	K	R	Operation	Late select mode Late write mode		Register-latch mode	
											DQ (n)	DQ (n+1)	DQ (n)	DQ (n+1)
H	x	x	x	x	x	x	x	x	x	Sleep mode	High-Z	High-Z	High-Z	High-Z
L	H	x	x	x	x	x	x	L-H	H-L	Dead (not selected)	x	High-Z	High-Z	x
L	x	H	H	x	x	x	x	x	x	Dead (dummy read)	High-Z	x	High-Z	High-Z
L	L	L	H	x	x	x	x	L-H	H-L	Read	x	D <sub>OUT</sub> (a, b, c, d) 0 to 8	D <sub>OUT</sub> (a, b, c, d) 0 to 8	x
L	L	x	L	L	L	L	L	L-H	H-L	Write a, b, c, d byte	High-Z	D <sub>IN</sub> (a, b, c, d) 0 to 8	High-Z	D <sub>IN</sub> (a, b, c, d) 0 to 8
L	L	x	L	H	L	L	L	L-H	H-L	Write b, c, d byte	High-Z	D <sub>IN</sub> (b, c, d) 0 to 8	High-Z	D <sub>IN</sub> (b, c, d) 0 to 8
L	L	x	L	L	H	L	L	L-H	H-L	Write a, c, d byte	High-Z	D <sub>IN</sub> (a, c, d) 0 to 8	High-Z	D <sub>IN</sub> (a, c, d) 0 to 8
L	L	x	L	L	L	H	L	L-H	H-L	Write a, b, d byte	High-Z	D <sub>IN</sub> (a, b, d) 0 to 8	High-Z	D <sub>IN</sub> (a, b, d) 0 to 8
L	L	x	L	L	L	L	H	L-H	H-L	Write a, b, c byte	High-Z	D <sub>IN</sub> (a, b, c) 0 to 8	High-Z	D <sub>IN</sub> (a, b, c) 0 to 8
L	L	x	L	H	H	L	L	L-H	H-L	Write c, d byte	High-Z	D <sub>IN</sub> (c, d) 0 to 8	High-Z	D <sub>IN</sub> (c, d) 0 to 8
L	L	x	L	L	H	H	L	L-H	H-L	Write a, d byte	High-Z	D <sub>IN</sub> (a, d) 0 to 8	High-Z	D <sub>IN</sub> (a, d) 0 to 8
L	L	x	L	L	L	H	H	L-H	H-L	Write a, b byte	High-Z	D <sub>IN</sub> (a, b) 0 to 8	High-Z	D <sub>IN</sub> (a, b) 0 to 8
L	L	x	L	H	L	L	H	L-H	H-L	Write b, c byte	High-Z	D <sub>IN</sub> (b, c) 0 to 8	High-Z	D <sub>IN</sub> (b, c) 0 to 8
L	L	x	L	H	H	H	L	L-H	H-L	Write d byte	High-Z	D <sub>IN</sub> (d) 0 to 8	High-Z	D <sub>IN</sub> (d) 0 to 8
L	L	x	L	H	H	L	H	L-H	H-L	Write c byte	High-Z	D <sub>IN</sub> (c) 0 to 8	High-Z	D <sub>IN</sub> (c) 0 to 8
L	L	x	L	H	L	H	H	L-H	H-L	Write b byte	High-Z	D <sub>IN</sub> (b) 0 to 8	High-Z	D <sub>IN</sub> (b) 0 to 8
L	L	x	L	L	H	H	H	L-H	H-L	Write a byte	High-Z	D <sub>IN</sub> (a) 0 to 8	High-Z	D <sub>IN</sub> (a) 0 to 8

Notes: 1. H: V<sub>IH</sub>, L: V<sub>IL</sub>, x: V<sub>IH</sub> or V<sub>IL</sub>2. SWE, SS, SWEa to SWE $\bar{d}$ , SA and SAS are sampled at the rising edge of K clock.

## Programmable Impedance Output Drivers

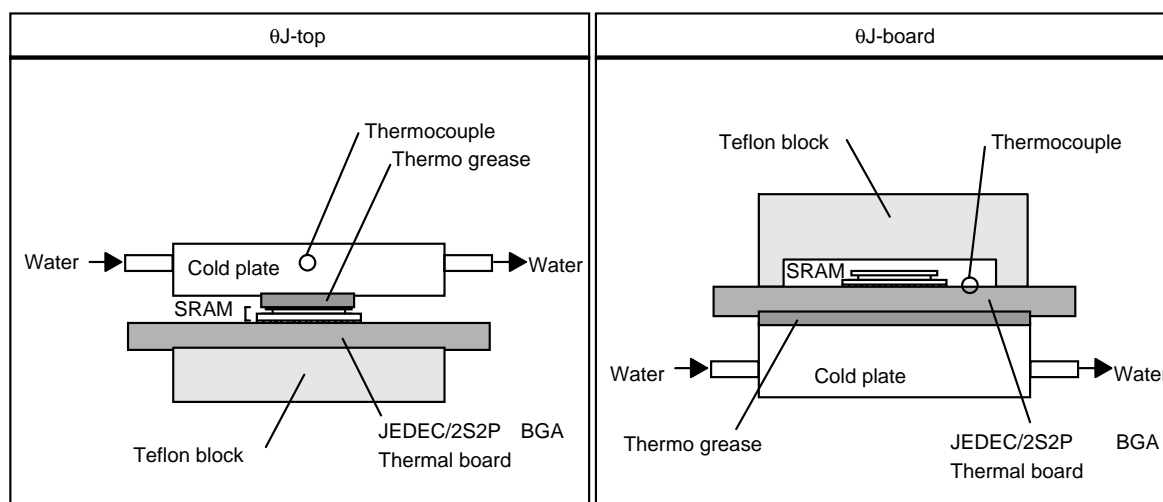
Output buffer impedance can be programmed by terminating the ZQ pin to  $V_{SS}$  through a precision resistor ( $R_Q$ ). The value of  $R_Q$  is five times the output impedance desired. The allowable value of  $R_Q$  to guarantee impedance matching with a tolerance of 15% is 250  $\Omega$ . If the status of ZQ pin is open, output impedance is maximum value. Maximum impedance also occurs with ZQ connected to  $V_{DDQ}$ . The impedance update of the output driver occurs when the SRAM is in high-Z. Write and deselect operations will synchronously switch the SRAM into and out of high-Z, therefore will trigger an update. At power up, the output buffer is in high-Z. It will take 4,096 cycles for the impedance to be completely updated.

## Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Input voltage on any pin	$V_{IN}$	-0.5 to $V_{DDQ} + 0.5$	V	1, 4
Core supply voltage	$V_{DD}$	-0.5 to +3.13	V	1
Output supply voltage	$V_{DDQ}$	-0.5 to +2.1	V	1, 4
Operating temperature	$T_{OPR}$	0 to +85	°C	
Storage temperature	$T_{STG}$	-55 to +125	°C	
Output short-circuit current	$I_{OUT}$	25	mA	
Latch up current	$I_{LI}$	200	mA	
Package junction to top thermal resistance	$\theta_{J-top}$	6.5	°C/W	5
Package junction to board thermal resistance	$\theta_{J-board}$	12	°C/W	5

Notes: 1. All voltage is referenced to  $V_{SS}$ .

- Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted the operation conditions. Exposure to higher voltages than recommended voltages for extended periods of time could affect device reliability.
- These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.
- The following supply voltage application sequence is recommended:  $V_{SS}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$  then  $V_{IN}$ . Remember, according to the absolute maximum ratings table,  $V_{DDQ}$  is not to exceed 2.1 V, whatever the instantaneous value of  $V_{DDQ}$ .
- See figure below.



Note: The following DC and AC specifications shown in the tables, this device is tested under the minimum transverse air flow exceeding 500 linear feet per minute.

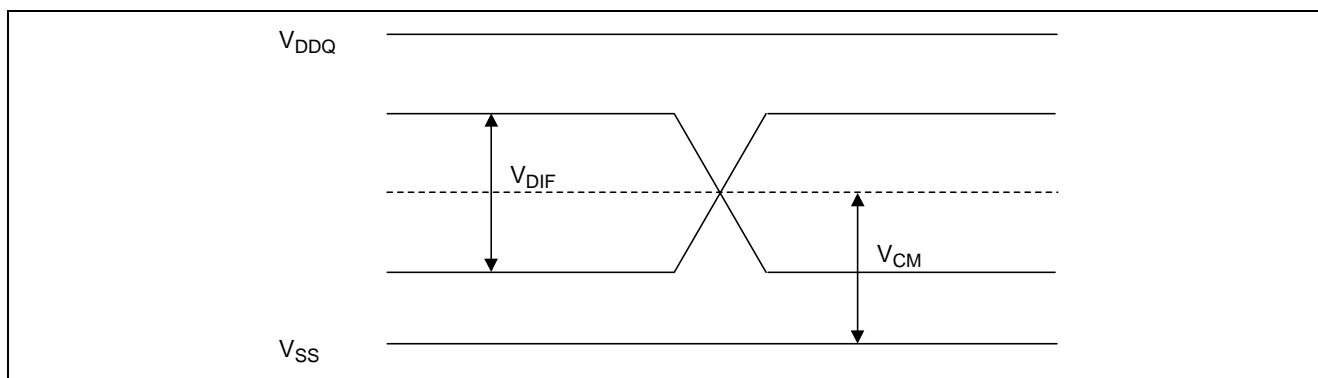
## Recommended DC Operating Conditions

(Ta = 0 to +85°C)

Parameter	Symbol	Late select mode Late write mode			Register-latch mode			Unit	Notes
		Min	Typ	Max	Min	Typ	Max		
Power supply voltage: core	V <sub>DD</sub>	2.38	2.50	2.63	2.38	2.50	2.63	V	
Power supply voltage: I/O	V <sub>DDQ</sub>	1.40	1.50	1.60	1.40	1.50	1.60	V	
Input reference voltage: I/O	V <sub>REF</sub>	0.60	0.75	0.90	0.70	0.75	0.80	V	1
Input high voltage	V <sub>IH</sub>	V <sub>REF</sub> + 0.10	—	V <sub>DDQ</sub> + 0.30	V <sub>REF</sub> + 0.15	—	V <sub>DDQ</sub> + 0.50	V	4
Input low voltage	V <sub>IL</sub>	−0.30	—	V <sub>REF</sub> − 0.10	−0.50	—	V <sub>REF</sub> − 0.15	V	4
Clock differential voltage	V <sub>DIF</sub>	0.10	—	V <sub>DDQ</sub> + 0.30	0.10	—	V <sub>DDQ</sub> + 0.30	V	2, 3
Clock common mode voltage	V <sub>CM</sub>	0.60	—	0.90	0.90	—	1.30	V	3

- Notes: 1. Peak to peak AC component superimposed on V<sub>REF</sub> may not exceed 5% of V<sub>REF</sub>.  
2. Minimum differential input voltage required for differential input clock operation.  
3. See figure below.  
4. V<sub>REF</sub> = 0.75 V (typ).

## Differential Voltage / Common Mode Voltage





## DC Characteristics

(Ta = 0 to +85°C, V<sub>DD</sub> = 2.5 V ± 5%)

Parameter	Symbol	Late select mode Late write mode		Register-latch mode		Unit	Notes
		Min	Max	Min	Max		
Input leakage current	I <sub>LI</sub>	—	2	—	2	μA	1
Output leakage current	I <sub>LO</sub>	—	5	—	5	μA	2
Standby current	I <sub>SBZZ</sub>	—	150	—	150	mA	3
V <sub>DD</sub> operating current, excluding output drivers	I <sub>DD</sub>	—	450	—	350	mA	4
Quiescent active power supply current	I <sub>DD2</sub>	—	200	—	200	mA	5
Maximum power dissipation, including output drivers	P	—	2.3	—	2.3	W	6

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output low voltage	V <sub>OL</sub>	V <sub>SS</sub>	—	V <sub>SS</sub> + 0.4	V	7
Output high voltage	V <sub>OH1</sub>	V <sub>DDQ</sub> - 0.4	—	V <sub>DDQ</sub>	V	8
	V <sub>OH2</sub>	1.3	—	V <sub>DDQ</sub>	V	12
ZQ pin connect resistance	RQ	—	250	—	Ω	
Output "Low" current	I <sub>OL</sub>	(V <sub>DDQ</sub> /2) / {(RQ/5) - 15%}		(V <sub>DDQ</sub> /2) / {(RQ/5) + 15%}	mA	9, 11
Output "High" current	I <sub>OH</sub>	(V <sub>DDQ</sub> /2) / {(RQ/5) + 15%}		(V <sub>DDQ</sub> /2) / {(RQ/5) - 15%}	mA	10, 11

- Notes: 1.  $0 \leq V_{IN} \leq V_{DDQ}$  for all input pins (except V<sub>REF</sub>, ZQ, M1, M2 pin)
2.  $0 \leq V_{OUT} \leq V_{DDQ}$ , DQ in high-Z
3. All inputs (except clock) are held at either V<sub>IH</sub> or V<sub>IL</sub>, ZZ is held at V<sub>IH</sub>, I<sub>OUT</sub> = 0 mA. Specification is guaranteed at +75°C junction temperature.
4. I<sub>OUT</sub> = 0 mA, read 50% / write 50%, V<sub>DD</sub> = V<sub>DD</sub> max, frequency = min. cycle
5. I<sub>OUT</sub> = 0 mA, read 50% / write 50%, V<sub>DD</sub> = V<sub>DD</sub> max, frequency = 3 MHz
6. Output drives a 12 pF load and switches every cycle. This parameter should be used by the SRAM designer to determine electrical and package requirements for the SRAM device.
7. RQ = 250 Ω, I<sub>OL</sub> = 6.8 mA
8. RQ = 250 Ω, I<sub>OH</sub> = -6.8 mA
9. Measured at V<sub>OL</sub> = 1/2 V<sub>DDQ</sub>
10. Measured at V<sub>OH</sub> = 1/2 V<sub>DDQ</sub>
11. The total external capacitance of ZQ pin must be less than 7.5 pF.
12. RQ = 250 Ω, I<sub>OH</sub> = -100 μA

## AC Characteristics

(Ta = 0 to +85°C, V<sub>DD</sub> = 2.5 V ± 5%)

## Late Select Mode, Late Write Mode

Parameter	Symbol	HM64YLB36512BP				Unit	Notes
		-28		-33			
		Min	Max	Min	Max		
CK clock cycle time	t <sub>KHKH</sub>	2.8	—	3.3	—	ns	
CK clock high width	t <sub>KHKL</sub>	1.2	—	1.3	—	ns	
CK clock low width	t <sub>KLKH</sub>	1.2	—	1.3	—	ns	
Address setup time	t <sub>AVKH</sub>	0.3	—	0.3	—	ns	2
Data setup time	t <sub>DVKH</sub>	0.3	—	0.3	—	ns	2
Address hold time	t <sub>KHAX</sub>	0.6	—	0.6	—	ns	
Data hold time	t <sub>KHDX</sub>	0.6	—	0.6	—	ns	
Clock high to output valid	t <sub>KHQV</sub>	—	1.6	—	1.6	ns	1
Clock high to output hold	t <sub>KHQX</sub>	0.65	—	0.65	—	ns	1, 6
Clock high to output low-Z ( $\overline{SS}$ control)	t <sub>KHQX2</sub>	0.65	—	0.65	—	ns	1, 4, 6
Clock high to output high-Z	t <sub>KHQZ</sub>	0.65	2.0	0.65	2.0	ns	1, 3, 6
Output enable low to output low-Z	t <sub>GLQX</sub>	0.1	—	0.1	—	ns	1, 4, 6
Output enable low to output valid	t <sub>GLQV</sub>	—	2.0	—	2.0	ns	1, 4
Output enable high to output high-Z	t <sub>GHQZ</sub>	—	2.0	—	2.0	ns	1, 3
Sleep mode recovery time	t <sub>ZZR</sub>	20.0	—	20.0	—	ns	5
Sleep mode enable time	t <sub>ZZE</sub>	—	15.0	—	15.0	ns	1, 3, 5

## Register-Latch Mode

Parameter	Symbol	HM64YLB36512BP		Unit	Notes
		-33			
		Min	Max		
CK clock cycle time	t <sub>KHKH</sub>	6.5	—	ns	
CK clock high width	t <sub>KHKL</sub>	1.2	—	ns	
CK clock low width	t <sub>KLKH</sub>	1.2	—	ns	
Address setup time	t <sub>AVKH</sub>	0.4	—	ns	2
Data setup time	t <sub>DVKH</sub>	0.4	—	ns	2
Address hold time	t <sub>KHAX</sub>	1.0	—	ns	
Data hold time	t <sub>KHDX</sub>	1.0	—	ns	
Clock high to output valid	t <sub>KHQV</sub>	1.7	5.5	ns	1
Clock low to output valid	t <sub>KLQV</sub>	0.5	2.3	ns	
Clock low to output hold	t <sub>KLQX</sub>	0.5	—	ns	
Clock low to output low-Z ( $\overline{SS}$ control)	t <sub>KLQX2</sub>	0.5	—	ns	1, 4, 6
Clock high to output high-Z	t <sub>KHQZ</sub>	0.5	2.3	ns	1, 3, 6
Output enable low to output low-Z	t <sub>GLQX</sub>	0.1	—	ns	1, 4, 6
Output enable low to output valid	t <sub>GLQV</sub>	—	2.3	ns	1, 4
Output enable high to output high-Z	t <sub>GHQZ</sub>	—	2.3	ns	1, 3
Sleep mode recovery time	t <sub>ZZR</sub>	20.0	—	ns	5
Sleep mode enable time	t <sub>ZZE</sub>	—	15.0	ns	1, 3, 5

Notes: 1. See figure in "AC Test Conditions".

2. Parameters may be guaranteed by design, i.e., without tester guardband.

3. Transitions are measured ±50 mV of output high impedance from output low impedance.

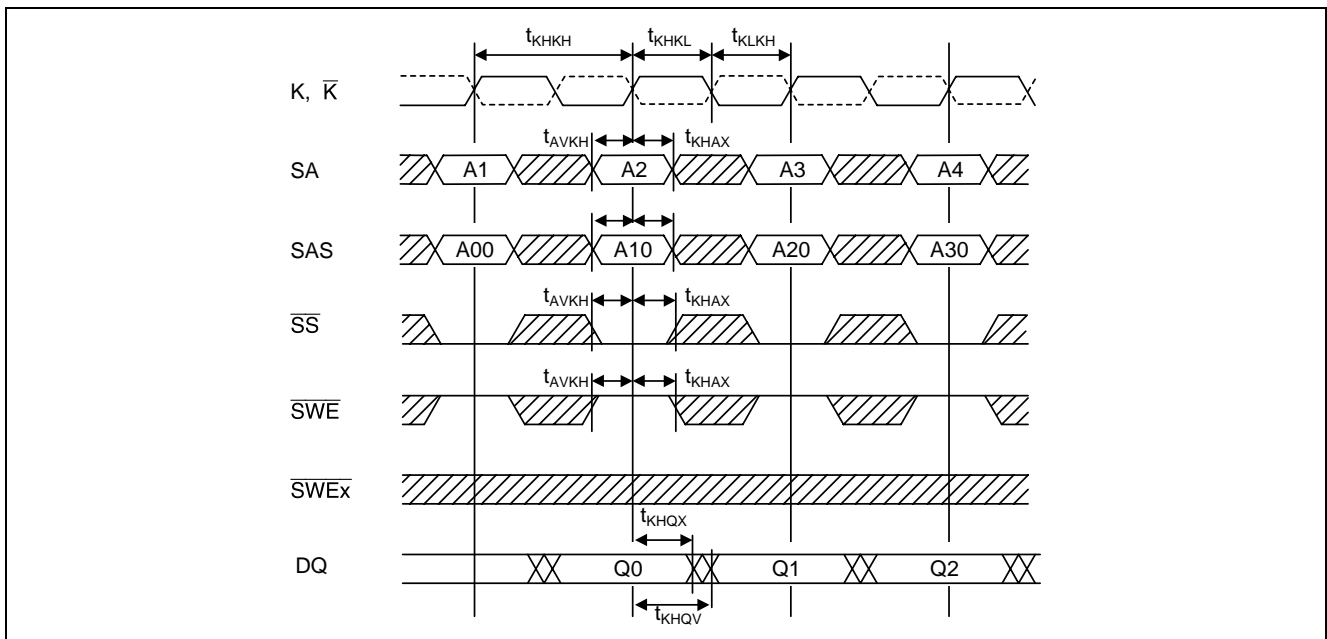
4. Transitions are measured ±50 mV from steady state voltage.

5. When ZZ is switching, clock input K must be at the same logic level for the reliable operation.

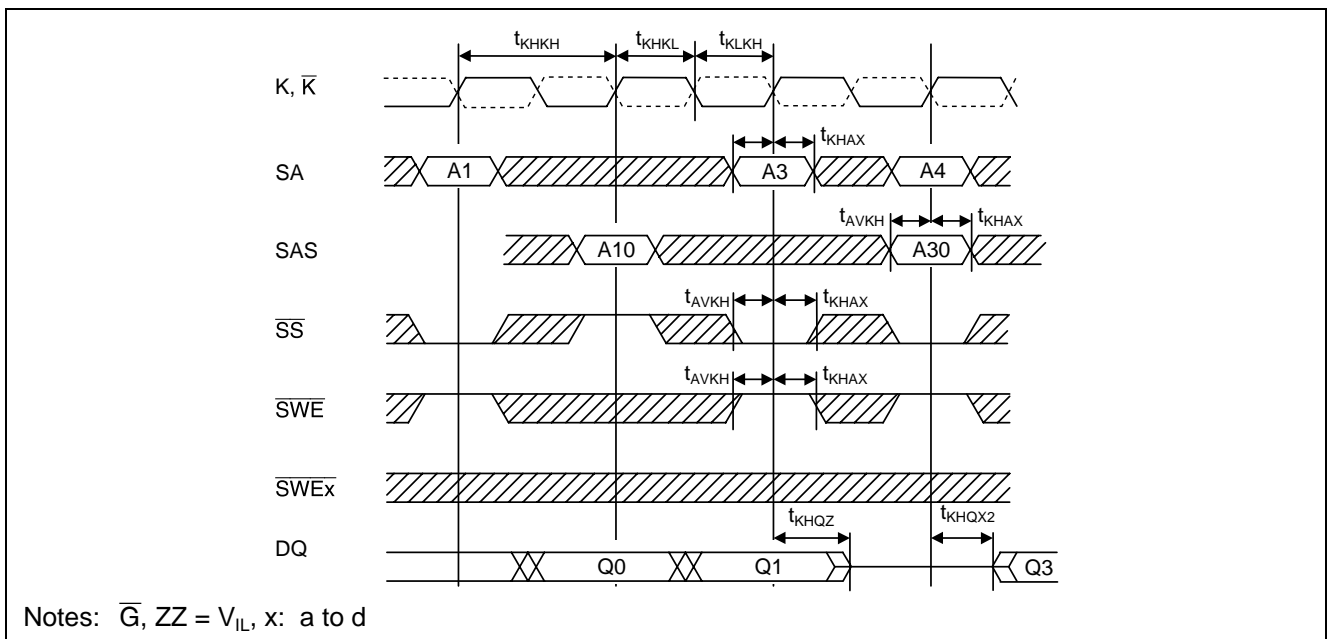
6. Minimum value is verified by design and tested without guardband.

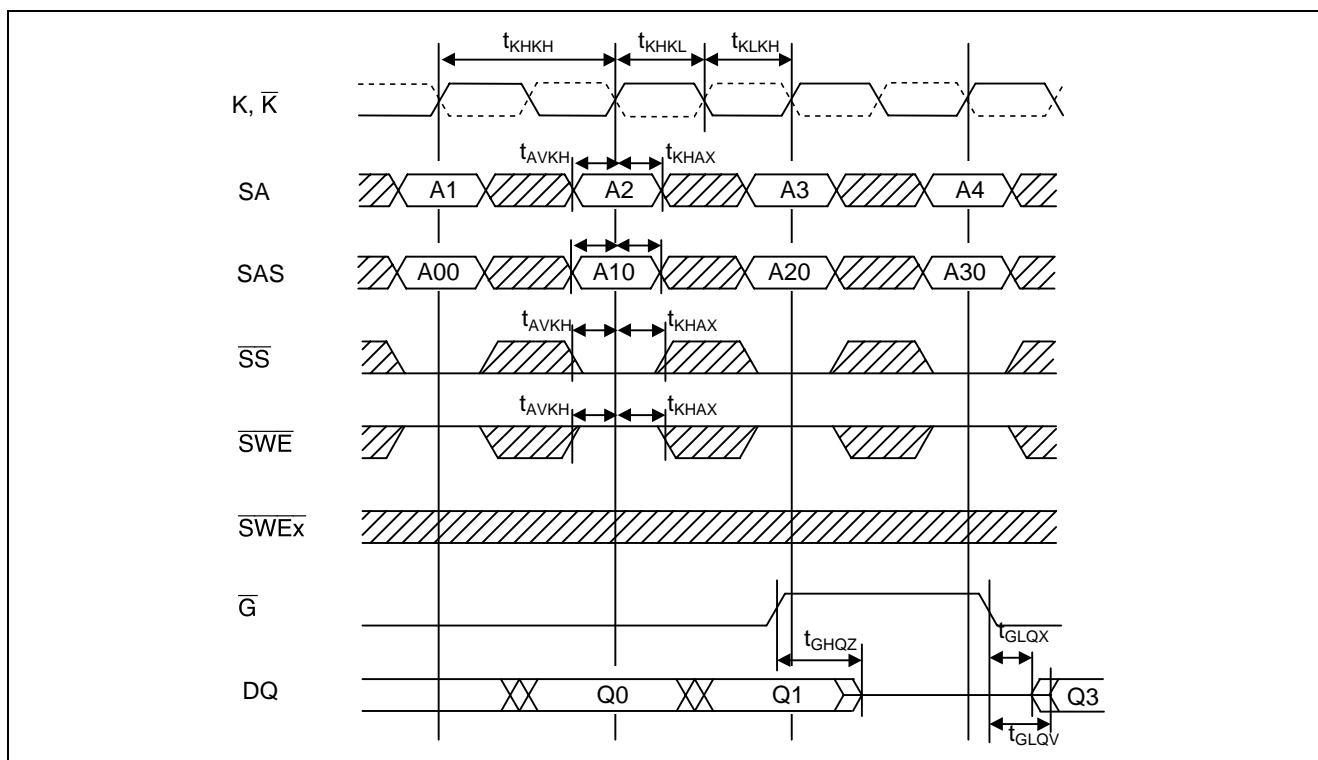
## Timing Waveforms (Late Select Mode)

### Read Cycle-1



### Read Cycle-2 ( $\bar{SS}$ Controlled)



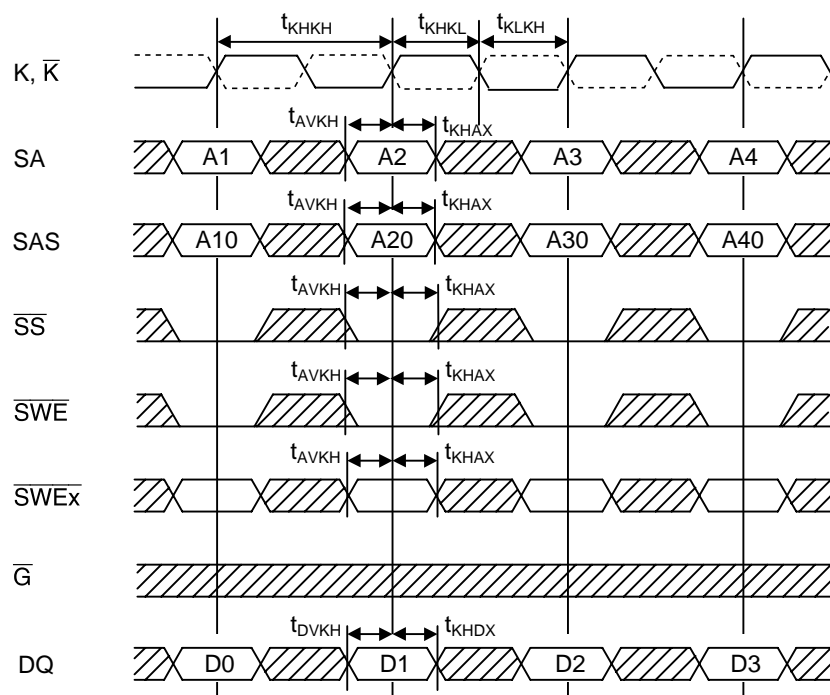
Read Cycle-3 ( $\overline{G}$  Controlled)

## Read operation (late select mode)

During read cycle, N-1 bits of address (SA) are registered during the first rising clock edge. The Nth bit of address (SAS) is registered one clock edge later (the second edge). The setup time requirements for all address bits are the same. SAS is used as the Nth bit of address on both read and write.

The internal array is read between this first edge and second edge, and data is captured in the output register at the second clock edge. This requires the Nth address bit (SAS) to be used as the MUX select before the output register. Alternatively, the Nth address bit can be registered, and used as the MUX select during the data drive cycle. In that case, the output drive should still have a monotonic edge transition (no glitches due to logic switch).

## Write Cycle

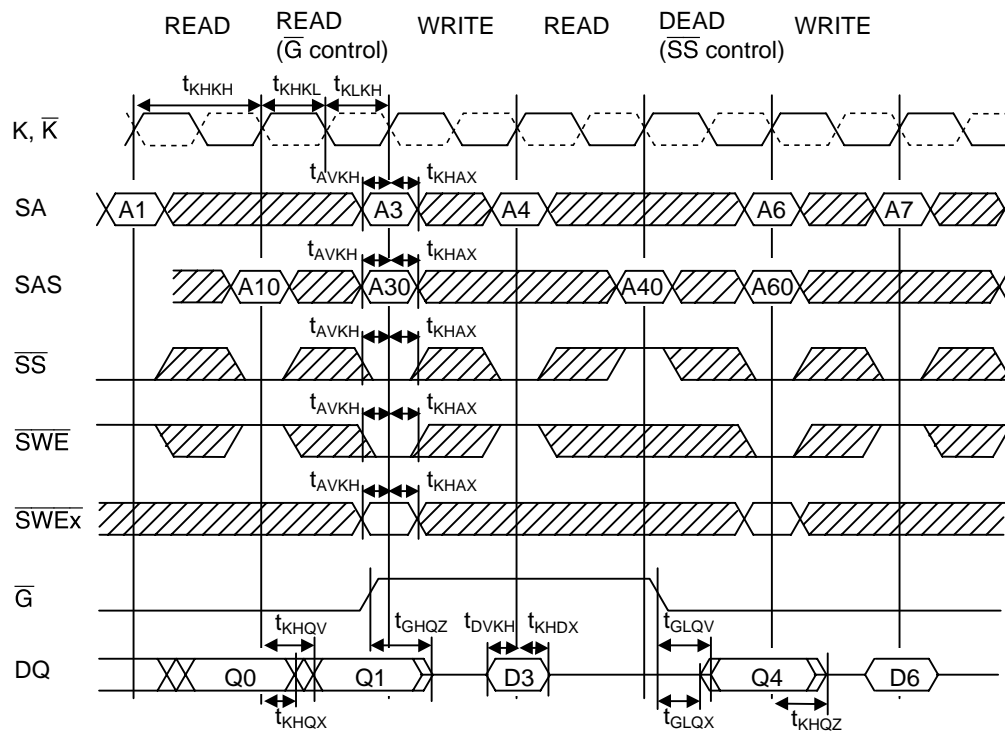


Notes: ZZ =  $V_{IL}$ , x: a to d

## Write operation (late write and late select mode)

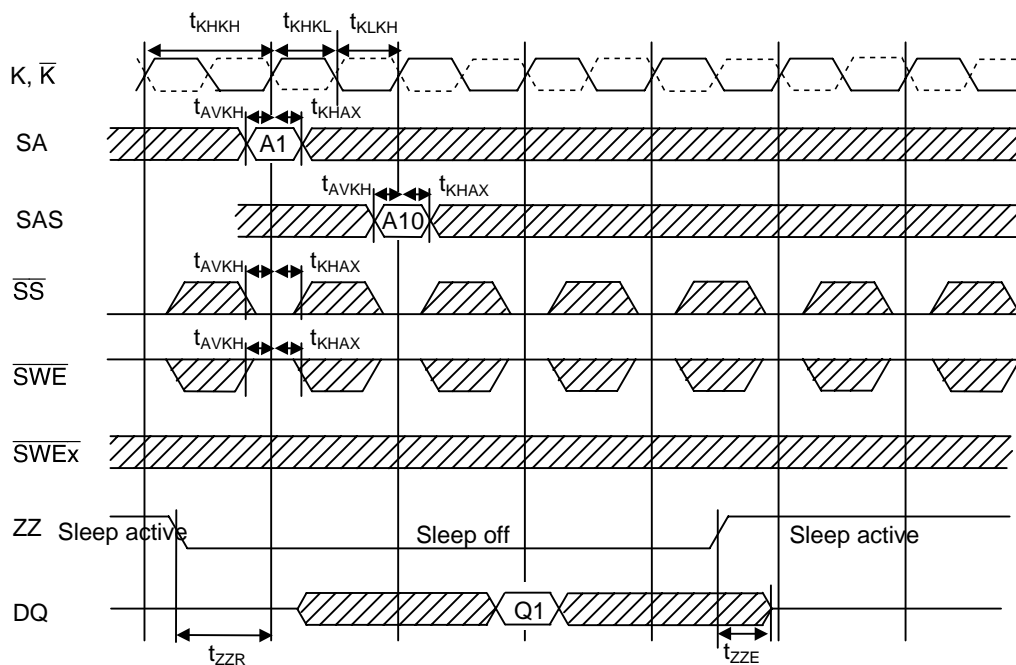
During writes, the write data follows the write address by one cycle. All N bits of address are presented during the same cycle. Any subsequent read to this address should get the latest data. Because in the actual implementation the data will be written into the SRAM array only after the next write address is received, a one-entry buffer is needed to hold the write data and to allow bypassing of data from the write buffer to the output if there is a read of the same address.

## Read-Write Cycle



Notes:  $ZZ = V_{IL}$ , x: a to d

## ZZ Control

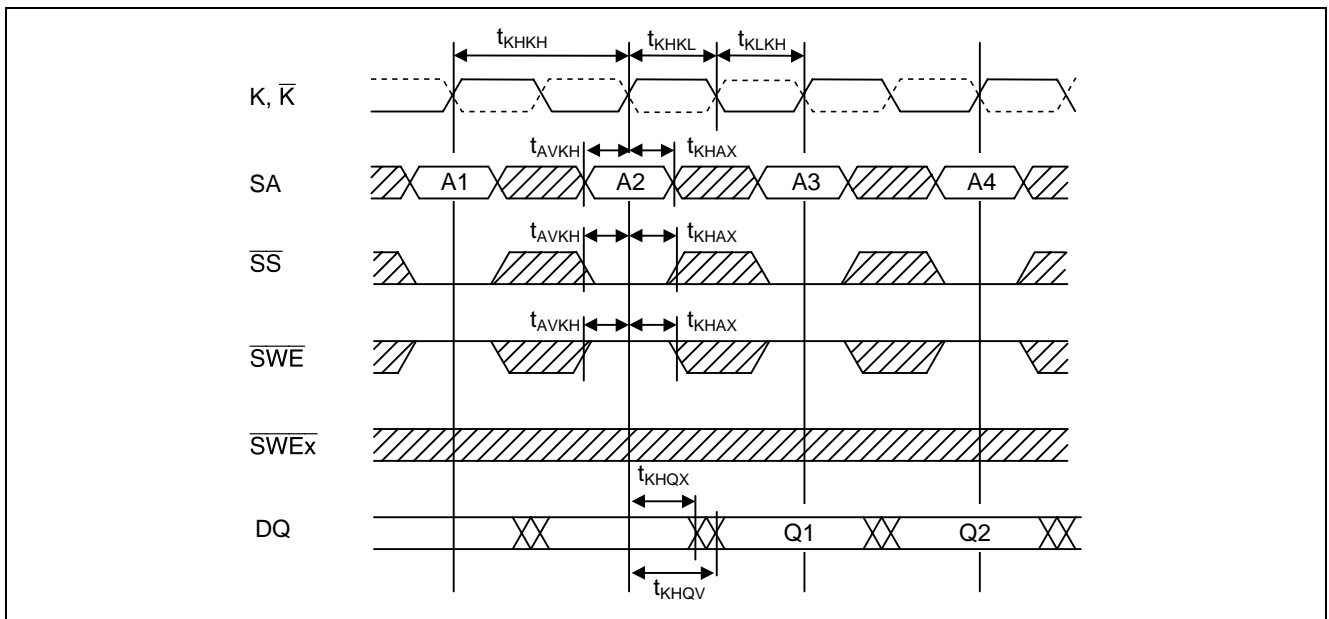


Notes:  $\bar{G} = V_{IL}$ , x: a to d

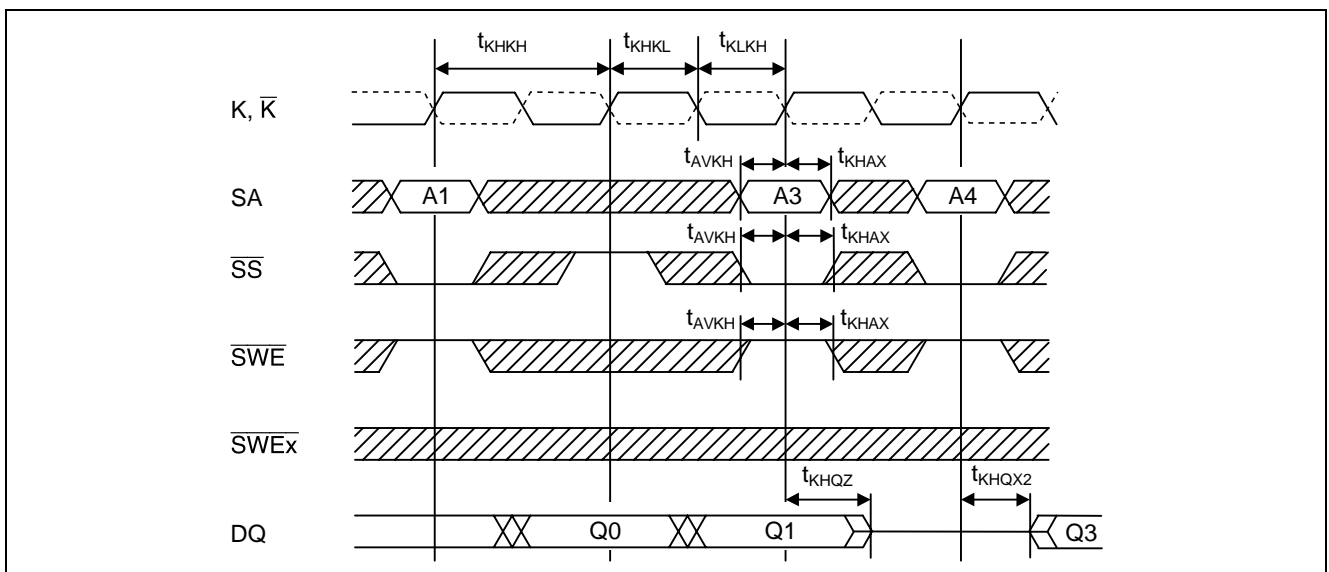
When  $ZZ$  is switching, clock input  $K$  must be at the same logic level for the reliable operation.

## Timing Waveforms (Late Write Mode)

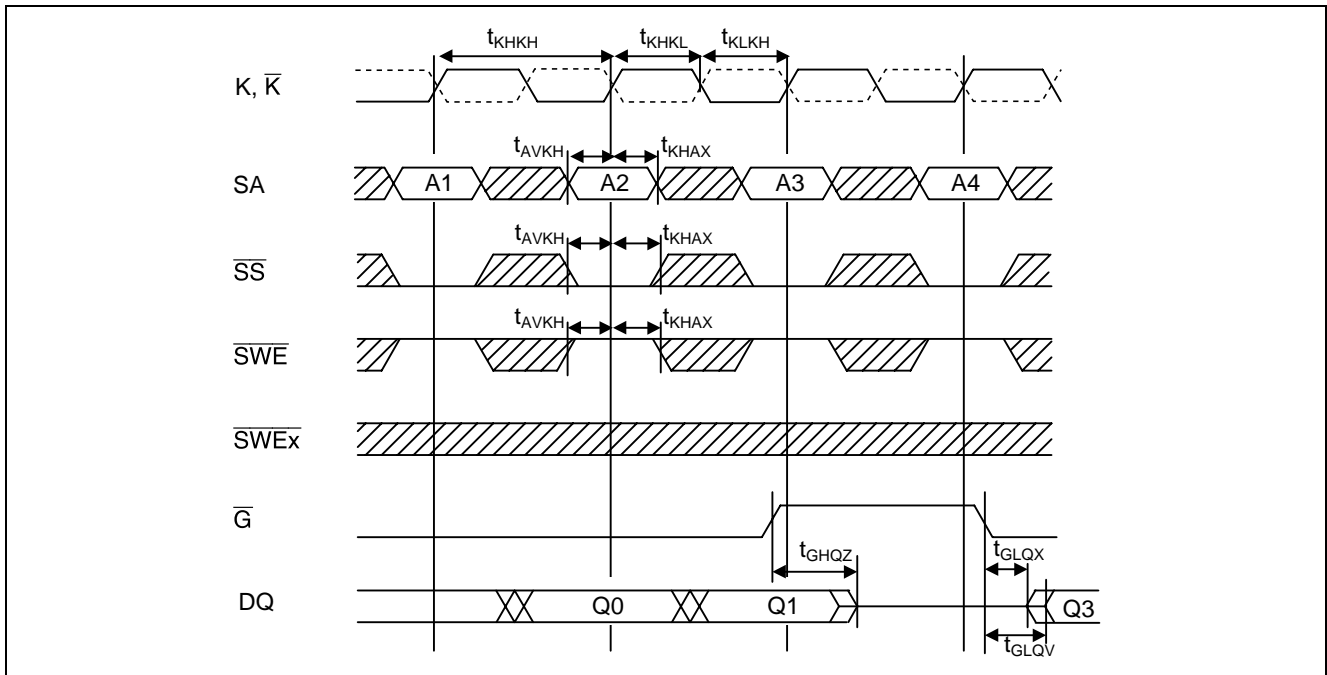
### Read Cycle-1



### Read Cycle-2 ( $\bar{SS}$ Controlled)



Read Cycle-3 ( $\overline{G}$  Controlled)

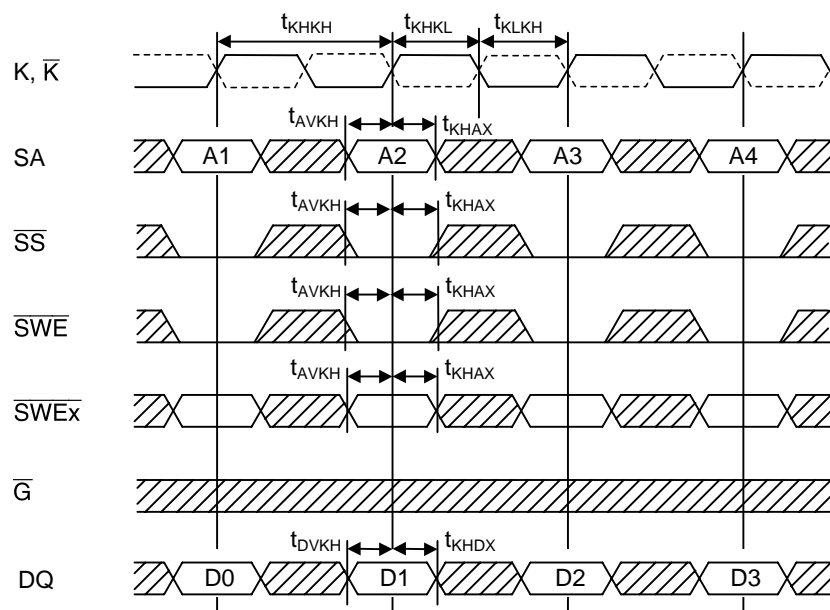


Read operation (late write mode)

During read cycle, the address is registered during the first rising clock edge, the internal array is read between this first edge and second edge, and data is captured in the output register.



## Write Cycle

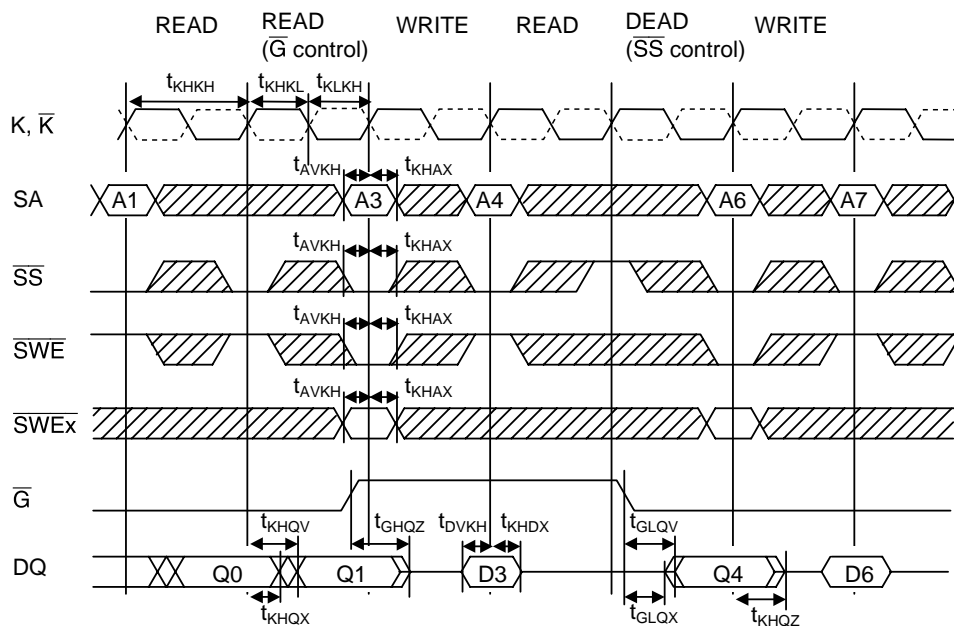


Notes: ZZ =  $V_{IL}$ , x: a to d

## Write operation (late write and late select mode)

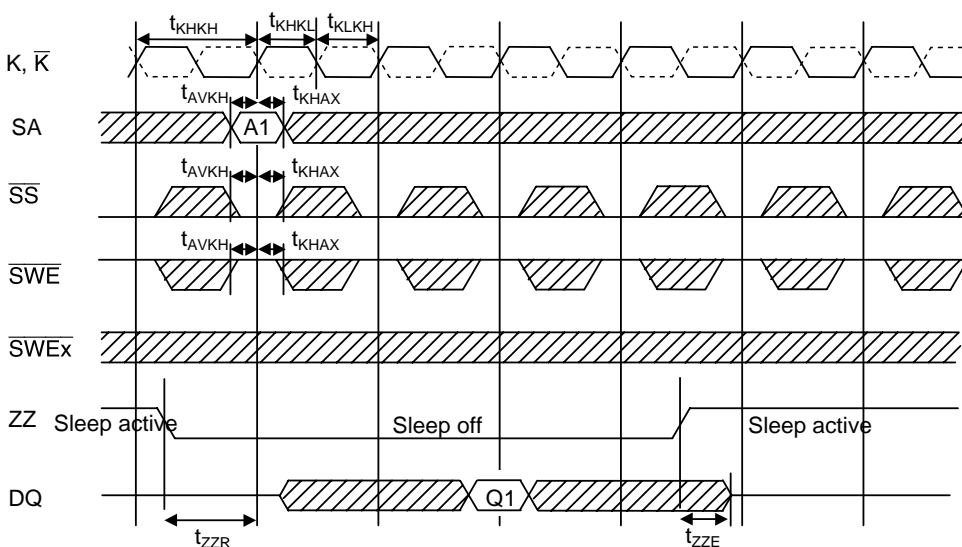
During write cycle, the write data follows the write address by one cycle. All N bits of address are presented during the same cycle. Any subsequent read to this address should get the latest data. Because in the actual implementation the data will be written into the SRAM array only after the next write address is received, a one-entry buffer is needed to hold the write data and to allow bypassing of data from the write buffer to the output if there is a read of the same address.

## Read-Write Cycle



Notes:  $\bar{ZZ} = V_{IL}$ , x: a to d

## ZZ Control

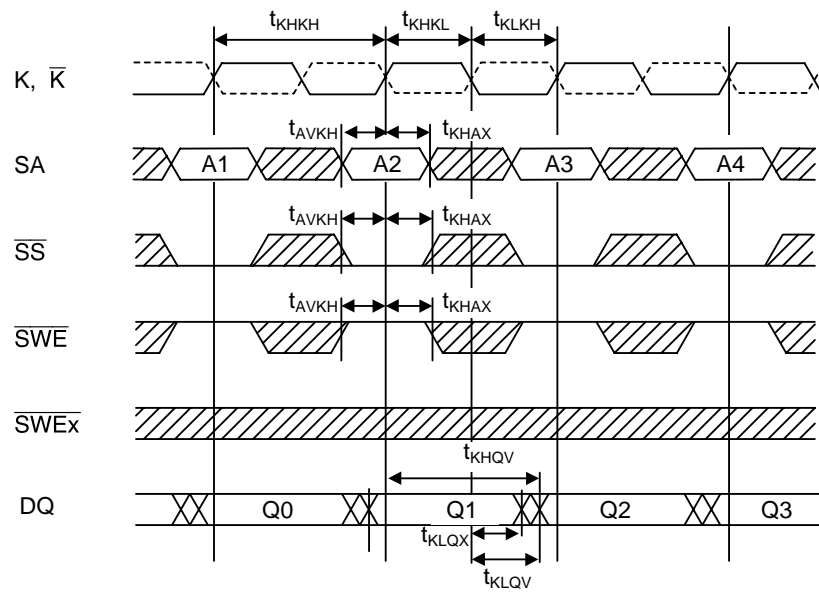


Notes:  $\bar{G} = V_{IL}$ , x: a to d

When  $ZZ$  is switching, clock input  $K$  must be at the same logic level for the reliable operation.

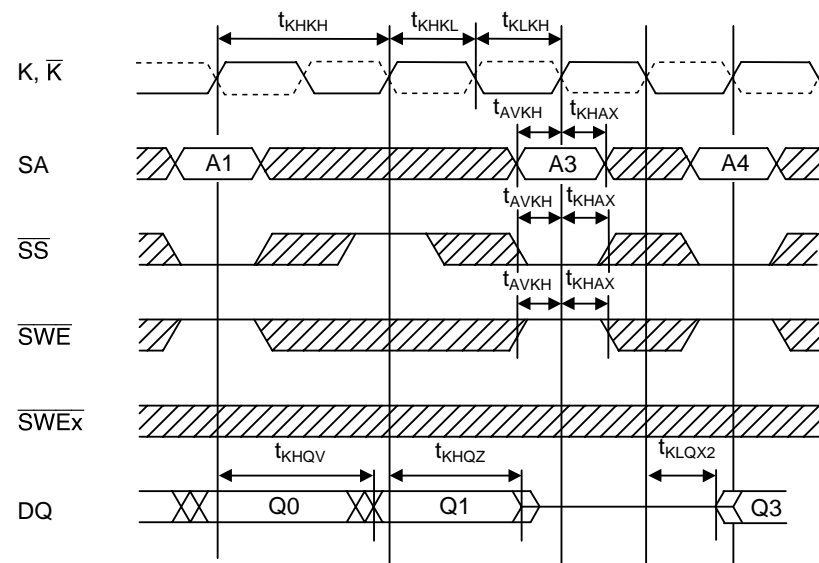
## Timing Waveforms (Register-Latch Mode)

### Read Cycle-1



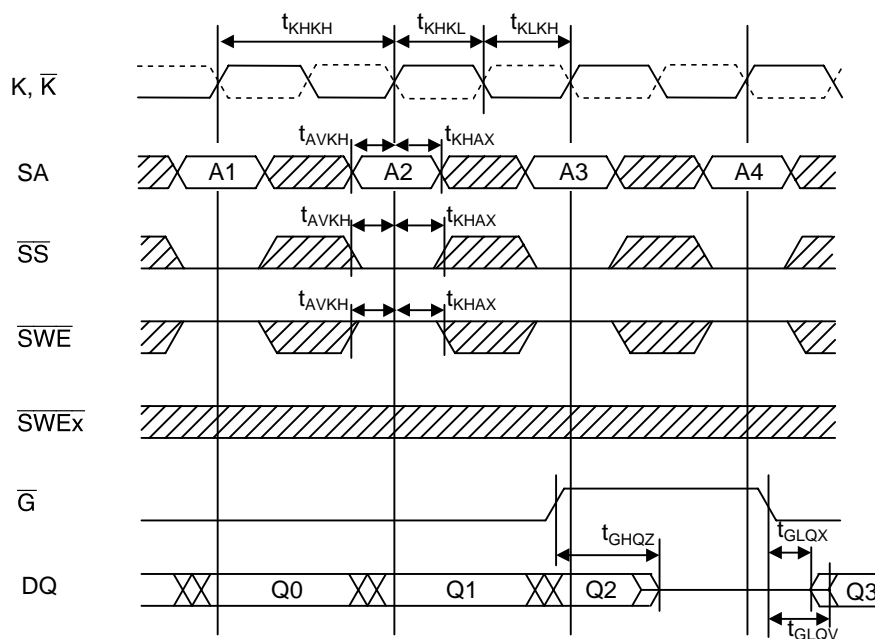
Note:  $ZZ = V_{IL}$

### Read Cycle-2 ( $\bar{SS}$ Controlled)



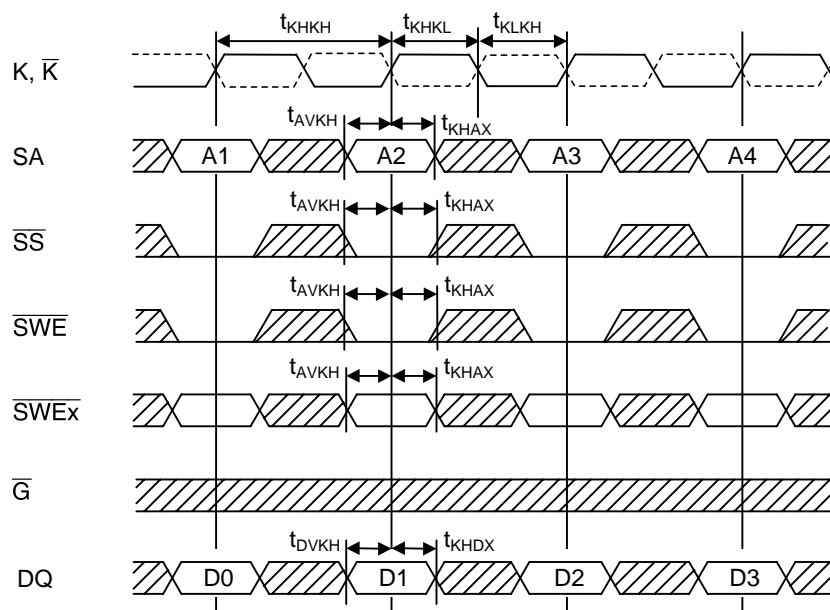
Note:  $ZZ = V_{IL}$

### Read Cycle-3 ( $\overline{G}$ Controlled)



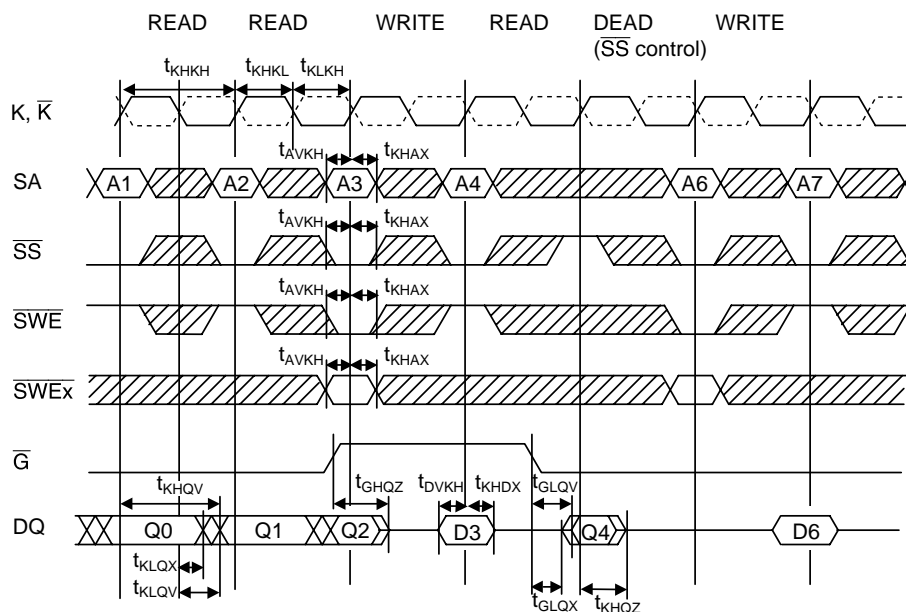
Note: ZZ =  $V_{IL}$

### Write Cycle



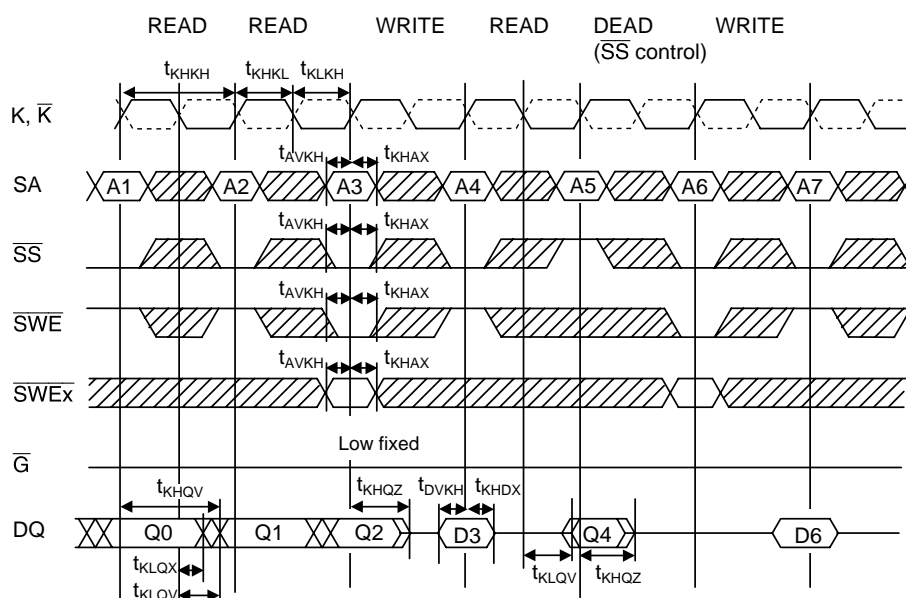
Note: ZZ =  $V_{IL}$

## Read-Write Cycle-1



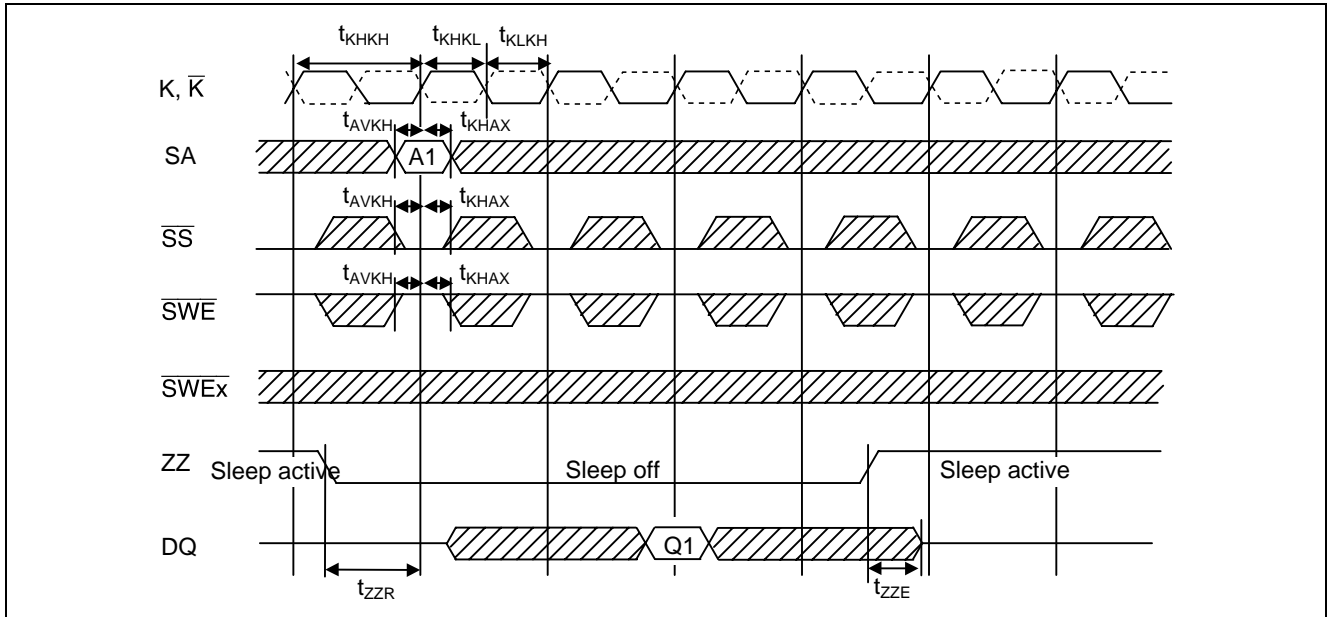
Note:  $ZZ = V_{IL}$

## Read-Write Cycle-2



Note:  $\bar{G}, ZZ = V_{IL}$   
 During this period  $DQ$  pins are in the output state so that the input signal of opposite phase to the outputs must not be applied.

## ZZ Control



## Input Capacitance

( $V_{DD} = 2.5\text{ V}$ ,  $V_{DDQ} = 1.5\text{ V}$ ,  $T_a = +25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

Parameter	Symbol	Min	Max	Unit	Pin name	Notes
Input capacitance	$C_{IN}$	—	4	pF	SAn, SAS, $\overline{SS}$ , $\overline{SWE}$ , $\overline{SWEx}$	1, 3
Clock input capacitance	$C_{CLK}$	—	5	pF	K, $\overline{K}$	1, 2, 3
I/O capacitance	$C_{IO}$	—	5	pF	DQxn	1, 3

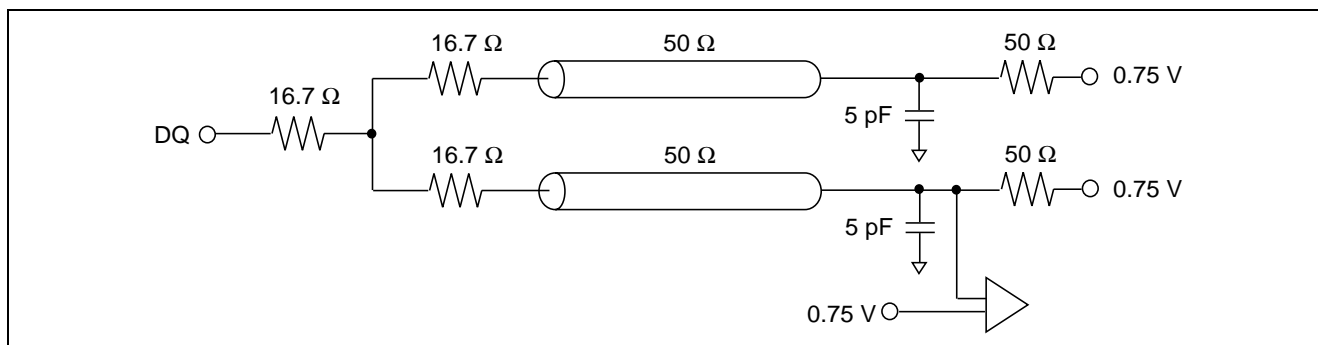
- Notes: 1. This parameter is sampled and not 100% tested.  
 2. Exclude  $\overline{G}$   
 3. Connect pins to GND, except  $V_{DD}$ ,  $V_{DDQ}$ , and the measured pin.

## AC Test Conditions

Parameter	Symbol	Conditions		Unit	Note
		Late select mode Late write mode	Register-latch mode		
Input and output timing reference levels	$V_{REF}$	0.75	0.75	V	
Input signal amplitude	$V_{IL}$ , $V_{IH}$	0.25 to 1.25	0.25 to 1.25	V	
Input rise / fall time	$t_r$ , $t_f$	0.5 (10% to 90%)	0.5 (10% to 90%)	ns	
Clock input timing reference level		Differential cross point	Differential cross point		
$V_{DIF}$ to clock		0.75	0.75	V	
$V_{CM}$ to clock		0.75	1.10	V	
Output loading conditions		See figure below	See figure below		

Note: Parameters are tested with  $R_Q = 250\ \Omega$  and  $V_{DDQ} = 1.5\text{ V}$ .

## Output Loading Conditions



## Boundary Scan Test Access Port Operations

### Overview

In order to perform the interconnect testing of the modules that include this SRAM, the serial boundary scan test access port (TAP) is designed to operate in a manner consistent with IEEE Standard 1149.1 - 1990. But does not implement all of the functions required for 1149.1 compliance. The HM64YLB series contains a TAP controller. Instruction register, boundary scans register, bypass register and ID register.

### Test Access Port Pins

Symbol I/O	Name
TCK	Test clock
TMS	Test mode select
TDI	Test data in
TDO	Test data out

Note: This device does not have a TRST (TAP reset) pin. TRST is optional in IEEE 1149.1.  
 To disable the TAP, TCK must be connected to  $V_{SS}$ . TDO should be left unconnected.  
 To test boundary scan, the ZZ pin needs to be kept below  $V_{REF} - 0.4$  V.

### TAP DC Operating Characteristics

( $T_a = 0$  to  $+85^{\circ}\text{C}$ )

Parameter	Symbol	Min	Max	Notes
Boundary scan input high voltage	$V_{IH}$	1.4 V	3.6 V	
Boundary scan input low voltage	$V_{IL}$	-0.3 V	0.8 V	
Boundary scan input leakage current	$I_{LI}$	-10 $\mu\text{A}$	+10 $\mu\text{A}$	1
Boundary scan output low voltage	$V_{OL}$	—	0.2 V	2
Boundary scan output high voltage	$V_{OH}$	2.1 V	—	3
Boundary scan output leakage current	$I_{LO}$	-5 $\mu\text{A}$	+5 $\mu\text{A}$	4

Notes: 1.  $0 \leq V_{IN} \leq 3.6$  V for all logic input pins  
 2.  $I_{OL} = 2$  mA at  $V_{DD} = 2.5$  V.  
 3.  $I_{OH} = -2$  mA at  $V_{DD} = 2.5$  V.  
 4.  $0 \leq V_{OUT} \leq V_{DD}$ , TDO in high-Z



## TAP AC Operating Characteristics

(Ta = 0 to +85°C)

Parameter	Symbol	Min	Max	Unit	Note
Test clock cycle time	t <sub>THTH</sub>	67	—	ns	
Test clock high pulse width	t <sub>HTL</sub>	30	—	ns	
Test clock low pulse width	t <sub>TLTH</sub>	30	—	ns	
Test mode select setup	t <sub>MVTH</sub>	10	—	ns	
Test mode select hold	t <sub>HMX</sub>	10	—	ns	
Capture setup	t <sub>CS</sub>	10	—	ns	1
Capture hold	t <sub>CH</sub>	10	—	ns	1
TDI valid to TCK high	t <sub>DVTH</sub>	10	—	ns	
TCK high to TDI don't care	t <sub>THDX</sub>	10	—	ns	
TCK low to TDO unknown	t <sub>TLQX</sub>	0	—	ns	
TCK low to TDO valid	t <sub>TLQV</sub>	—	20	ns	

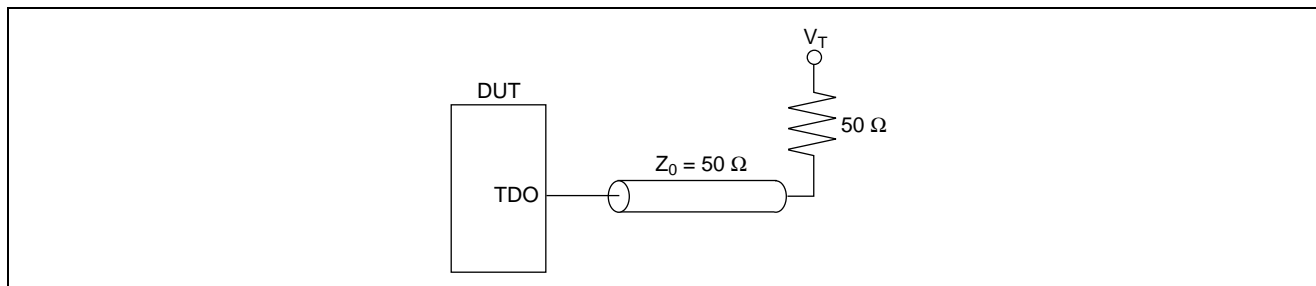
Note: 1. t<sub>CS</sub> + t<sub>CH</sub> defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

## TAP AC Test Conditions

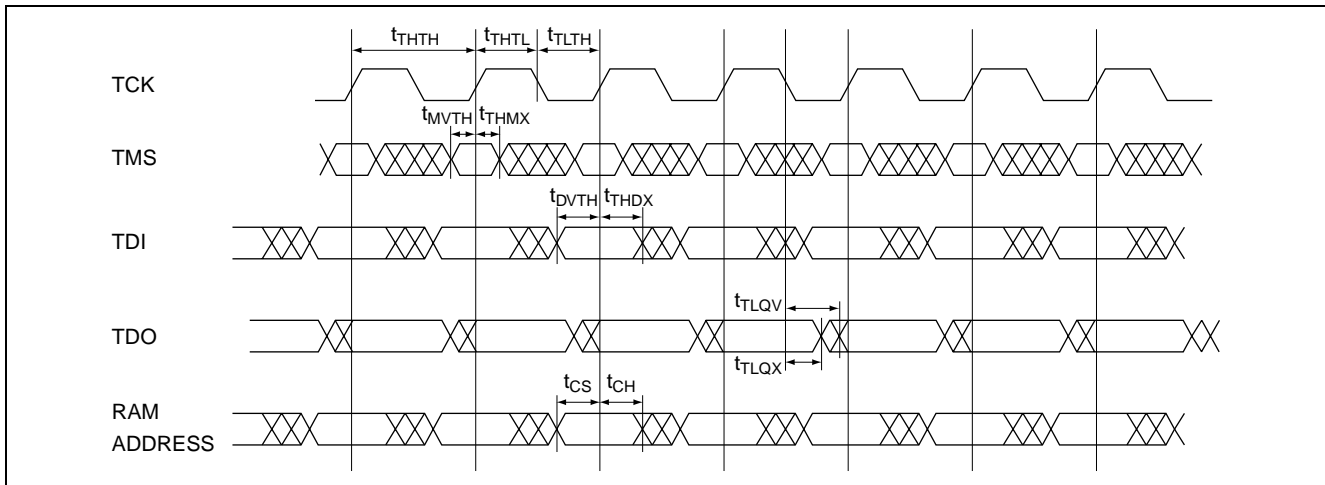
(V<sub>DD</sub> = 2.5 V)

Temperature	0°C ≤ Ta ≤ +85°C
Input timing measurement reference level	1.1 V
Input pulse levels	0 to 2.5 V
Input rise/fall time	1.5 ns typical (10% to 90%)
Output timing measurement reference level	1.25 V
Test load termination supply voltage (V <sub>T</sub> )	1.25 V
Output load	See figure below

## Boundary Scan AC Test Load



## TAP Controller Timing Diagram



## Test Access Port Registers

Register name	Length	Symbol	Note
Instruction register	3 bits	IR [2:0]	
Bypass register	1 bit	BP	
ID register	32 bits	ID [31:0]	
Boundary scan register	70 bits	BS [70:1]	

## TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Operation
0	0	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	Tristate all data drivers and capture the pad value
0	1	1	BYPASS	
1	0	0	SAMPLE	
1	0	1	BYPASS	
1	1	0	PRIVATE	Do not use. They are reserved for vendor use only
1	1	1	BYPASS	

Note: This device does not perform EXTEST, INTEST or the preload portion of the PRELOAD command in IEEE 1149.1.

## Boundary Scan Order (HM64YLB36512)

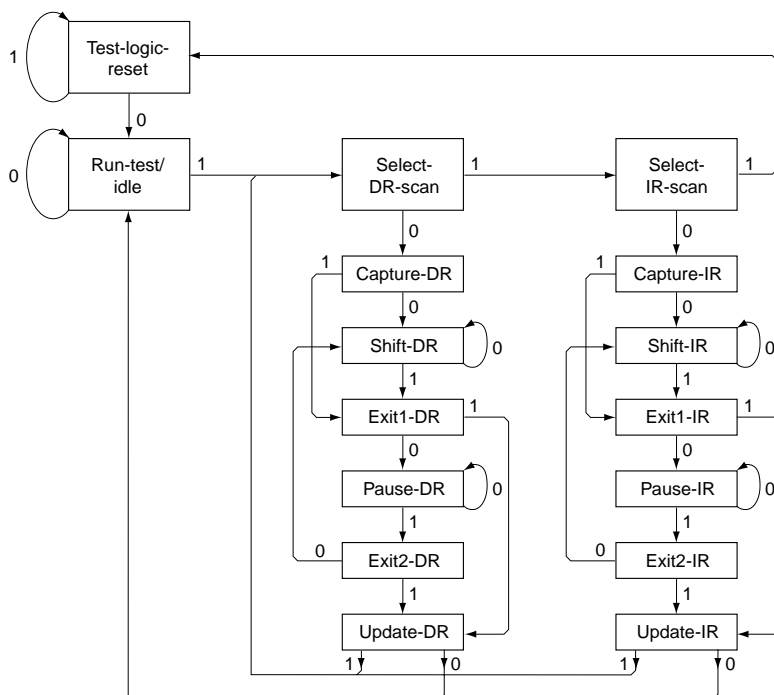
Bit #	Bump ID	Signal name	Bit #	Bump ID	Signal name
1	5R	M2	36	3B	SA12
2	4P	SAS/SA0	37	2B	SA15
3	4T	SA3	38	3A	SA13
4	6R	SA1	39	3C	SA11
5	5T	SA2	40	2C	SA16
6	7T	ZZ	41	2A	SA14
7	6P	DQa8	42	2D	DQc8
8	7P	DQa7	43	1D	DQc7
9	6N	DQa6	44	2E	DQc6
10	7N	DQa5	45	1E	DQc5
11	6M	DQa4	46	2F	DQc4
12	6L	DQa2	47	2G	DQc2
13	7L	DQa3	48	1G	DQc3
14	6K	DQa0	49	2H	DQc0
15	7K	DQa1	50	1H	DQc1
16	5L	$\overline{\text{SWEa}}$	51	3G	$\overline{\text{SWEc}}$
17	4L	$\overline{\text{K}}$	52	4D	ZQ
18	4K	K	53	4E	SS
19	4F	$\overline{\text{G}}$	54	4G	NC
20	5G	$\overline{\text{SWEb}}$	55	4H	NC
21	7H	DQb1	56	4M	$\overline{\text{SWE}}$
22	6H	DQb0	57	3L	$\overline{\text{SWEd}}$
23	7G	DQb3	58	1K	DQd1
24	6G	DQb2	59	2K	DQd0
25	6F	DQb4	60	1L	DQd3
26	7E	DQb5	61	2L	DQd2
27	6E	DQb6	62	2M	DQd4
28	7D	DQb7	63	1N	DQd5
29	6D	DQb8	64	2N	DQd6
30	6A	SA7	65	1P	DQd7
31	6C	SA8	66	2P	DQd8
32	5C	SA4	67	3T	SA18
33	5A	SA6	68	2R	SA10
34	6B	SA9	69	4N	SA17
35	5B	SA5	70	3R	M1

- Notes:
1. Bit#1 is the first scan bit to exit the chip.
  2. Bit#2 is SAS in both the late select mode and the late write mode, or is SA0 in the register-latch mode.
  3. The NC pads listed in this table are indeed no connects, but are represented in the boundary scan register by a "Place Holder". Place holder registers are internally connected to  $V_{SS}$ .
  4. In boundary scan mode, differential input K and  $\overline{\text{K}}$  are referenced to each other and must be at the opposite logic levels for the reliable operation.
  5. ZZ must remain  $V_{IL}$  during boundary scan.
  6. In boundary scan mode, ZQ must be driven to  $V_{DDQ}$  or  $V_{SS}$  supply rail to ensure consistent results.
  7. M1 and M2 must be driven to  $V_{DD}$ ,  $V_{DDQ}$  or  $V_{SS}$  supply rail to ensure consistent results.

## ID Register

Part	Revision number (31:28)	Device density and configuration (27:18)	Vendor definition (17:12)	Vendor JEDEC code (11:1)	Start bit (0)
HM64YLB36512	0000	0011100100	xxxxxx	00000000111	1

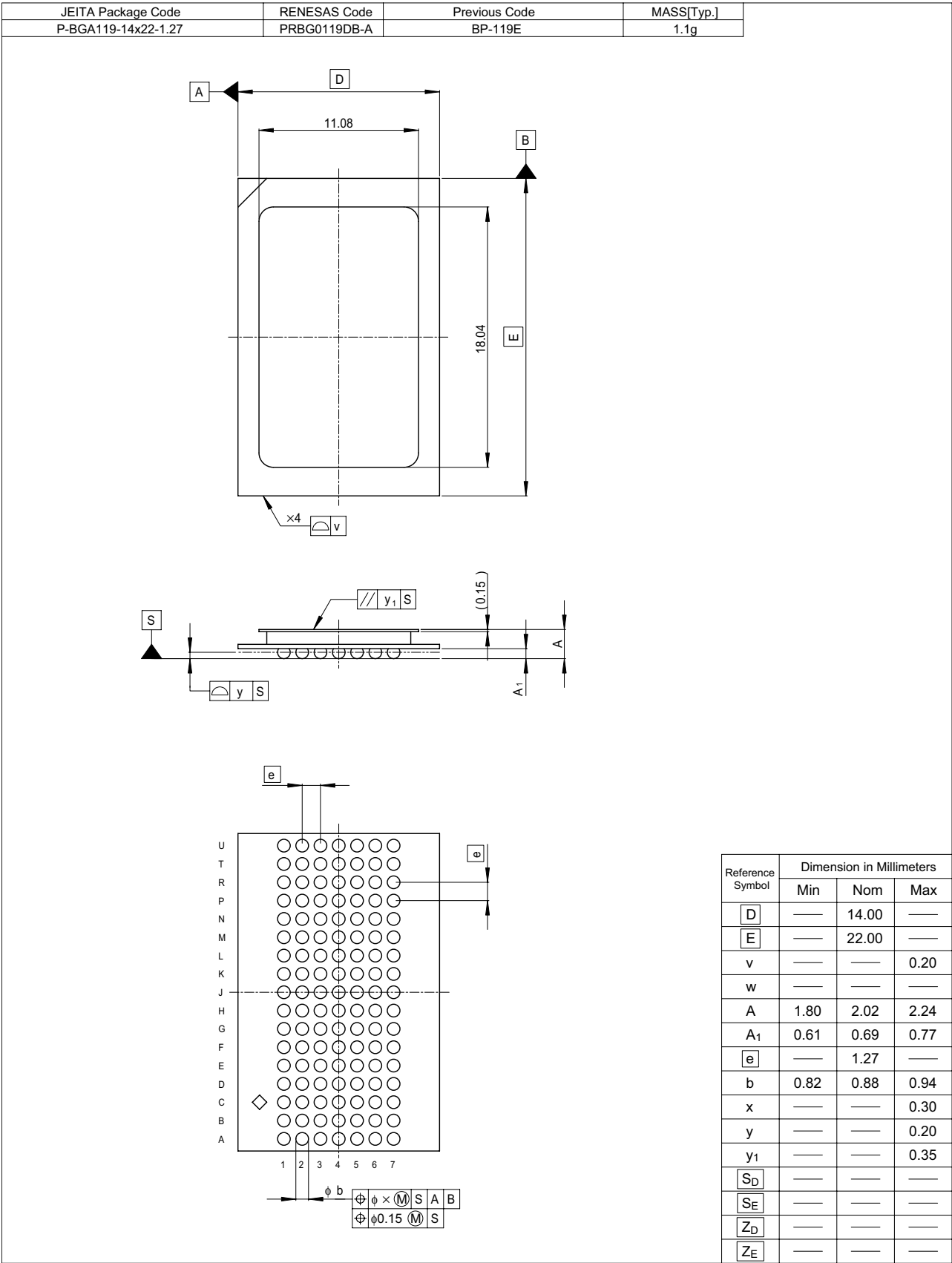
## TAP Controller State Diagram



Note: The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK.  
No matter what the original state of the controller, it will enter Test-logic-reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions

HM64YLB36512BP Series (PRBG0119DB-A / Previous Code: BP-119E)



## Revision History

## HM64YLB36512 Series Data Sheet

Rev.	Date	Description	
		Page	Summary
0.0	May. 6, 2002	—	Initial issue
0.1	Aug. 30, 2002	5	Truth Table
		18	Deletion of Notes3 Input Capacitance Addition of Notes3
1.0	Feb. 7, 2003	6	Change of Programmable Impedance Output Drivers
2.00	Jul. 19, 2005	—	Change format issued by Renesas Technology Corp.
		—	The Former HM64YLB36512BP-33 and the former HM64YLB36514BP-6H are integrated into the new HM64YLB36512BP-33
		1	Change of Features, adding register-latch mode
		2	Ordering Information
			Addition of Modes
			Addition of Renesas package codes
		2	Pin Arrangement
			4P: SAS to SAS/SA0
			Addition of Note
		4	Addition of Block Diagram in register-latch mode
		5	Pin Descriptions
			Change of SAn, SAS Notes, adding register-latch mode
			Addition of M1, M2 Protocol in register-latch mode
			Change of Notes2, adding register-latch mode
		6	Truth Table: Addition of DQ (n), DQ (n+1) in register-latch mode
		7	Change of
			Programmable Impedance
			Output Drivers
		8	Recommended DC Operating Conditions
			Addition of the values in register-latch mode
		9	DC Characteristics: Addition of the values in register-latch mode
		10	AC Characteristics: Addition of the table in register-latch mode
		19-22	Addition of Timing Waveforms in register-latch mode
		23	AC Test Conditions: Addition of the values in register-latch mode
		27	Boundary Scan Order
			Bit#2: SAS to SAS/SA0
			Notes2-6 to Notes3-7
			Addition of Notes2
		29	Package Dimensions
			Addition of Renesas package codes
			Changed to Renesas formats
3.00	Jan. 13, 2006	9	DC Characteristics: $V_{OH}$ to $V_{OH1}$ , addition of $V_{OH2}$

## Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



### RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

#### **Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

#### **Renesas Technology Europe Limited**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

#### **Renesas Technology (Shanghai) Co., Ltd.**

Unit 205, AZIA Center, No.133 Yincheng Rd (n), Pudong District, Shanghai 200120, China  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

#### **Renesas Technology Hong Kong Ltd.**

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

#### **Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

#### **Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

#### **Renesas Technology Korea Co., Ltd.**

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

#### **Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510