National Semiconductor

June 30, 2008

LM111QML
Voltage Comparator

General Description

The LM111 is a voltage comparator that has input currents nearly a thousand times lower than devices such as the LM106 or LM710. It is also designed to operate over a wider range of supply voltages: from standard ±15V op amp supplies down to the single 5V supply used for IC logic. The output is compatible with RTL, DTL and TTL as well as MOS circuits. Further, it can drive lamps or relays, switching voltages up to 50V at currents as high as 50 mA.

Both the inputs and the output of the LM111 can be isolated from system ground, and the output can drive loads referred to ground, the positive supply or the negative supply. Offset balancing and strobe capability are provided and outputs can be wire OR'ed. Although slower than the LM106 and LM710 (200 ns response time vs 40 ns) the device is also much less prone to spurious oscillations. The LM111 has the same pin configuration as the LM106 and LM710.

Features

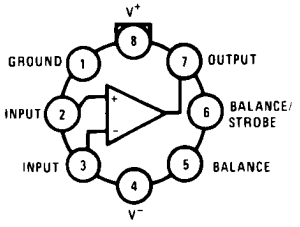
- Available with radiation guaranteed
  - — High Dose Rate 50 krad(Si)
  - — Low Dose and ELDRS Free 100 krad(Si)
- Operates from single 5V supply
- Input current: 200 nA max. over temperature
- Offset current: 20 nA max. over temperature
- Differential input voltage range: ±30V
- Power consumption: 135 mW at ±15V
- Power supply voltage, single 5V to ±15V
- Offset voltage null capability
- Strobe capability

Ordering Information

NS PART NUMBER	SMD PART NUMBER	NS PACKAGE NUMBER	PACKAGE DESCRIPTION
LM111E-SMD	5962-8687701Q2A	E20A	20LD Leadless Chip Carrier
LM111H-SMD	5962-8687701QGA	H08C	8LD TO-99 Metal Can
LM111J-8-SMD	5962-8687701QPA	J08A	8LD CERDIP
LM111WG-SMD	5962-8687701QZA	WG10A	10LD Ceramic SOIC
LM111E/883		E20A	20LD Leadless Chip Carrier
LM111H/883		H08C	8LD TO-99 Metal Can
LM111J-8/883		J08A	8LD CERDIP
LM111J/883		J14A	14LD CERDIP
LM111W/883		W10A	10LD CERPACK
LM111WG/883		WG10A	10LD Ceramic SOIC
LM111HLQMLV (Note 12) **High Dose Rate ONLY**	5962L0052401VGA 50k rd(Si)	H08C	8LD TO-99 Metal Can
LM111J-8LQMLV (Note 12) **High Dose Rate ONLY**	5962L0052401VPA 50k rd(Si)	J08A	8LD CERDIP
LM111WGLQMLV (Note 12) **High Dose Rate ONLY**	5962L0052401VZA 50k rd(Si)	WG10A	10LD Ceramic SOIC
LM111WLQMLV (Note 12) **High Dose Rate ONLY**	5962L0052401VHA 50k rd(Si)	W10A	10LD CERPACK
LM111HRLQMLV (Note 14) **ELDRS Free ONLY**	5962R0052402VGA 100k rd(Si)	H08C	8LD TO-99 Metal Can
LM111J-8RLQMLV (Note 14) **ELDRS Free ONLY**	5962R0052402VPA 100k rd(Si)	J08A	8LD CERDIP
LM111WGRLQMLV (Note 14) **ELDRS Free ONLY**	5962R0052402VZA 100k rd(Si)	WG10A	10LD Ceramic SOIC
LM111WRLQMLV (Note 14) **ELDRS Free ONLY**	5962R0052402VHA 100k rd(Si)	W10A	10LD CERPACK

Connection Diagrams

Metal Can Package



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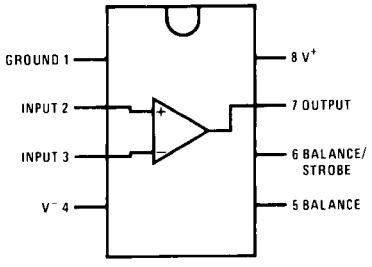
Note: Pin 4 connected to case

Top View
See NS Package Number H08C

Dual-In-Line Package



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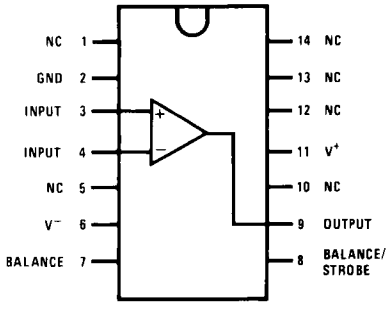
Top View
See NS Package Number J08A

Dual-In-Line Package



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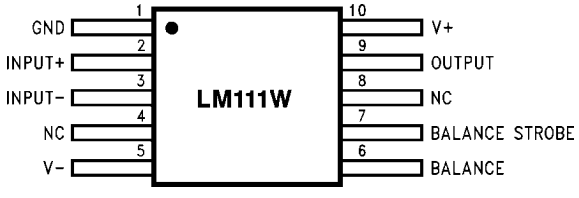
Top View
See NS Package Number J14A



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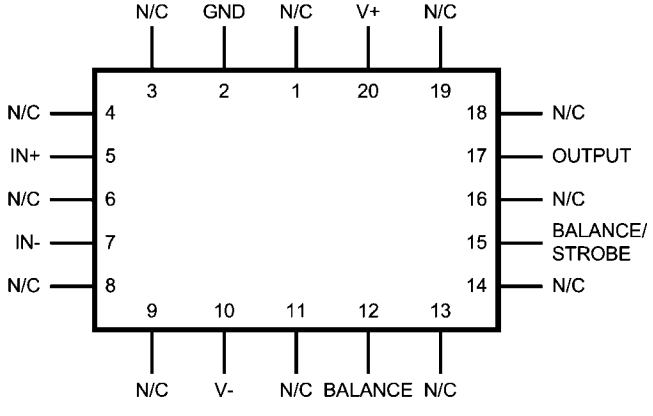
See NS Package Number W10A, WG10A



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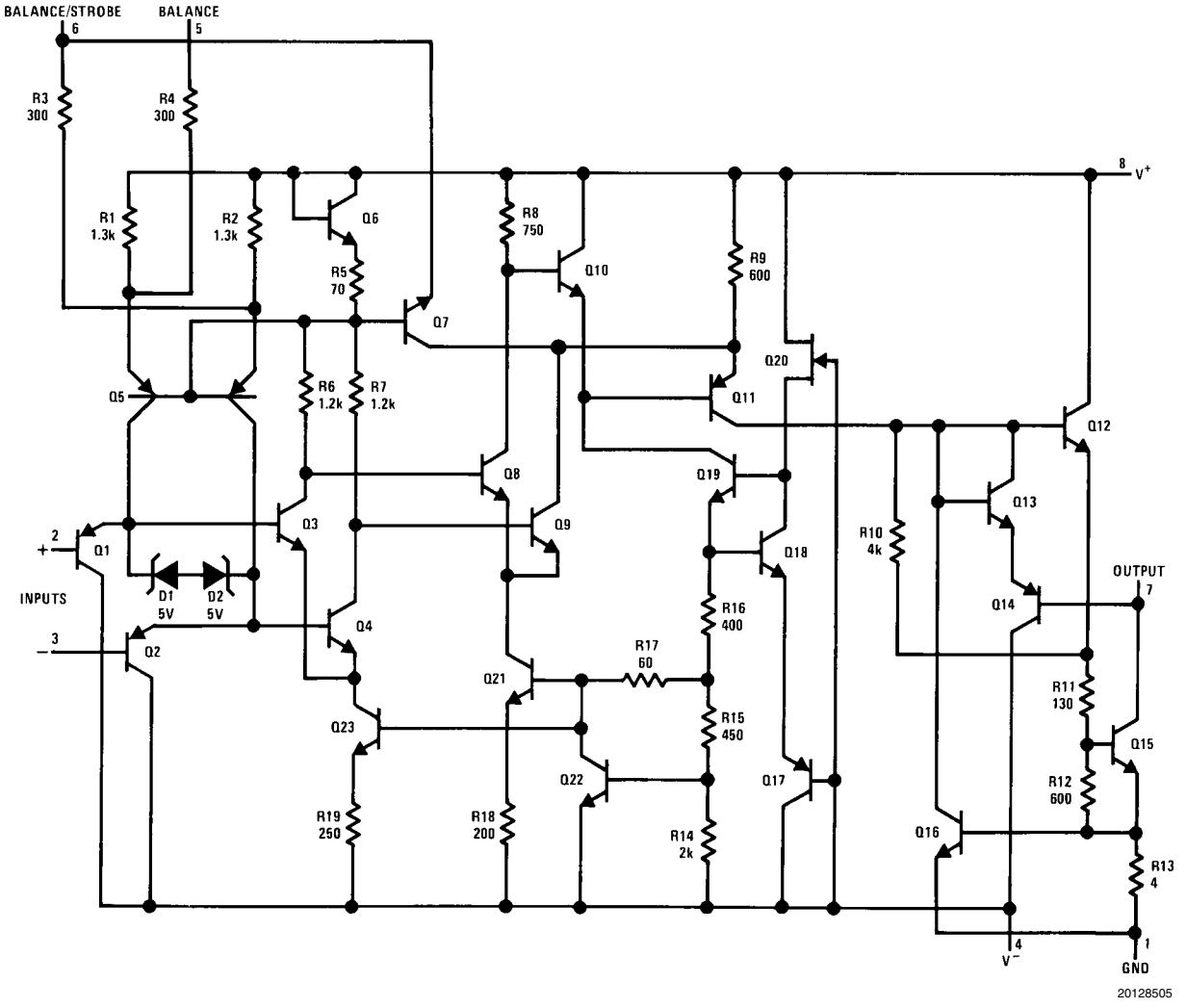
See NS Package NumberE20A

Schematic Diagram

(Note Pin connections shown on schematic diagram are for H08 package.)



Note 1: Pin connections shown on schematic diagram are for H08 package.

Absolute Maximum Ratings (Note 2)

Positive Supply Voltage	+30.0V
Negative Supply Voltage	-30.0V
Total Supply Voltage	36V
Output to Negative Supply Voltage	50V
GND to Negative Supply Voltage	30V
Differential Input Voltage	±30V
Sink Current	50mA
Input Voltage (Note 3)	±15V
Power Dissipation (Note 4)	
8 LD CERDIP	400mW @ 25°C
8 LD Metal Can	330mW @ 25°C
10 LD CERPACK	330mW @ 25°C
10 LD Ceramic SOIC	330mW @ 25°C
20 LD LCC	500mW @ 25°C
Output Short Circuit Duration	10 seconds
Maximum Strobe Current	10mA
Operating Temperature Range	$-55°C \leq T_A \leq 125°C$
Thermal Resistance	
θ_{JA}	
8 LD CERDIP (Still Air @ 0.5W)	134°C/W
8 LD CERDIP (500LF/Min Air flow @ 0.5W)	76°C/W
8 LD Metal Can (Still Air @ 0.5W)	162°C/W
8 LD Metal Can (500LF/Min Air flow @ 0.5W)	92°C/W
10 Ceramic SOIC (Still Air @ 0.5W)	231°C/W
10 Ceramic SOIC (500LF/Min Air flow @ 0.5W)	153°C/W
10 CERPACK (Still Air @ 0.5W)	231°C/W
10 CERPACK (500LF/Min Air flow @ 0.5W)	153°C/W
14 LD CERDIP (Still Air @ 0.5W)	97°C/W
14 LD CERDIP (500LF/Min Air flow @ 0.5W)	65°C/W
20 LD LCC (Still Air @ 0.5W)	90°C/W
20 LD LCC (500LF/Min Air flow @ 0.5W)	65°C/W
θ_{JC}	
8 LD CERDIP	21°C/W
8 LD Metal Can Pkg	50°C/W
10 LD Ceramic SOIC	24°C/W
10 LD CERPACK	24°C/W
14 LD CERDIP	20°C/W
20 LD LCC	21°C/W
Storage Temperature Range	$-65°C \leq T_A \leq 150°C$
Maximum Junction Temperature	175°C
Lead Temperature (Soldering, 60 seconds)	300°C
Voltage at Strobe Pin	$V^+ = -5V$
Package Weight (Typical)	
8 LD Metal Can	965mg
8 LD CERDIP	1100mg
10 LD CERPACK	250mg
10 LD Ceramic SOIC	225mg
14 LD CERDIP	TBD
20 LD LCC	TBD
ESD Rating (Note 5)	300V

Recommended Operating Conditions

Supply Voltage	$V_{CC} = \pm 15V_{DC}$
Operating Temperature Range	$-55°C \leq T_A \leq 125°C$

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temperature (°C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

LM111/883 Electrical Characteristics

DC Parameters

The following conditions apply, unless otherwise specified. V_{56} = 0, R_S = 0 Ω, V_{CC} = ±15V, V_{CM} = 0, V_O = 1.4V WRT $-V_{CC}$
The pin assignments are based on the 8 pin package configuration. (Note 7)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current	V_{CM} = 13.5V, R_S = 50KΩ		-10	10	nA	1
				-20	20	nA	2, 3
		V_{CM} = 13.5V, V_{85} = V_{86} = 0V, R_S = 50KΩ	(Note 7)	-30	30	nA	1
		V_{CM} = -14.5V, R_S= 50KΩ		-10	10	nA	1
				-20	20	nA	2, 3
		V_{CM} = -14.5V, V_{85} = V_{86} = 0V, R_S= 50KΩ	(Note 7)	-30	30	nA	1
		R_S = 50KΩ		-10	10	nA	1
				-20	20	nA	2, 3
		V_{85} = V_{86} = 0V, R_S = 50KΩ	(Note 7)	-30	30	nA	1
I_{IB}	Input Bias Current	V_{CM} = 13.5V, R_S = 50KΩ			100	nA	1
					150	nA	2, 3
		V_{CM} = -14.5V, R_S = 50KΩ			100	nA	1
					150	nA	2, 3
		R_S = 50KΩ			100	nA	1
					150	nA	2, 3
I_{OL}	Output Leakage Current	V_{CC} = ± 18V, I_5 + I_6 = 5mA, V_O = 35V WRT $-V_{CC}$	(Note 7)		10	nA	1
			(Note 7)		500	nA	2, 3
I_{GL}	Ground Leakage Current	V_{CC} = ± 18V, I_5 + I_6 = 5mA, V_O = 50V WRT $-V_{CC}$	(Note 7)		25	nA	1
			(Note 7)		500	nA	2
V_{Sat}	Saturation Voltage	V_I = -5mV, I_7 = 50mA	(Note 7)		1.5	V	1, 2, 3
		V_I = -6mV, I_7 = 8mA	(Note 7)		0.4	V	1, 2, 3
$-I_{CC}$	Negative Supply Current				5.0	mA	1, 2
					15	mA	3
$+I_{CC}$	Positive Supply Current				6.0	mA	1, 2
					15	mA	3
I_{L1}	Input Leakage Current	V_{CC} = ± 18V, V_{28} = 1V, V_{38} = 30V, I_5 + I_6 = 5mA V_O = 50V WRT $-V_{CC}$	(Note 7)		10	nA	1
			(Note 7)		30	nA	2
I_{L2}	Input Leakage Current	V_{CC} = ± 18V, V_{38} = 1V, V_{28} = 30V, I_5 + I_6 = 5mA V_O = 50V WRT $-V_{CC}$	(Note 7)		10	nA	1
			(Note 7)		30	nA	2
V_OSt	Collector Output Voltage (Strobe)			14		V	1
		I_{St} = 3mA		14		V	1

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 13.5V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{CM} = 13.5V, V_{85} = V_{86}= 0V	(Note 7)	-3.0	3.0	mV	1
		V_{CM} = -14.5V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{CM} = -14.5V, V_{85} = V_{86} = 0V	(Note 7)	-3.0	3.0	mV	1
				-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_{85} = V_{86} = 0V	(Note 7)	-3.0	3.0	mV	1
		V_O = 0.4V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 3V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		V_O = 4.5V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 3V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
		V_O = 0.4V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 0.5V		-5.0	5.0	mV	1
				-6.0	6.0	mV	2, 3
		V_O = 4.5V, +V_{CC} = 4.5V, -V_{CC} = 0V, V_{CM} = 0.5V		-3.0	3.0	mV	1
				-4.0	4.0	mV	2, 3
A_{VS}	Large Signal Gain	-12V ≤ V_O ≤ 35V, R_L = 1KΩ	(Note 6)	40		V/mV	4
			(Note 6)	30		V/mV	5, 6

AC Parameters

The following conditions apply, unless otherwise specified. V_{56} = 0, R_S = 0 Ω, V_{CC} = ±15V, V_{CM} = 0, V_O = 1.4V WRT –V_{CC}
The pin assignments are based on the 8 pin package configuration. (Note 7)

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR	Response Time				400	nS	7

LM111-SMD Electrical Characteristics SMD 5962-8687701

DC Parameters

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = +2.5V, $-V_{CC}$ = -2.5V, V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
V_{IO} R	Raised Input Offset Voltage	V_I = 0V, R_S = 50Ω	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω	(Note 15)	-3	+3	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	V_I = 0V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
I_{IO}R	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	(Note 15)	-25	+25	nA	1, 2
				-50	+50	nA	3
±I_{IB}	Input Bias Current	V_I = 0V, R_S = 50KΩ		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	$+V_I$ = Gnd, $-V_I$ = 15V, I_{St} = -3mA, R_S = 50Ω	(Notes 8, 13)	14		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	-28V ≤ $-V_{CC}$ ≤ -0.5V, R_S = 50Ω, 2V ≤ $+V_{CC}$ ≤ 29.5V, R_S = 50Ω, -14.5V ≤ V_{CM} ≤ 13V, R_S = 50Ω		80		dB	1, 2, 3

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OL}	Low Level Output Voltage	$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = 0.71V, V_{ID} = -6mV			0.4	V	1, 2, 3
		$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = –1.75V, V_{ID} = -6mV			0.4	V	1, 2, 3
		I_O = 50mA, $\pm V_I$ = 13V, V_{ID} = -5mV			1.5	V	1, 2, 3
		I_O = 50mA, $\pm V_I$= -14V, V_{ID} = -5mV			1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_L	Input Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = +12V, $-V_I$ = -17V	(Note 11)	-5.0	500	nA	1, 2, 3
		$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = -17V, $-V_I$ = +12V	(Note 11)	-5.0	500	nA	1, 2, 3
$+I_{CC}$	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient Input Offset Voltage	25°C ≤ T ≤ 125°C	(Notes 11, 13)	-25	25	µV/°C	2
		-55°C ≤ T ≤ 25°C	(Notes 11, 13)	-25	25	µV/°C	3
$\Delta I_{IO} / \Delta T$	Temperature Coefficient Input Offset Current	25°C ≤ T ≤ 125°C	(Notes 11, 13)	-100	100	pA/°C	2
		-55°C ≤ T ≤ 25°C	(Notes 11, 13)	-200	200	pA/°C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V	(Note 10)		200	mA	1
			(Note 10)		150	mA	2
			(Note 10)		250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	(Note 6)	10		V/mV	4
			(Note 6)	8.0		V/mV	5, 6

AC Parameters SMD 5962-8687701

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV	(Note 13)		300	nS	7, 8B
			(Note 13)		640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV	(Note 13)		300	nS	7, 8B
			(Note 13)		500	nS	8A

LM111 RADIATION Electrical Characteristics SMD 5962L0052401

DC Parameters (Note 12)

The following conditions apply, unless otherwise specified. $V_{CC} = \pm 15V$, $V_{CM} = 0$

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$V_I = 0V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_I = 0V$, $V_{CM} = -14.5V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_I = 0V$, $V_{CM} = +13V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC} = +2.5V$, $-V_{CC} = -2.5V$, $V_I = 0V$, $R_S = 50\Omega$		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
V_{IO} R	Raised Input Offset Voltage	$V_I = 0V$, $R_S = 50\Omega$	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_I = 0V$, $V_{CM} = -14.5V$, $R_S = 50\Omega$	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_I = 0V$, $V_{CM} = +13V$, $R_S = 50\Omega$	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	$V_I = 0V$, $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_I = 0V$, $V_{CM} = -14.5V$, $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_I = 0V$, $V_{CM} = +13V$, $R_S = 50K\Omega$		-10	+10	nA	1, 2
				-20	+20	nA	3
I_{IO}R	Raised Input Offset Current	$V_I = 0V$, $R_S = 50K\Omega$	(Note 15)	-25	+25	nA	1, 2
				-50	+50	nA	3
$\pm I_{IB}$	Input Bias Current	$V_I = 0V$, $R_S = 50K\Omega$		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		$+V_{CC} = 29.5V$, $-V_{CC} = -0.5V$, $V_I = 0V$, $V_{CM} = -14.5V$, $R_S = 50K\Omega$		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		$+V_{CC} = 2V$, $-V_{CC} = -28V$, $V_I = 0V$, $V_{CM} = +13V$, $R_S = 50K\Omega$		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	$+V_I$ = Gnd, $-V_I = 15V$, $I_{St} = -3mA$, $R_S = 50\Omega$	(Notes 8, 13)	14		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	$-28V \le -V_{CC} \le -0.5V$, $R_S = 50\Omega$, $2V \le +V_{CC} \le 29.5V$, $R_S = 50\Omega$, $-14.5V \le V_{CM} \le 13V$, $R_S = 50\Omega$		80		dB	1, 2, 3

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OL}	Low Level Output Voltage	$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = 0.5V, V_{ID} = -6mV			0.4	V	1, 2, 3
		$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = 3V, V_{ID} = -6mV			0.4	V	1, 2, 3
		I_O = 50mA, $\pm V_I$ = 13V, V_{ID} = -5mV			1.5	V	1, 2, 3
		I_O = 50mA, $\pm V_I$ = -14V, V_{ID} = -5mV			1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_L	Input Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = +12V, $-V_I$ = -17V	(Note 11)	-5.0	500	nA	1, 2, 3
		$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = -17V, $-V_I$ = +12V	(Note 11)	-5.0	500	nA	1, 2, 3
$+I_{CC}$	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
ΔV_{IO} / ΔT	Temperature Coefficient Input Offset Voltage	25°C ≤ T ≤ 125°C		-25	25	µV/°C	2
		-55°C ≤ T ≤ 25°C		-25	25	µV/°C	3
ΔI_{IO} / ΔT	Temperature Coefficient Input Offset Current	25°C ≤ T ≤ 125°C		-100	100	pA/°C	2
		-55°C ≤ T ≤ 25°C		-200	200	pA/°C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V	(Note 10)		200	mA	1
			(Note 10)		150	mA	2
			(Note 10)		250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	(Note 6)	10		V/mV	4
			(Note 6)	8.0		V/mV	5, 6

AC Parameters SMD 5962L0052401 (Note 12)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV	(Note 13)		300	nS	7, 8B
					640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV	(Note 13)		300	nS	7, 8B
					500	nS	8A

DC DELTA Parameters SMD 5962L0052401 (Note 12)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-12.5	12.5	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-5.0	5.0	nA	1

Post Radiation Parameters SMD 5962L0052401 (Note 12)

The following conditions apply, unless otherwise specified

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
I_{IO}	Input Offset Current	$+V_{CC}$ = 29.5V, $-V_{CC}$ = −0.5V, V_I = 0V, V_{CM} = −14.5V, R_S = 50KΩ		−50	+50	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = −28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		−50	+50	nA	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		−150	0.1	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = −0.5V, V_I = 0V, V_{CM} = −14.5V, R_S = 50KΩ		−175	0.1	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = −18V, V_O = 32V		−25	+25	nA	1

LM111 RADIATION Electrical Characteristics SMD 5962R0052402

DC Parameters (Note 14)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
		$+V_{CC}$ = +2.5V, $-V_{CC}$ = -2.5V, V_I = 0V, R_S = 50Ω		-3.0	+3.0	mV	1
				-4.0	+4.0	mV	2, 3
V_{IO} R	Raised Input Offset Voltage	V_I = 0V, R_S = 50Ω	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω	(Note 15)	-3.0	+3.0	mV	1
				-4.5	+4.5	mV	2, 3
I_{IO}	Input Offset Current	V_I = 0V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
I_{IO}R	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	(Note 15)	-25	+25	nA	1, 2
				-50	+50	nA	3
±I_{IB}	Input Bias Current	V_I = 0V, R_S = 50KΩ		-100	0.1	nA	1, 2
				-150	0.1	nA	3
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-150	0.1	nA	1, 2
				-200	0.1	nA	3
V_OSt	Collector Output Voltage (Strobe)	$+V_I$ = Gnd, $-V_I$ = 15V, I_{St} = -3mA, R_S = 50Ω	(Notes 8, 13)	14		V	1, 2, 3
CMRR	Common Mode Rejection Ratio	-28V ≤ $-V_{CC}$ ≤ -0.5V, R_S = 50Ω, 2V ≤ $+V_{CC}$ ≤ 29.5V, R_S = 50Ω, -14.5V ≤ V_{CM} ≤ 13V, R_S = 50Ω		80		dB	1, 2, 3

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{OL}	Low Level Output Voltage	$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = 0.5V, V_{ID} = -6mV			0.4	V	1, 2, 3
		$+V_{CC}$ = 4.5V, $-V_{CC}$ = Gnd, I_O = 8mA, $\pm V_I$ = 3V, V_{ID} = -6mV			0.4	V	1, 2, 3
		I_O = 50mA, $\pm V_I$ = 13V, V_{ID} = -5mV			1.5	V	1, 2, 3
		I_O = 50mA, $\pm V_I$ = -14V, V_{ID} = -5mV			1.5	V	1, 2, 3
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-1.0	10	nA	1
				-1.0	500	nA	2
I_L	Input Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = +12V, $-V_I$ = -17V	(Note 11)	-5.0	500	nA	1, 2, 3
		$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, $+V_I$ = -17V, $-V_I$ = +12V	(Note 11)	-5.0	500	nA	1, 2, 3
$+I_{CC}$	Power Supply Current				6.0	mA	1, 2
					7.0	mA	3
$-I_{CC}$	Power Supply Current			-5.0		mA	1, 2
				-6.0		mA	3
$\Delta V_{IO} / \Delta T$	Temperature Coefficient Input Offset Voltage	25°C ≤ T ≤ 125°C		-25	25	µV/°C	2
		-55°C ≤ T ≤ 25°C		-25	25	µV/°C	3
$\Delta I_{IO} / \Delta T$	Temperature Coefficient Input Offset Current	25°C ≤ T ≤ 125°C		-100	100	pA/°C	2
		-55°C ≤ T ≤ 25°C		-200	200	pA/°C	3
I_{OS}	Short Circuit Current	V_O = 5V, t ≤ 10mS, $-V_I$ = 0.1V, $+V_I$ = 0V	(Note 10)		200	mA	1
			(Note 11)		150	mA	2
			(Note 11)		250	mA	3
$+V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω		5.0		mV	1
$-V_{IO}$ adj.	Input Offset Voltage (Adjustment)	V_O = 0V, V_I = 0V, R_S = 50Ω			-5.0	mV	1
$\pm A_{VE}$	Voltage Gain (Emitter)	R_L = 600Ω	(Note 7)	10		V/mV	4
			(Note 7)	8.0		V/mV	5, 6

AC Parameters SMD 5962R0052402 (Note 14)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
tR_{LHC}	Response Time (Collector Output)	V_{OD}(Overdrive) = -5mV, C_L = 50pF, V_I = -100mV	(Note 13)		300	nS	7, 8B
					640	nS	8A
tR_{HLC}	Response Time (Collector Output)	V_{OD}(Overdrive) = 5mV, C_L = 50pF, V_I = 100mV	(Note 13)		300	nS	7, 8B
					500	nS	8A

DC DELTA Parameters SMD 5962R0052402 (Note 14)

The following conditions apply, unless otherwise specified. V_{CC} = ±15V, V_{CM} = 0

Delta calculations performed on QMLV devices at group B , subgroup 5.

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	V_I = 0V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50Ω		-0.5	0.5	mV	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50Ω		-0.5	0.5	mV	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = -0.5V, V_I = 0V, V_{CM} = -14.5V, R_S = 50KΩ		-12.5	12.5	nA	1
		$+V_{CC}$ = 2V, $-V_{CC}$ = -28V, V_I = 0V, V_{CM} = +13V, R_S = 50KΩ		-12.5	12.5	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = -18V, V_O = 32V		-5.0	5.0	nA	1

Post Radiation Parameters SMD 5962R0052402 (Note 14)

The following conditions apply, unless otherwise specified

Symbol	Parameter	Conditions	Notes	Min	Max	Unit	Sub-groups
$I_{IO}R$	Raised Input Offset Current	V_I = 0V, R_S = 50KΩ	(Note 15)	–100	+100	nA	1
$\pm I_{IB}$	Input Bias Current	V_I = 0V, R_S = 50KΩ		–180	0.1	nA	1
		$+V_{CC}$ = 29.5V, $-V_{CC}$ = –0.5V, V_I = 0V, V_{CM} = –14.5V, R_S = 50KΩ		–225	0.1	nA	1
I_{CEX}	Output Leakage Current	$+V_{CC}$ = 18V, $-V_{CC}$ = –18V, V_O = 32V		–1.0	+25	nA	1

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: This rating applies for ±15V supplies. The positive input voltage limits is 30 V above the negative supply. The negative input voltage limits is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 5: Human body model, 1.5 kΩ in series with 100 pF.

Note 6: Datalog reading in K=V/mV.

Note 7: Pin names based on an 8 pin package configuration. When using higher pin count packages then: Pin 2 & 3 are Inputs, Pin 5 is Balance, Pin 6 is Balance / Strobe, Pin 7 is Output, and Pin 8 is V^+. For example: $V_{56}$is the Voltage between the Balance and Balance / Strobe pins

Note 8: I_{ST} = –2mA at –55°C

Note 9: Calculated parameter.

Note 10: Actual min. limit used is 5mA due to test setup.

Note 11: V_{ID} is voltage difference between inputs.

Note 12: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be dose rate sensitive in a space environment and demonstrate enhanced low dose rate effect. Radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in Mil-Std-883, Method 1019, Condition A.

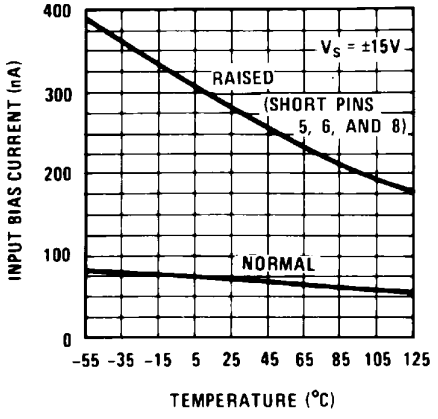
Note 13: Group A sample ONLY

Note 14: Pre and post irradiation limits are identical to those listed under AC and DC electrical characteristics except as listed in the Post Radiation Limits Table. These parts may be sensitive in a high dose environment. Low dose rate testing has been performed on a wafer-by-wafer basis, per test method 1019 condition D of MIL-STD-883, with no enhanced low dose rate sensitivity (ELDRS) effect.

Note 15: Subscript (R) indicates tests which are performed with input stage current raised by connecting BAL and BAL/STB terminals to $+V_{CC}$.

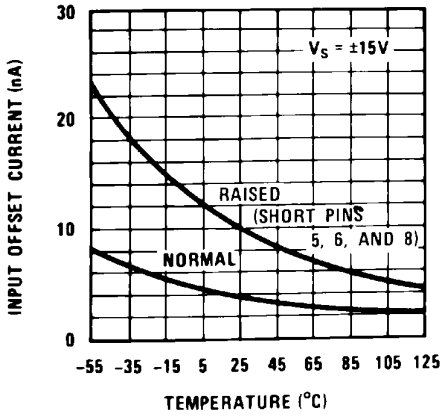
LM111 Typical Performance Characteristics

Input Bias Current



20128543

Input Bias Current



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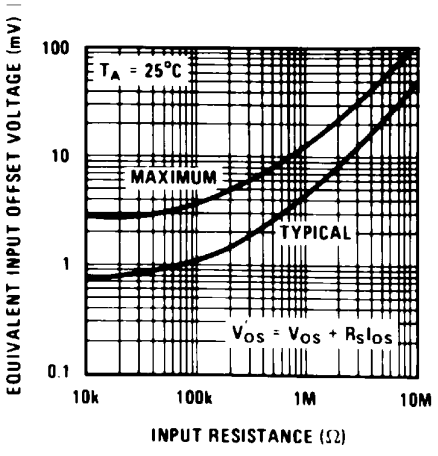
Input Bias Current



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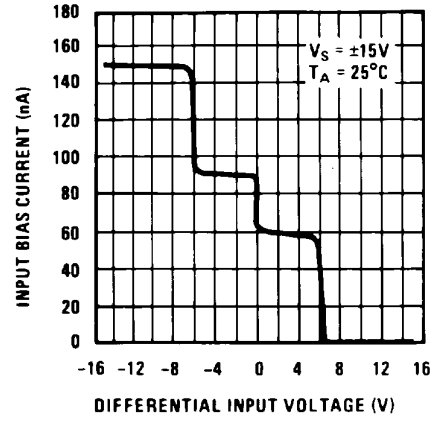
Input Bias Current



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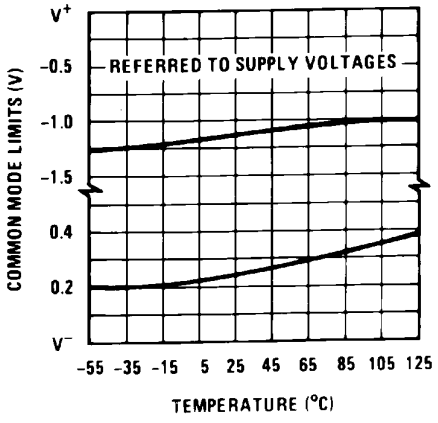
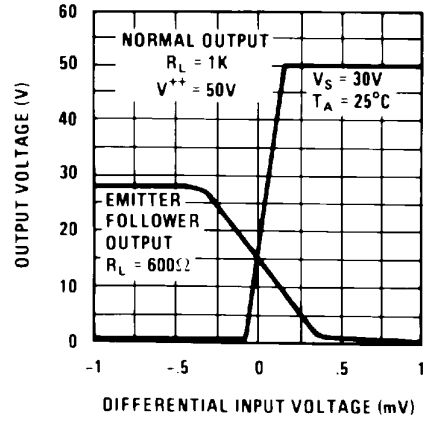
Input Bias Current



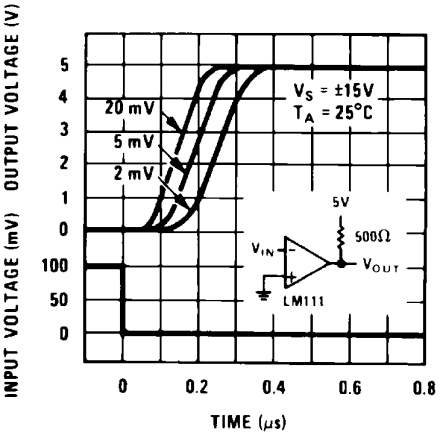
20128547

Input Bias Current



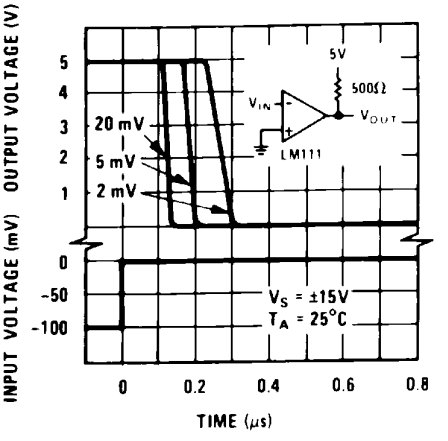
20128548

Input Bias Current
Input Overdrives



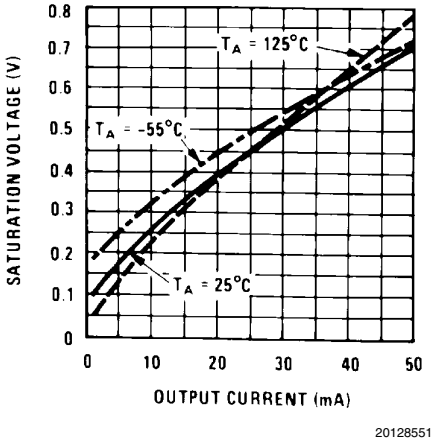
20128549

Input Bias Current
Input Overdrives



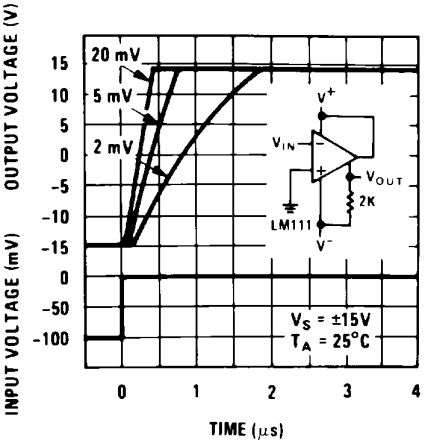
20128550

Input Bias Current



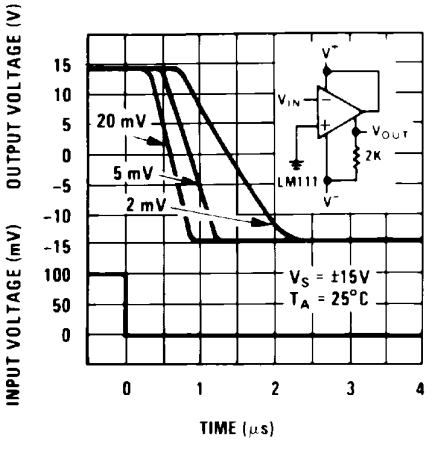
20128551

Response Time for Various
Input Overdrives



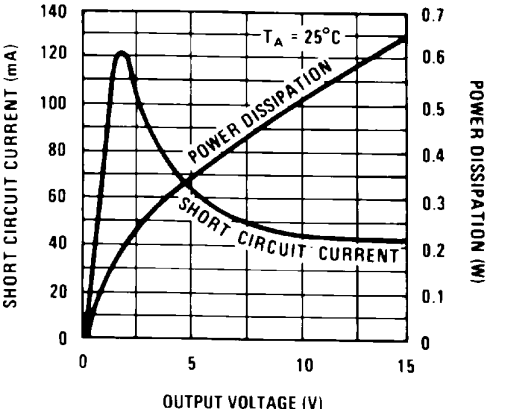
20128552

Response Time for Various
Input Overdrives



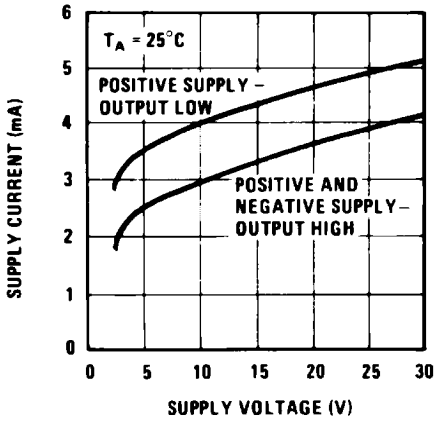
20128553

Output Limiting Characteristics



20128554

Supply Current



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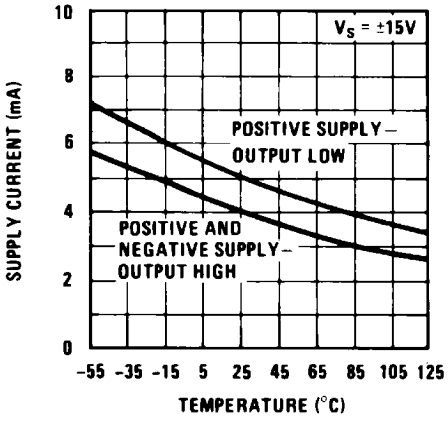
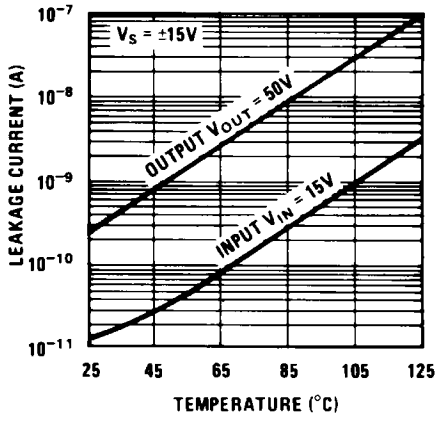
Supply Current



20128556

Leakage Currents



20128557

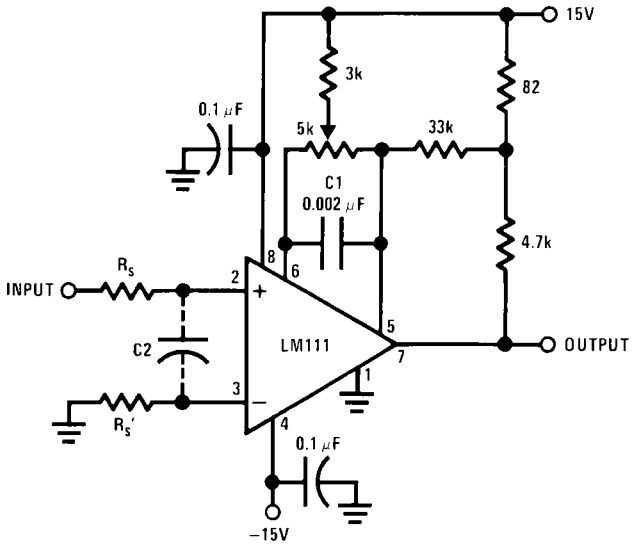
Application Hints

CIRCUIT TECHNIQUES FOR AVOIDING OSCILLATIONS IN COMPARATOR APPLICATIONS

When a high-speed comparator such as the LM111 is used with fast input signals and low source impedances, the output response will normally be fast and stable, assuming that the power supplies have been bypassed (with 0.1 µF disc capacitors), and that the output signal is routed well away from the inputs (pins 2 and 3) and also away from pins 5 and 6.

However, when the input signal is a voltage ramp or a slow sine wave, or if the signal source impedance is high (1 kΩ to 100 kΩ), the comparator may burst into oscillation near the crossing-point. This is due to the high gain and wide bandwidth of comparators like the LM111. To avoid oscillation or instability in such a usage, several precautions are recommended, as shown in *Figure 1* below.

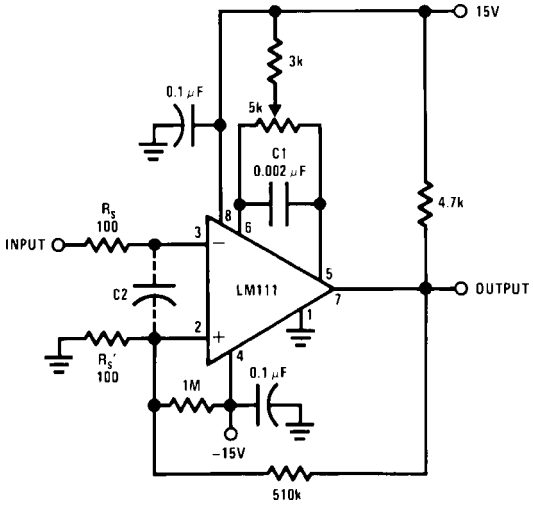
1. The trim pins (pins 5 and 6) act as unwanted auxiliary inputs. If these pins are not connected to a trim-pot, they should be shorted together. If they are connected to a trim-pot, a 0.01 µF capacitor C1 between pins 5 and 6 will minimize the susceptibility to AC coupling. A smaller capacitor is used if pin 5 is used for positive feedback as in *Figure 1*.
2. Certain sources will produce a cleaner comparator output waveform if a 100 pF to 1000 pF capacitor C2 is connected directly across the input pins.
3. When the signal source is applied through a resistive network, R_S, it is usually advantageous to choose an $R_S{}'$ of substantially the same value, both for DC and for dynamic (AC) considerations. Carbon, tin-oxide, and metal-film resistors have all been used successfully in comparator input circuitry. Inductive wire wound resistors are not suitable.
4. When comparator circuits use input resistors (e.g. summing resistors), their value and placement are particularly important. In all cases the body of the resistor should be close to the device or socket. In other words there should be very little lead length or printed-circuit foil run between comparator and resistor to radiate or pick up signals. The same applies to capacitors, pots, etc. For example, if R_S=10 kΩ, as little as 5 inches of lead between the resistors and the input pins can result in oscillations that are very hard to damp. Twisting these input leads tightly is the only (second best) alternative to placing resistors close to the comparator.
5. Since feedback to almost any pin of a comparator can result in oscillation, the printed-circuit layout should be engineered thoughtfully. Preferably there should be a ground plane under the LM111 circuitry, for example, one side of a double-layer circuit card. Ground foil (or, positive supply or negative supply foil) should extend between the output and the inputs, to act as a guard. The foil connections for the inputs should be as small and compact as possible, and should be essentially surrounded by ground foil on all sides, to guard against capacitive coupling from any high-level signals (such as the output). If pins 5 and 6 are not used, they should be shorted together. If they are connected to a trim-pot, the trim-pot should be located, at most, a few inches away from the LM111, and the 0.01 µF capacitor should be installed. If this capacitor cannot be used, a shielding printed-circuit foil may be advisable between pins 6 and 7. The power supply bypass capacitors should be located within a couple inches of the LM111. (Some other comparators require the power-supply bypass to be located immediately adjacent to the comparator.)
6. It is a standard procedure to use hysteresis (positive feedback) around a comparator, to prevent oscillation, and to avoid excessive noise on the output because the comparator is a good amplifier for its own noise. In the circuit of *Figure 2*, the feedback from the output to the positive input will cause about 3 mV of hysteresis. However, if R_S is larger than 100Ω, such as 50 kΩ, it would not be reasonable to simply increase the value of the positive feedback resistor above 510 kΩ. The circuit of *Figure 3* could be used, but it is rather awkward. See the notes in paragraph 7 below.
7. When both inputs of the LM111 are connected to active signals, or if a high-impedance signal is driving the positive input of the LM111 so that positive feedback would be disruptive, the circuit of *Figure 1* is ideal. The positive feedback is to pin 5 (one of the offset adjustment pins). It is sufficient to cause 1 to 2 mV hysteresis and sharp transitions with input triangle waves from a few Hz to hundreds of kHz. The positive-feedback signal across the 82Ω resistor swings 240 mV below the positive supply. This signal is centered around the nominal voltage at pin 5, so this feedback does not add to the V_{OS} of the comparator. As much as 8 mV of V_{OS} can be trimmed out, using the 5 kΩ pot and 3 kΩ resistor as shown.
8. These application notes apply specifically to the LM111 and are applicable to all high-speed comparators in general, (with the exception that not all comparators have trim pins).



20128529

Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 1. Improved Positive Feedback



20128530

Pin connections shown are for LM111H in the H08 hermetic package

FIGURE 2. Conventional Positive Feedback

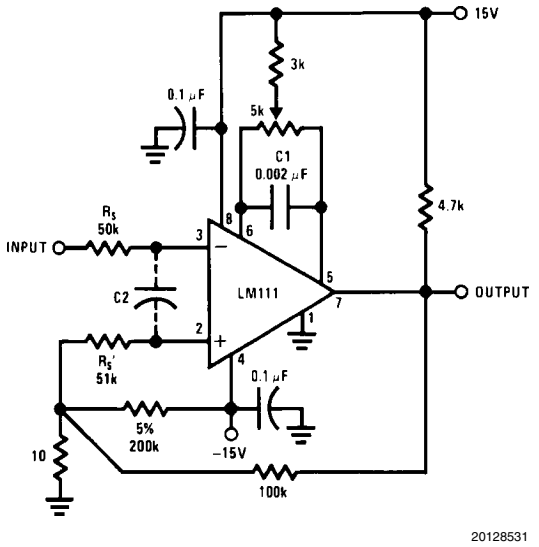
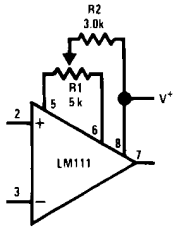


FIGURE 3. Positive Feedback with High Source Resistance

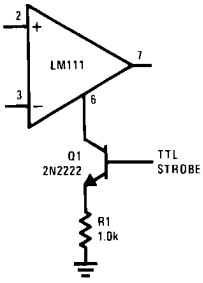
Typical Applications (Note 18)

Offset Balancing



20128536

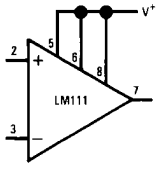
Strobing



20128537

Note: Do Not Ground Strobe Pin. Output is turned off when current is pulled from Strobe Pin.

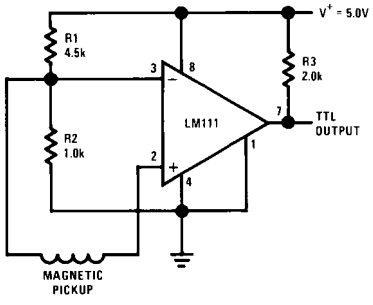
Increasing Input Stage Current (Note Increases typical common mode slew from 7.0V/µs to 18V/µs.)



20128538

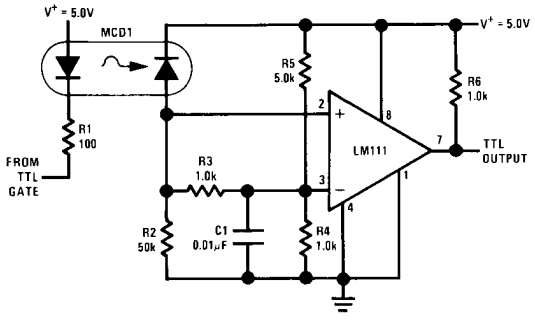
Note 16: Increases typical common mode slew from 7.0V/µs to 18V/µs.

Detector for Magnetic Transducer



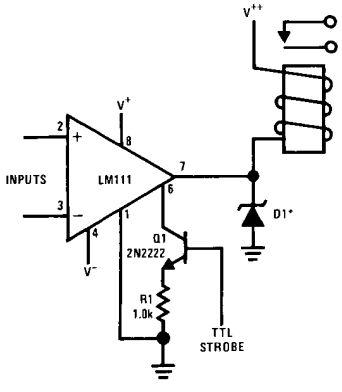
20128539

Digital Transmission Isolator



20128540

Relay Driver with Strobe

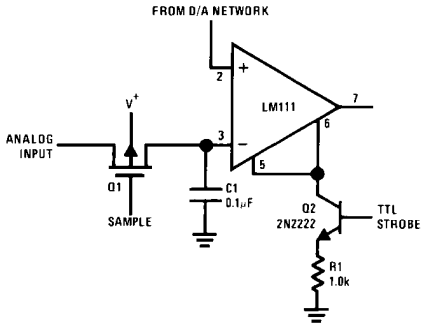


20128541

*Absorbs inductive kickback of relay and protects IC from severe voltage transients on V++ line.

Note: Do Not Ground Strobe Pin.

Strobing off Both Input and Output Stages (Note Typical input current is 50 pA with inputs strobed off.)



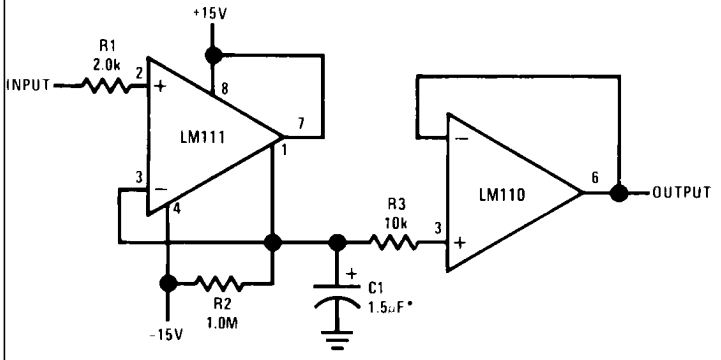
20128542

Note: Do Not Ground Strobe Pin.

Note 17: Typical input current is 50 pA with inputs strobed off.

Note 18: Pin connections shown on schematic diagram and typical applications are for H08 metal can package.

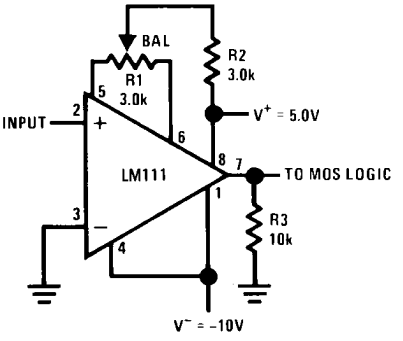
Positive Peak Detector



20128523

*Solid tantalum

Zero Crossing Detector Driving MOS Logic

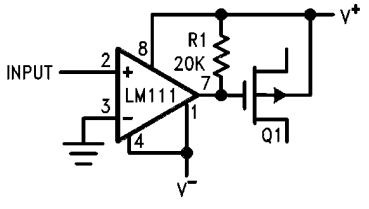


20128524

Typical Applications for H08 Package

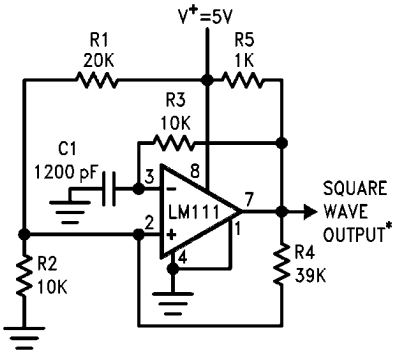
(Pin numbers refer to H08 package)

Zero Crossing Detector Driving MOS Switch



20128513

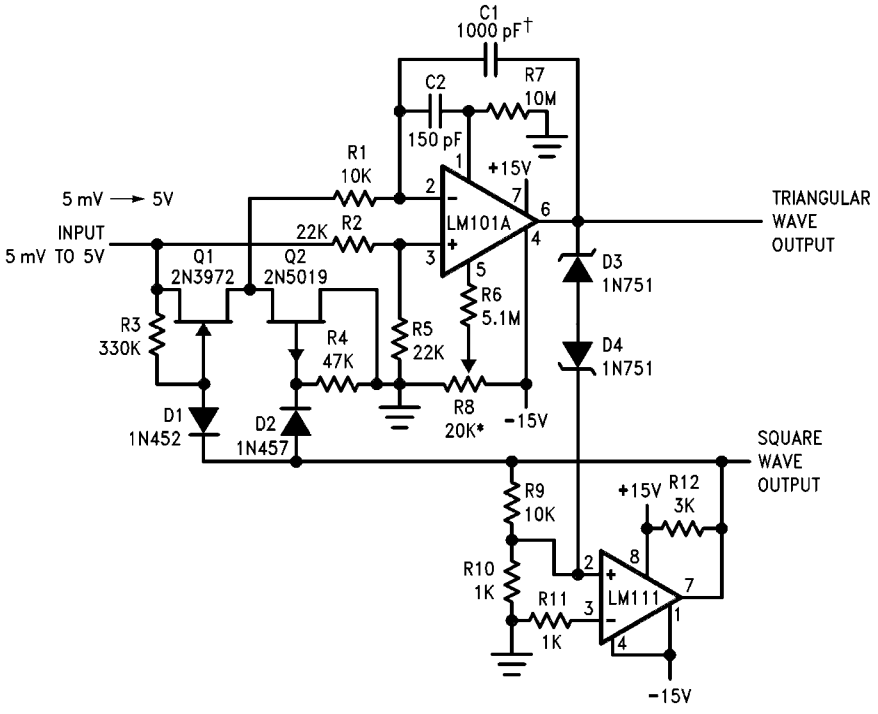
100 kHz Free Running Multivibrator



20128514

*TTL or DTL fanout of two

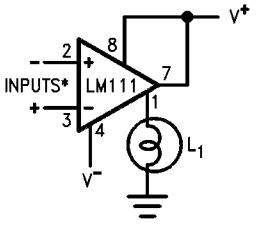
10 Hz to 10 kHz Voltage Controlled Oscillator



20128515

*Adjust for symmetrical square wave time when V_{IN} = 5 mV
†Minimum capacitance 20 pF Maximum frequency 50 kHz

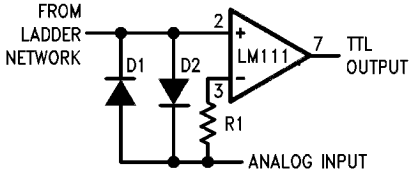
Driving Ground-Referred Load



20128516

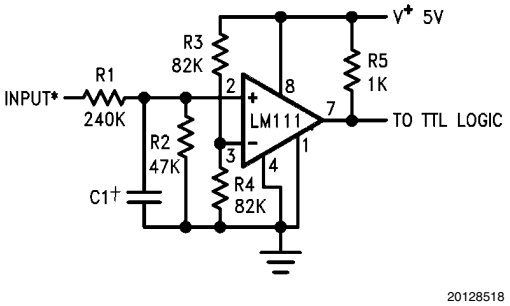
*Input polarity is reversed when using pin 1 as output.

Using Clamp Diodes to Improve Response



20128517

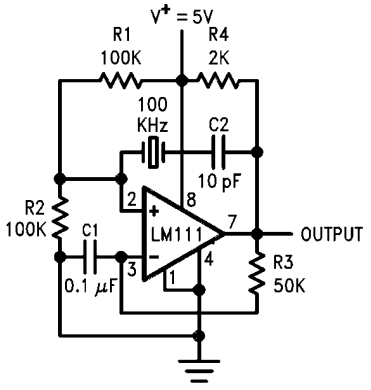
TTL Interface with High Level Logic



20128518

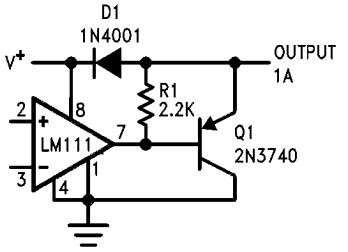
*Values shown are for a 0 to 30V logic swing and a 15V threshold.
†May be added to control speed and reduce susceptibility to noise spikes.

Crystal Oscillator



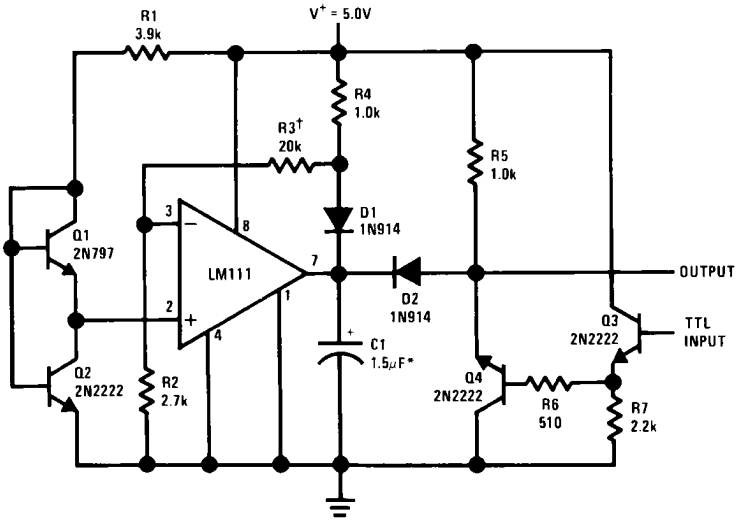
20128519

Comparator and Solenoid Driver



20128520

Precision Squarer

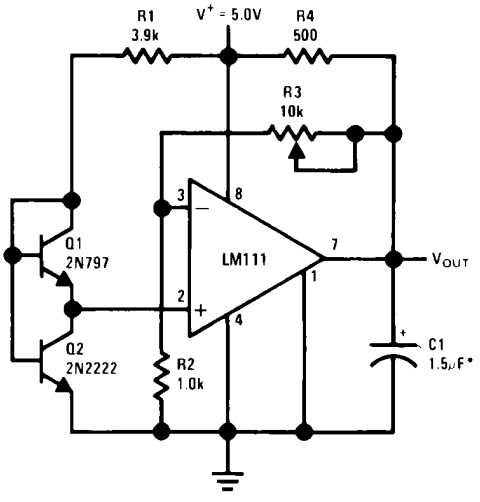


20128521

*Solid tantalum

†Adjust to set clamp level

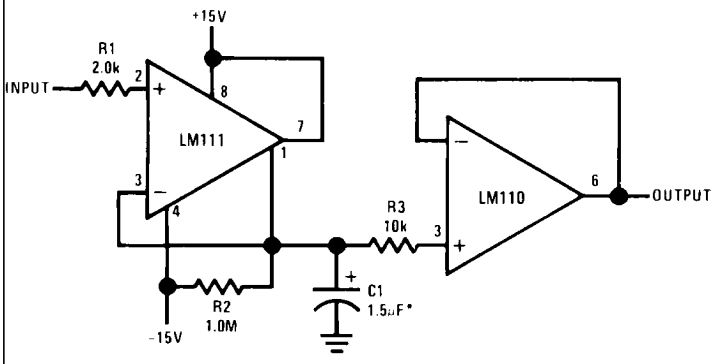
Low Voltage Adjustable Reference Supply



20128522

*Solid tantalum

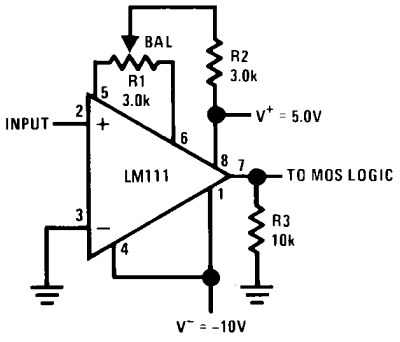
Positive Peak Detector



20128523

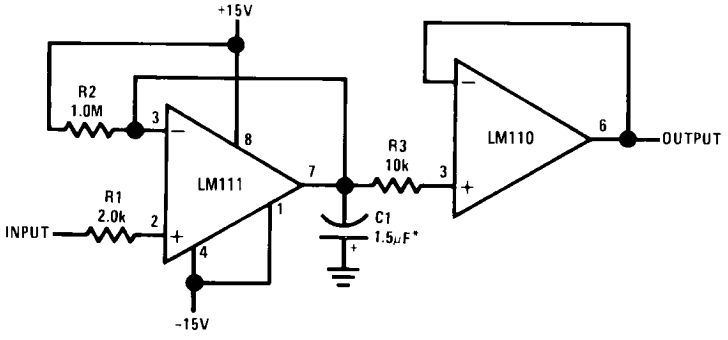
*Solid tantalum

Zero Crossing Detector Driving MOS Logic



20128524

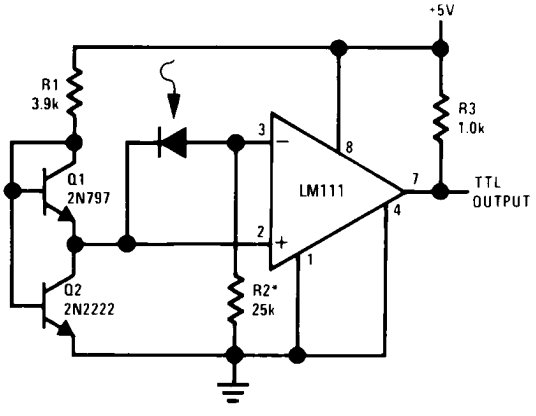
Negative Peak Detector



20128525

*Solid tantalum

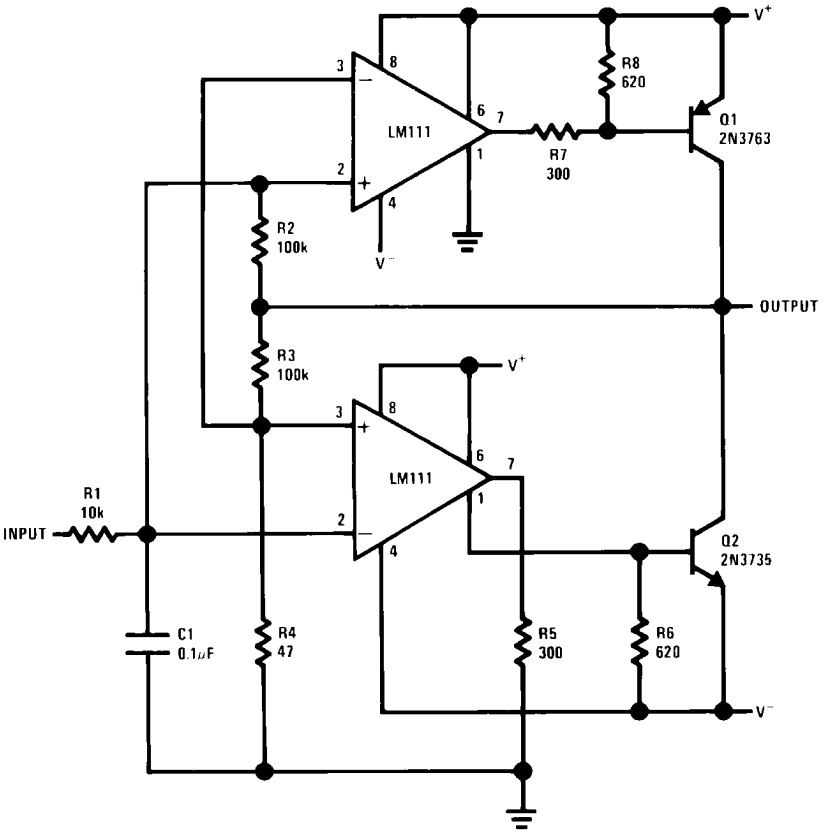
Precision Photodiode Comparator



20128526

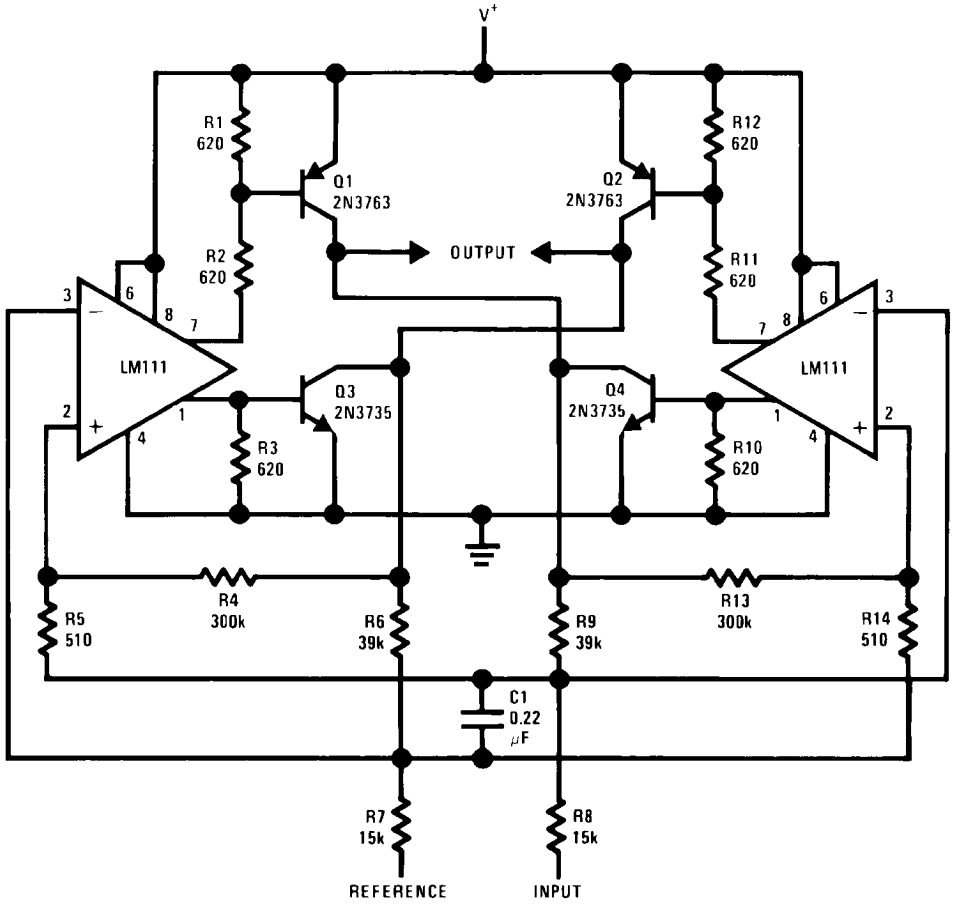
*R2 sets the comparison level. At comparison, the photodiode has less than 5 mV across it, decreasing leakages by an order of magnitude.

Switching Power Amplifier



20128527

Switching Power Amplifier

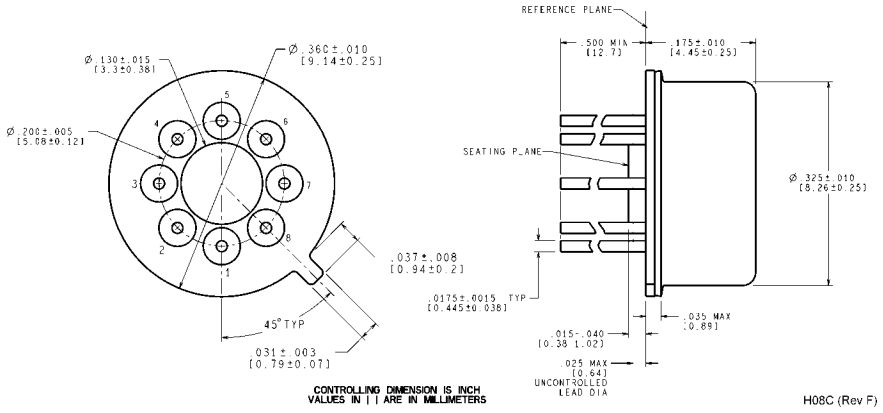


20128528

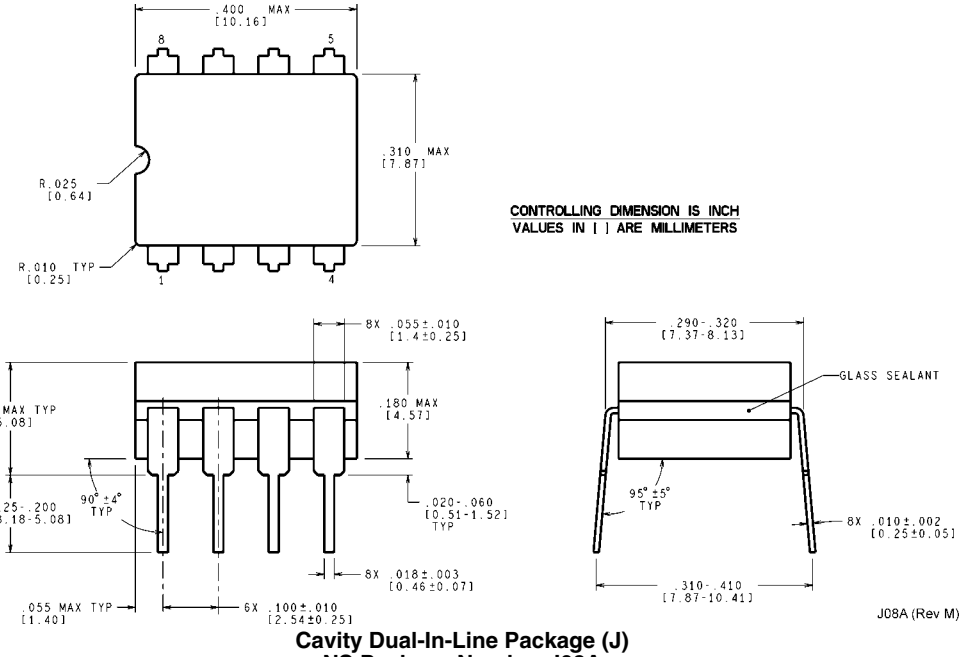
Revision History

Released	Revision	Section	Originator	Changes
10/11/05	A	New Release, Corporate format	L. Lytle	3 MDS data sheets converted into one Corp. data sheet format. MNLM111-X Rev 0A0, MDLM111-X Rev. 0B0, and MRLM111-X-RH Rev 0E1. The drift table was eliminated from the 883 section since it did not apply; Note #3 was removed from RH & QML datasheets with SG verification that it no longer applied. Added NSID's for 50k Rad and Post Radiation Table. MDS data sheets will be archived.
12/14/05	B	Ordering Information Table	R. Malone	Removed NSID reference LM111J-8PQMLV, 5962P0052401VPA 30k rd(Si). Reason: NSID on LTB, Inventory exhausted. Added following NSID's: LM111HPQMLV, LM111WPQMLV and LM111WGPQMLV. Reason: Still have Inventory. LM111QML, Revision A will be archived.
06/26/08	C	Features, Ordering Information Table, Electrical section Notes.	Larry McGee	Added Radiation reference, ELDRS NSID's and Note 14 and 15, Low Dose Electrical Table. Deleted 30k rd(Si) NSID's: LM111HPQMLV, LM111WPQMLV and LM111WGPQMLV. Reason: EOL 9/06/05. Revision B will be archived.

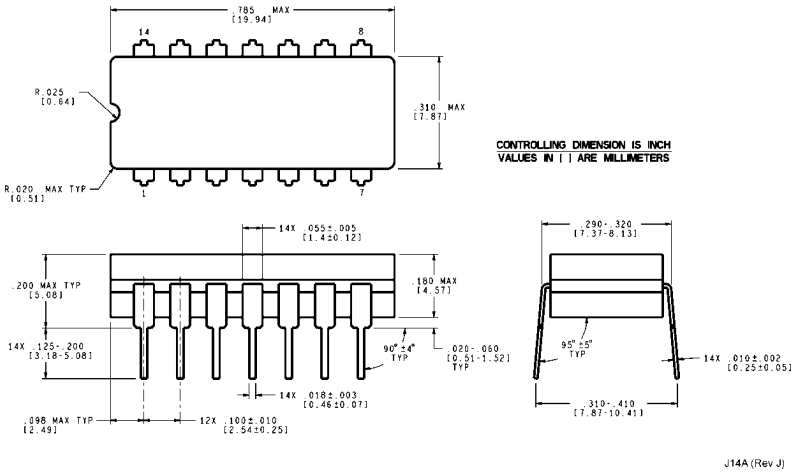
Physical Dimensions inches (millimeters) unless otherwise noted



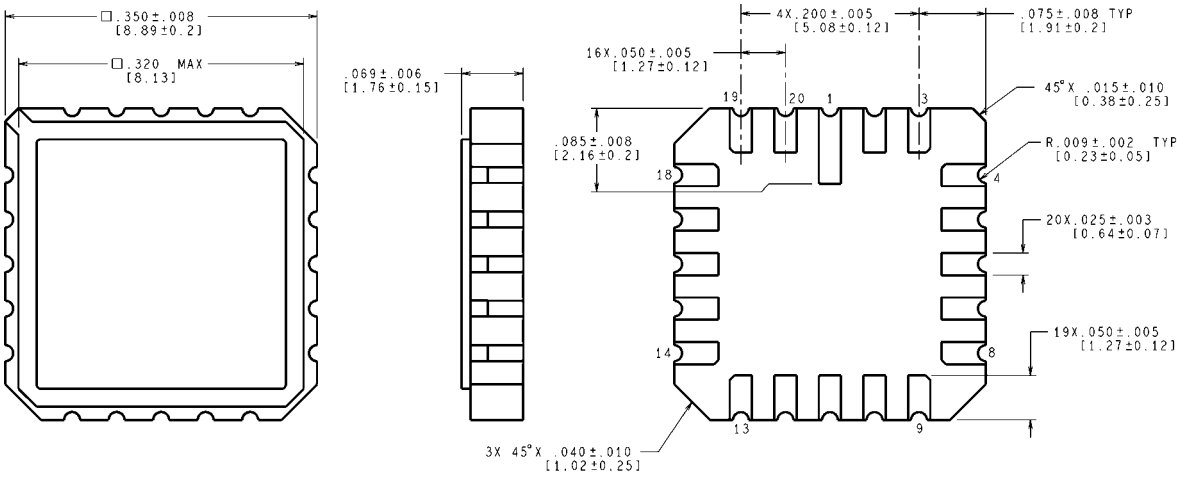
Metal Can Package (H)
NS Package Number H08C



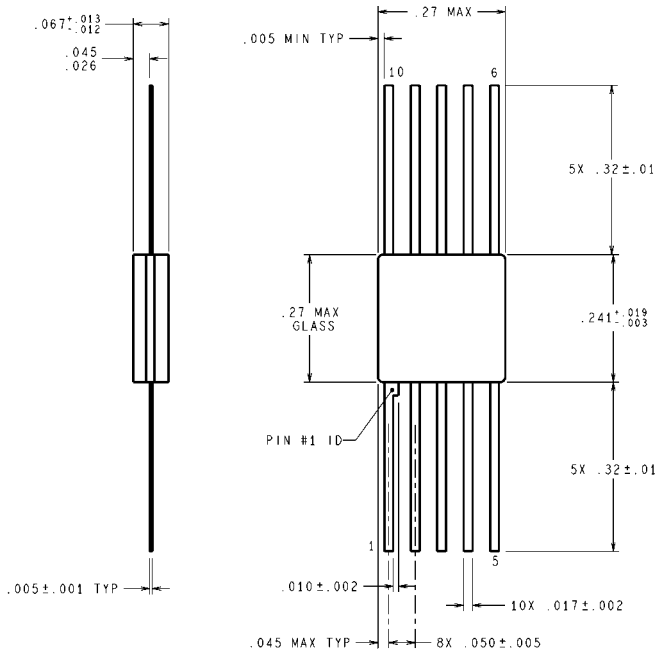
Cavity Dual-In-Line Package (J)
NS Package Number J08A



Dual-In-Line Package (J)
NS Package Number J14A



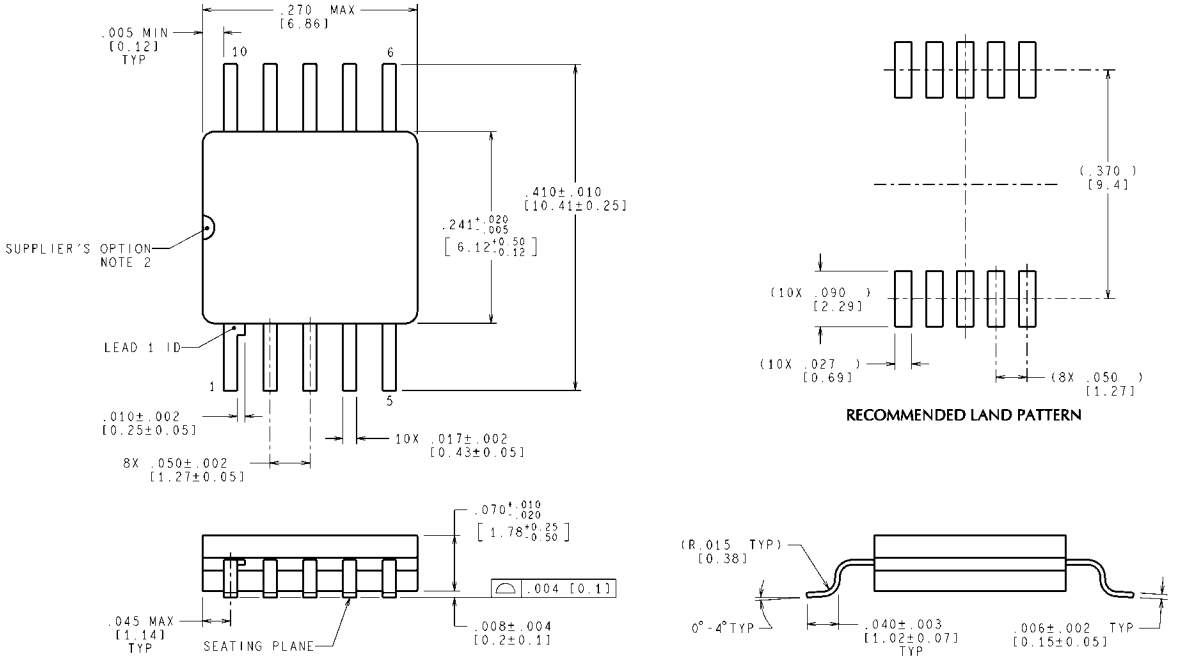
Leadless Chip Carrier (E)
NS Package Number E20A



DIMENSIONS ARE IN INCHES

W10A (Rev H)

Cerpack Package (W)
NS Package Number W10A



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Notes

Notes

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