1 TMS320F2802x (Piccolo™) MCUs

1.1 Features

- **High-Efficiency 32-Bit CPU (TMS320C28x™)**
  - **60 MHz (16.67-ns Cycle Time)**
  - **40 MHz (25-ns Cycle Time)**
  - **16 x 16 and 32 x 32 MAC Operations**
  - **16 x 16 Dual MAC**
  - **Harvard Bus Architecture**
  - **Atomic Operations**
  - **Fast Interrupt Response and Processing**
  - **Unified Memory Programming Model**
  - **Code-Efficient (in C/C++ and Assembly)**
- **Low Device and System Cost:**
  - **Single 3.3-V Supply**
  - **No Power Sequencing Requirement**
  - **Integrated Power-on Reset and Brown-out Reset**
  - **Small Packaging, as low as 38-pin available**
  - **Low Power**
  - **No Analog Support Pins**
- **Clocking:**
  - **2 Internal Zero-pin Oscillators**
  - **On-chip Crystal Oscillator/External Clock Input**
  - **Dynamic PLL Ratio Changes Supported**
  - **Watchdog Timer Module**
  - **Missing Clock Detection Circuitry**
- **Up to 22 Individually Programmable, Multiplexed GPIO Pins With Input Filtering**
- **Peripheral Interrupt Expansion (PIE) Block That Supports All Peripheral Interrupts**
- **Three 32-Bit CPU Timers**
- **On-Chip Memory**
  - **Flash, SARAM, OTP, Boot ROM Available**
- **128-Bit Security Key/Lock**
  - **Protects Secure Memory Blocks**
  - **Prevents Firmware Reverse Engineering**
- **Serial Port Peripherals**
  - **One SCI (UART) Module**
  - **One SPI Module**
  - **One Inter-Integrated-Circuit (I2C) Bus**
- **Advanced Emulation Features**
  - **Analysis and Breakpoint Functions**
  - **Real-Time Debug via Hardware**
- **Enhanced Control Peripherals**
  - **Enhanced Pulse Width Modulator (ePWM)**
  - **High-resolution PWM (HRPWM)**
  - **Enhanced Capture (eCAP)**
  - **Analog-to-Digital Converter (ADC)**
  - **Comparator**
- **2802x Packages**
  - **38-Pin DA Plastic Small Outline Package (PSOP)**
  - **48-Pin PT Plastic Quad Flatpack (PQFP)**

ADVANCE INFORMATION

1.2 Description

The F2802x Piccolo™ family of microcontrollers provides the power of the C28x™ core coupled with highly integrated control peripherals in low pin-count devices. This family is code compatible with previous C28-based code, as well as providing a high level of analog integration.

An internal voltage regulator allows for single rail operation. Enhancements have been made to the HRPWM module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from 0 to 3.3-V fixed full scale range and supports ratio-metric V_{REFHI}/V_{REFLO} references. The interface has been optimized for low overhead/latency.

1.3 Getting Started

This section gives a brief overview of the steps to take when first developing for a C28x device. For more detail on each of these steps, see the following:

- *Getting Started With TMS320C28x™ Digital Signal Controllers* (literature number SPRAAM0).
- C2000 Getting Started Website (http://www.ti.com/c2000getstarted)
- TMS320F28x MCU Development and Experimenter's Kits (http://www.ti.com/f28xkits)

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2 Hardware Features

Table 2-1. Hardware Features

FEATURE		TYPE(1)	28022 (40 MHz)	28023 (40 MHz)	28024 (40 MHz)	28025 (40 MHz)	28026 (60 MHz)	28027 (60 MHz)
Instruction cycle		–	25 ns	25 ns	25 ns	25 ns	16.67 ns	16.67 ns
On-chip flash (16-bit word)		–	16K	32K	16K	32K	16K	32K
On-chip SARAM (16-bit word)		–	6K	6K	6K	6K	6K	6K
Code security for on-chip flash/SARAM/OTP blocks		–	Yes	Yes	Yes	Yes	Yes	Yes
Boot ROM (8K X16)		–	Yes	Yes	Yes	Yes	Yes	Yes
One-time programmable (OTP) ROM (16-bit word)		–	1K	1K	1K	1K	1K	1K
ePWM modules		1	ePWM1/2/3/4	ePWM1/2/3/4	ePWM1/2/3/4	ePWM1/2/3/4	ePWM1/2/3/4	ePWM1/2/3/4
eCAP modules		0	eCAP1	eCAP1	eCAP1	eCAP1	eCAP1	eCAP1
Watchdog timer		–	Yes	Yes	Yes	Yes	Yes	Yes
12-Bit ADC	MSPS	3	3.07	3.07	3.07	3.07	4.6	4.6
	Conversion Time		325 ns	325 ns	325 ns	325 ns	216.67 ns	216.67 ns
	Channels		7	7	13	13	13	13
32-Bit CPU timers		–	3	3	3	3	3	3
HiRES ePWM Channels		1	4	4	4	4	4	4
Comparators w/ Integrated DACs		0	1	1	2	2	2	2
Inter-integrated circuit (I2C)		0	1	1	1	1	1	1
Serial Peripheral Interface (SPI)		1	1	1	1	1	1	1
Serial Communications Interface (SCI)		0	1	1	1	1	1	1
I/O pins (shared)	Digital	–	20	20	22	22	22	22
	Analog	–	6	6	6	6	6	6
External interrupts		–	3	3	3	3	3	3
Supply voltage (nominal)		–	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V
Packaging	48-Pin PT PQFP	–	–	–	Yes	Yes	Yes	Yes
	38-Pin DA PSOP	–	Yes	Yes	–	–	–	–
Temperature options	A: - 40°C to 85°C	–	Yes	Yes	Yes	Yes	Yes	Yes
	S: - 40°C to 125°C	–	–	–	Yes	Yes	–	–
Product status(2)		–	TMX	TMX	TMX	TMX	TMX	TMX

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (SPRU566) and in the peripheral reference guides.

(2) See Section 5.1, Device and Development Support Nomenclature for descriptions of device stages. TMX is an experimental device that is not necessarily representative of the final device's electrical specifications. TMS is a fully qualified production device.

2.1 Pin Assignments

Figure 2-1 shows the 48-pin PT plastic quad flatpack (PQFP) pin assignments. Figure 2-2 shows the 38-pin DA plastic small outline package (PSOP) pin assignments.

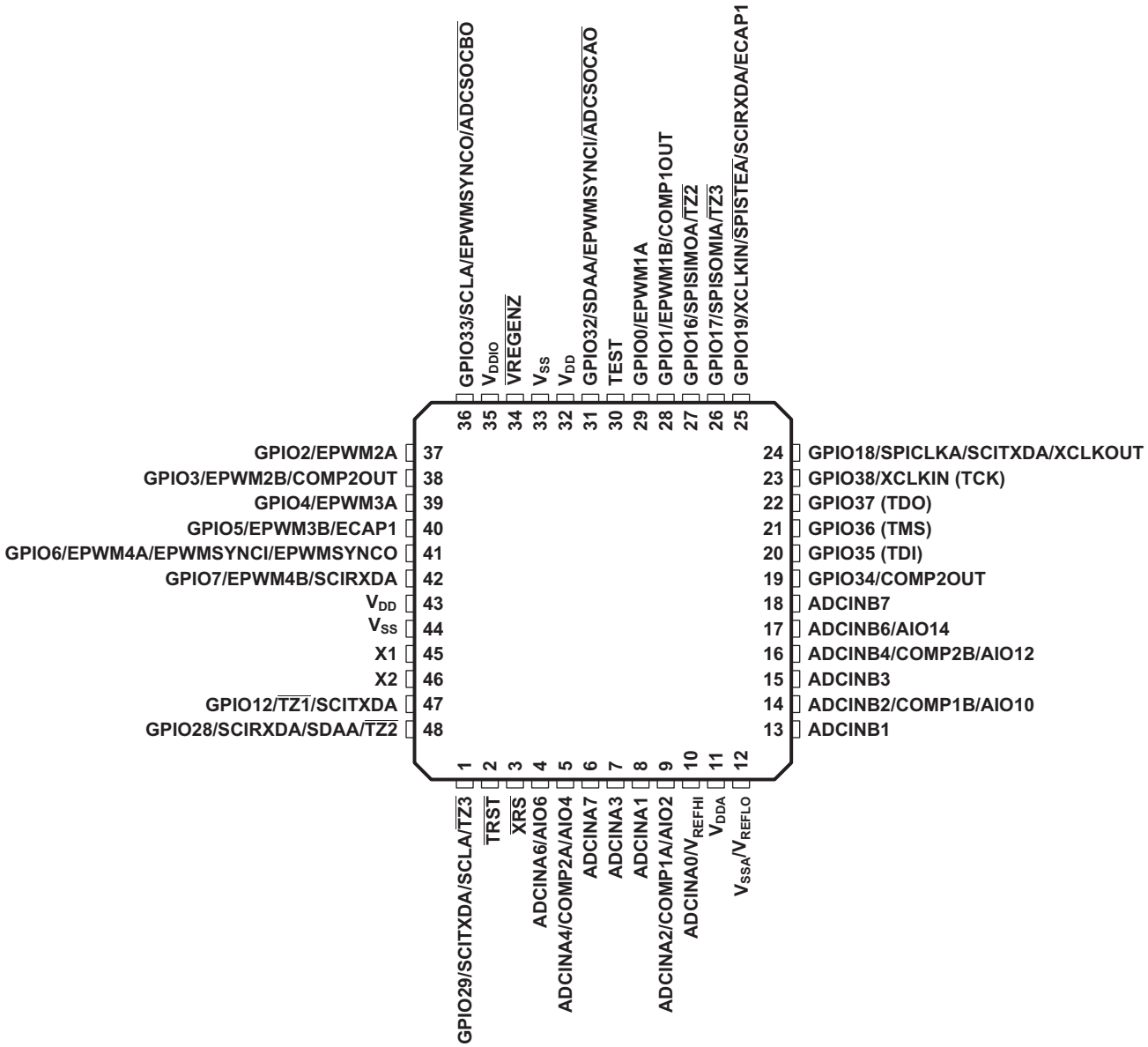

Figure 2-1. 2802x 48-Pin PT PQFP (top view)

ADVANCE INFORMATION

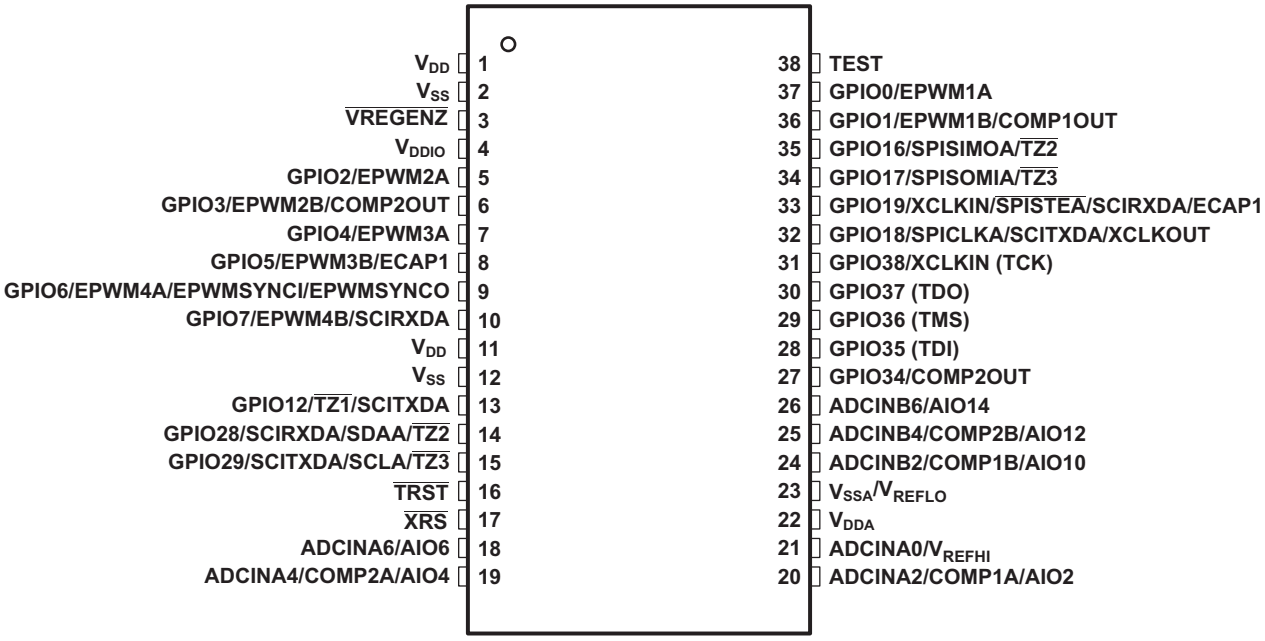

Figure 2-2. 2802x 38-Pin DA PSOP (top view)

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2.2 Signal Descriptions

Table 2-2. TERMINAL FUNCTIONS

TERMINAL			I/O/Z	DESCRIPTION
NAME	PT NO.	DA NO.		
JTAG				
$\overline{\text{TRST}}$	2	16	I	JTAG test reset with internal pulldown. $\overline{\text{TRST}}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. NOTE: $\overline{\text{TRST}}$ is an active high test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is recommended on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Since this is application-specific, it is recommended that each target board be validated for proper operation of the debugger and the application. (↓)
TCK	See GPIO38		I	See GPIO38. JTAG test clock with internal pullup (↑)
TMS	See GPIO36		I	See GPIO36. JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (↑)
TDI	See GPIO35		I	See GPIO35. JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑)
TDO	See GPIO37		O/Z	See GPIO37. JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (8 mA drive)
FLASH				
TEST	30	38	I/O	Test Pin. Reserved for TI. Must be left unconnected.
CLOCK				
XCLKOUT	See GPIO18		O/Z	See GPIO18. Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
XCLKIN	See GPIO19 and GPIO38		I	See GPIO19 and GPIO38. External oscillator input. Pin source for the clock is controlled by the XCLKINSEL bit in the XCLK register, GPIO38 is the default selection. This pin feeds a clock from an external 3.3-V oscillator. In this case, the X1 pin, if available, must be tied to GND and the on-chip crystal oscillator must be disabled via bit 14 in the CLKCTL register. If a crystal/resonator is used, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. Note: Designs that use the GPIO38/TCK/XCLKIN pin to supply an external clock for normal device operation may need to incorporate some hooks to disable this path during debug using the JTAG connector. This is to prevent contention with the TCK signal, which is active during JTAG debug sessions. The zero-pin internal oscillators may be used during this time to clock the device.
X1	45	–	I	On-chip crystal oscillator Input. To use this oscillator, a quartz crystal or a ceramic resonator must be connected across X1 and X2. In this case, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. If this pin is not used, it must be tied to GND. (I)
X2	46	–	O	On-chip crystal oscillator output. A quartz crystal or a ceramic resonator must be connected across X1 and X2. If X2 is not used, it must be left unconnected. (O)

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Table 2-2. TERMINAL FUNCTIONS (continued)

TERMINAL			I/O/Z	DESCRIPTION
NAME	PT NO.	DA NO.		
RESET				
$\overline{\text{XRS}}$	3	17	I/O	Device Reset (in) and Watchdog Reset (out). Piccolo devices have a built-in power-on-reset (POR) and brown-out-reset (BOR) circuitry. As such, no external circuitry is needed to generate a reset pulse. During a power-on or brown-out condition, this pin is driven low by the device. See the electrical section for thresholds of the POR/BOR block. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the $\overline{\text{XRS}}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. If need be, an external circuitry may also drive this pin to assert a device reset. In this case, it is recommended that this pin be driven by an open-drain device An R-C circuit must be connected to this pin for noise immunity reasons. Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3FFFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain with an internal pullup. (I/OD)
ADC, COMPARATOR, ANALOG I/O				
ADCINA7	6		I	ADC Group A, Channel 7 input
ADCINA6 AIO6	4	18	I I/O	ADC Group A, Channel 6 input Digital AIO 6
ADCINA4 COMP2A AIO4	5	19	I I I/O	ADC Group A, Channel 4 input Comparator Input 2A Digital AIO 4
ADCINA3	7	–	I	ADC Group A, Channel 3 input
ADCINA2 COMP1A AIO2	9	20	I I I/O	ADC Group A, Channel 2 input Comparator Input 1A Digital AIO 2
ADCINA1	8	–	I	ADC Group A, Channel 1 input
ADCINA0 VREFHI	10	21	I I	ADC Group A, Channel 0 input ADC External Reference – only used when in ADC external reference mode. See ADC Section.
ADCINB7	18	–	I	ADC Group B, Channel 7 input
ADCINB6 AIO14	17	26	I I/O	ADC Group B, Channel 6 input Digital AIO 14
ADCINB4 COMP2B AIO12	16	25	I I I/O	ADC Group B, Channel 4 input Comparator Input 2B Digital AIO12
ADCINB3	15	–	I	ADC Group B, Channel 3 input
ADCINB2 COMP1B AIO10	14	24	I I I/O	ADC Group B, Channel 2 input Comparator Input 1B Digital AIO 10
ADCINB1	13	–	I	ADC Group B, Channel 1 input
CPU AND I/O POWER				
V_{DDA}	11	22		Analog Power Pin
V_{SSA} V_{REFLO}	12	23	I	Analog Ground Pin ADC Low Reference (always tied to ground)
V_{DD}	32	1		CPU and Logic Digital Power Pins – no supply source needed when using internal VREG. Tie with 1.2 µF ceramic capacitor to ground when using internal VREG.
V_{DD}	43	11		
V_{DDIO}	35	4		Digital I/O and Flash Power Pin – Single Supply source when VREG is enabled
V_{SS}	33	2		Digital Ground Pins
V_{SS}	44	12		
VOLTAGE REGULATOR CONTROL SIGNAL				
$\overline{\text{VREGENZ}}$	34	3	I	Internal VREG Enable/Disable – pull low to enable VREG, pull high to disable VREG
GPIO AND PERIPHERAL SIGNALS				
GPIO0	29	37	I/O/Z	General purpose input/output 0

Table 2-2. TERMINAL FUNCTIONS (continued)

TERMINAL			I/O/Z	DESCRIPTION
NAME	PT NO.	DA NO.		
EPWM1A			O	Enhanced PWM1 Output A and HRPWM channel
–			–	–
–			–	–
GPIO1	28	36	I/O/Z	General purpose input/output 1
EPWM1B			O	Enhanced PWM1 Output B
–			–	
COMP1OUT			O	Direct output of Comparator 1
GPIO2	37	5	I/O/Z	General purpose input/output 2
EPWM2A			O	Enhanced PWM2 Output A and HRPWM channel
–				–
–				–
GPIO3	38	6	I/O/Z	General purpose input/output 3
EPWM2B			O	Enhanced PWM2 Output B
–				–
COMP2OUT			O	Direct output of Comparator 2
GPIO4	39	7	I/O/Z	General purpose input/output 4
EPWM3A			O	Enhanced PWM3 output A and HRPWM channel
–				–
–				–
GPIO5	40	8	I/O/Z	General purpose input/output 5
EPWM3B			O	Enhanced PWM3 output B
–				–
ECAP1			I/O	Enhanced Capture input/output 1
GPIO6	41	9	I/O/Z	General purpose input/output 6
EPWM4A			O	Enhanced PWM4 output A and HRPWM channel
EPWMSYNCI			I	External ePWM sync pulse input
EPWMSYNCO			O	External ePWM sync pulse output
GPIO7	42	10	I/O/Z	General purpose input/output 7
EPWM4B			O	Enhanced PWM4 output B
SCIRXDA			I	SCI-A receive data
–				–
GPIO12	47	13	I/O/Z	General purpose input/output 12
$\overline{TZ1}$			I	Trip Zone input 1
SCITXDA			O	SCI-A transmit data
–				–
GPIO16	27	35	I/O/Z	General purpose input/output 16
SPISIMOA			I/O	SPI slave in, master out
–				–
$\overline{TZ2}$			I	Trip Zone input 2
GPIO17	26	34	I/O/Z	General purpose input/output 17
SPISOMIA			I/O	SPI-A slave out, master in
–				–
$\overline{TZ3}$			I	Trip zone input 3
GPIO18	24	32	I/O/Z	General purpose input/output 18
SPICLKA			I/O	SPI-A clock input/output
SCITXDA			O	SCI-A transmit

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Table 2-2. TERMINAL FUNCTIONS (continued)

TERMINAL			I/O/Z	DESCRIPTION
NAME	PT NO.	DA NO.		
XCLKOUT			O/Z	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
GPIO19	25	33	I/O/Z	General purpose input/output 19
XCLKIN				External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken not to enable this path for clocking if it is being used for the other periperhal functions
$\overline{\text{SPISTEA}}$			I/O	SPI-A slave transmit enable input/output
SCIRXDA			I	SCI-A receive
ECAP1			I/O	Enhanced Capture input/output 1
GPIO28	48	14	I/O/Z	General purpose input/output 28
SCIRXDA			I	SCI receive data
SDAA			I/OC	I2C data open-drain bidirectional port
$\overline{\text{TZ2}}$			I	Trip zone input 2
GPIO29	1	15	I/O/Z	General purpose input/output 29.
SCITXDA			O	SCI transmit data
SCLA			I/OC	I2C clock open-drain bidirectional port
$\overline{\text{TZ3}}$			I	Trip zone input 3
GPIO32	31	-	I/O/Z	General purpose input/output 32
SDAA			I/OC	I2C data open-drain bidirectional port
EPWMSYNCI			I	Enhanced PWM external sync pulse input
$\overline{\text{ADCSOCAO}}$			O	ADC start-of-conversion A
GPIO33	36	–	I/O/Z	General-Purpose Input/Output 33
SCLA			I/OC	I2C clock open-drain bidirectional port
EPWMSYNCO			O	Enhanced PWM external synch pulse output
$\overline{\text{ADCSOCBO}}$			O	ADC start-of-conversion B
GPIO34	19	27	I/O/Z	General-Purpose Input/Output 34
COMP2OUT			O	Direct output of Comparator 2
–				–
–				–
GPIO35	20	28	I/O/Z	General-Purpose Input/Output 35
TDI			I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK
GPIO36	21	29	I/O/Z	General-Purpose Input/Output 36
TMS			I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
GPIO37	22	30	I/O/Z	General-Purpose Input/Output 37
TDO			O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK (8 mA drive)
GPIO38	23	31	I/O/Z	General-Purpose Input/Output 38
TCK			I	JTAG test clock with internal pullup
XCLKIN			I	External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken to not enable this path for clocking if it is being used for the other periperhal functions.

3 Functional Overview

3.1 Block Diagram

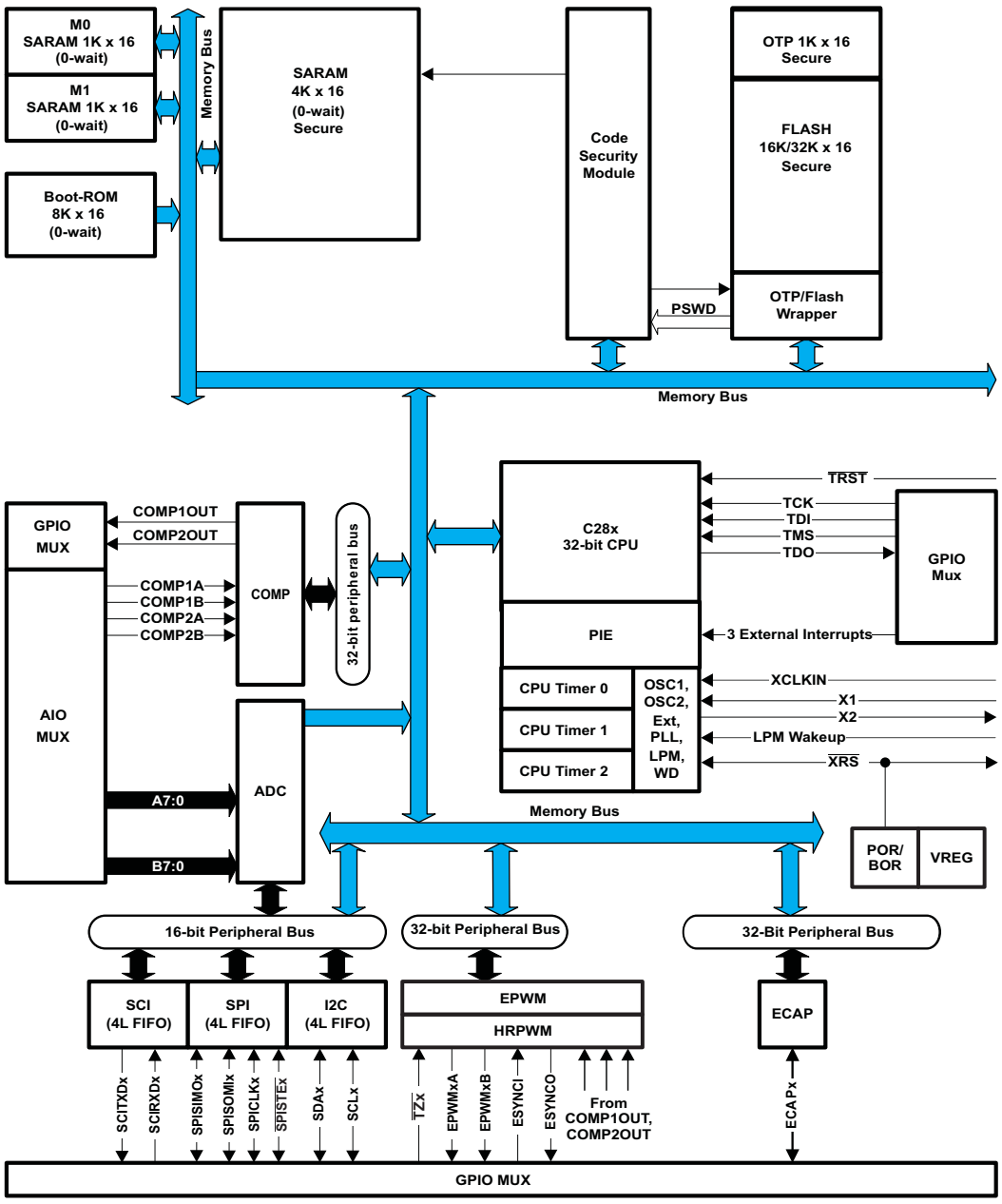

Figure 3-1. Functional Block Diagram

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3.2 Memory Maps

In Figure 3-2, the following apply:

- Memory blocks are not to scale.
- Peripheral Frame 0, Peripheral Frame 1 and Peripheral Frame 2 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.
- *Protected* means the order of Write-followed-by-Read operations is preserved rather than the pipeline order.
- Certain memory ranges are EALLOW protected against spurious writes after configuration.
- Locations 0x3D7C80 – 0x3D7CC0 contain the internal oscillator and ADC calibration routines. These locations are not programmable by the user.

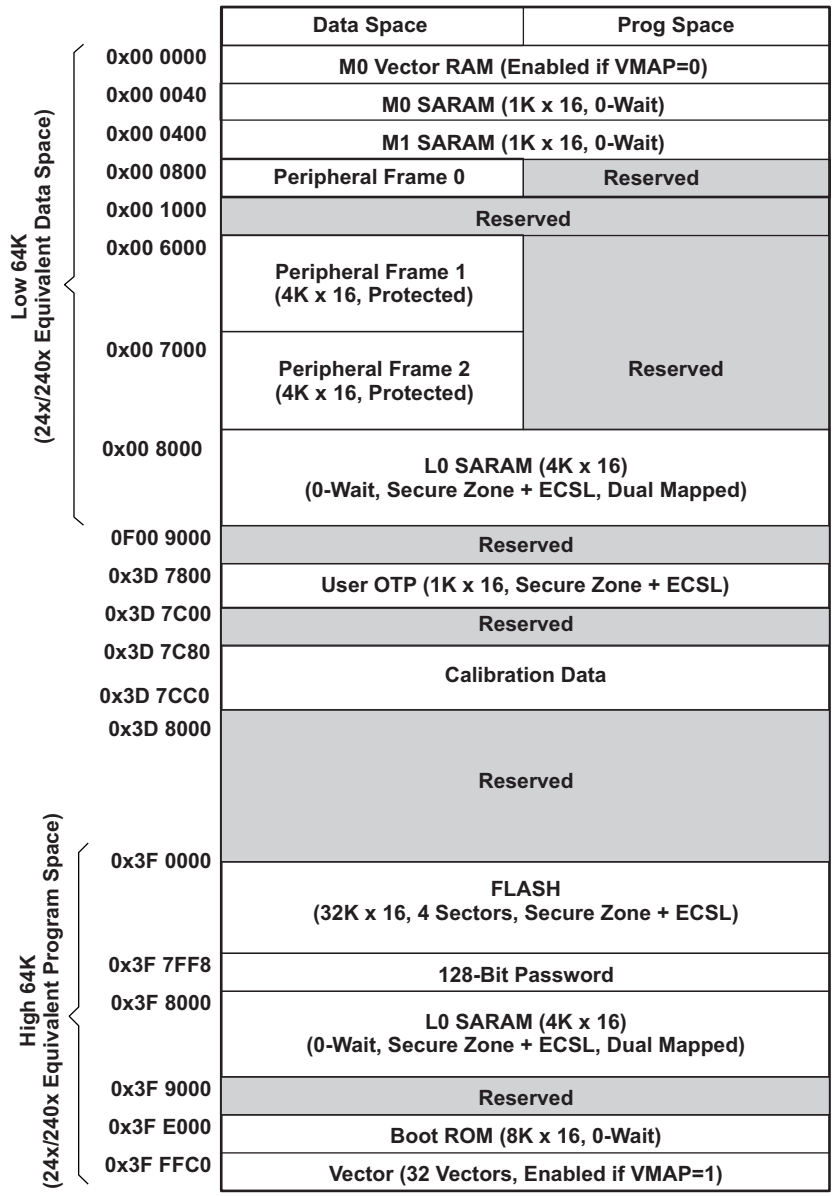

Figure 3-2. 28023/28025/28027 Memory Map

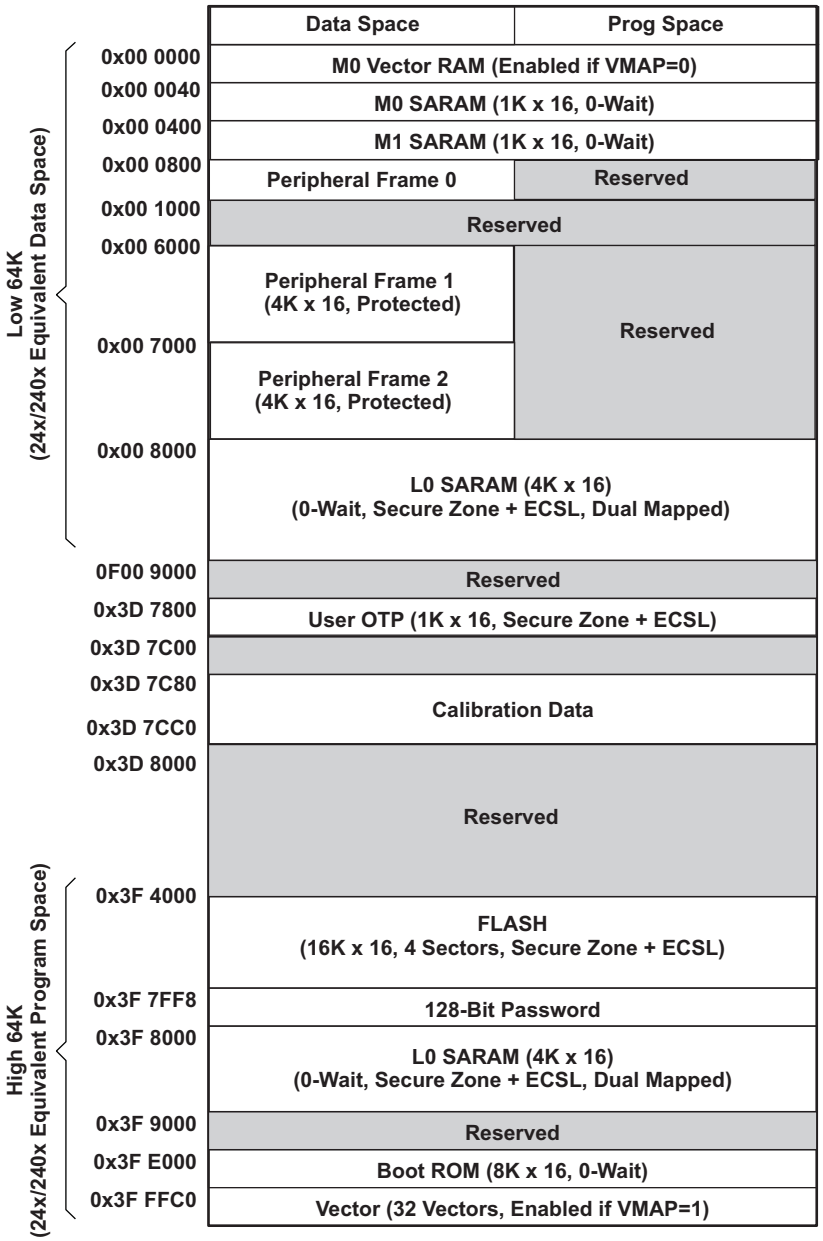

Figure 3-3. 28022/28024/28026 Memory Map

Table 3-1. Addresses of Flash Sectors in F28023/28025/28027

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 0000 - 0x3F 1FFF	Sector D (8K x 16)
0x3F 2000 - 0x3F 3FFF	Sector C (8K x 16)
0x3F 4000 - 0x3F 5FFF	Sector B (8K x 16)
0x3F 6000 - 0x3F 7F7F	Sector A (8K x 16)
0x3F 7F80 - 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 - 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 - 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 3-2. Addresses of Flash Sectors in F28022/28024/28026

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3F 4000 - 0x3F 4FFF	Sector D (4K x 16)
0x3F 5000 - 0x3F 5FFF	Sector C (4K x 16)
0x3F 6000 - 0x3F 6FFF	Sector B (4K x 16)
0x3F 7000 - 0x3F 7F7F	Sector A (4K x 16)
0x3F 7F80 - 0x3F 7FF5	Program to 0x0000 when using the Code Security Module
0x3F 7FF6 - 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 - 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

NOTE

- When the code-security passwords are programmed, all addresses between 0x3F 7F80 and 0x3F 7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F 7F80 through 0x3F 7FEF may be used for code or data. Addresses 0x3F 7FF0 – 0x3F 7FF5 are reserved for data and should not contain program code.

Table 3-3 shows how to handle these memory locations.

Table 3-3. Impact of Using the Code Security Module

ADDRESS	FLASH	
	Code security enabled	Code security disabled
0x3F 7F80 - 0x3F 7FEF	Fill with 0x0000	Application code and data
0x3F 7FF0 - 0x3F 7FF5		Reserved for data only

Peripheral Frame 1 and Peripheral Frame 2 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode makes sure that all accesses to these blocks happen as written. Because of the pipeline, a write immediately followed by a read to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The CPU supports a block protection mode where a region of memory can be protected so that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it protects the selected zones.

The wait-states for the various spaces in the memory map area are listed in Table 3-4.

Table 3-4. Wait-states

AREA	WAIT-STATES (CPU)	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Cycles can be extended by peripheral generated ready.
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed. Cycles cannot be extended by the peripheral.
L0 SARAM	0-wait data and program	Assumes no CPU conflicts
OTP	Programmable 1-wait minimum	Programmed via the Flash registers. 1-wait is minimum number of wait states allowed.
FLASH	Programmable 0-wait Paged min 1-wait Random min Random ≥ Paged	Programmed via the Flash registers.
FLASH Password	16-wait fixed	Wait states of password locations are fixed.
Boot-ROM	0-wait	

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3.3 Brief Descriptions

3.3.1 CPU

The 2802x (C28x) family is a member of the TMS320C2000™ microcontroller (MCU) platform. The C28x-based controllers have the same 32-bit fixed-point architecture as existing C28x MCUs. It is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enabling development of math algorithms using C/C++. The device is as efficient at MCU math tasks as it is at system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 x 32-bit MAC 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables it to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

3.3.2 Memory Bus (Harvard Bus Architecture)

As with many MCU-type devices, multiple busses are used to move data between the memories and peripherals and the CPU. The memory bus architecture contains a program read bus, data read bus, and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write busses consist of 32 address lines and 32 data lines each. The 32-bit-wide data busses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

3.3.3 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) MCU family of devices, the devices adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various busses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Three versions of the peripheral bus are supported. One version supports only 16-bit accesses (called peripheral frame 2). Another version supports both 16- and 32-bit accesses (called peripheral frame 1).

3.3.4 Real-Time JTAG and Analysis

The devices implement the standard IEEE 1149.1 JTAG(1) interface for in-circuit based debug. Additionally, the devices support real-time mode of operation allowing modification of the contents of memory, peripheral, and register locations while the processor is running and executing code and servicing interrupts. The user can also single step through non-time-critical code while enabling time-critical interrupts to be serviced without interference. The device implements the real-time mode in

(1) IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture

hardware within the CPU. This is a feature unique to the 28x family of devices, requiring no software monitor. Additionally, special analysis hardware is provided that allows setting of hardware breakpoint or data/address watch-points and generating various user-selectable break events when a match occurs. These devices do not support boundary scan; however, IDCODE and BYPASS features are available if the following considerations are taken into account. The IDCODE does not come by default. The user needs to go through a sequence of SHIFT IR and SHIFT DR state of JTAG to get the IDCODE. For BYPASS instruction, the first shifted DR value would be 1.

3.3.5 Flash

The F28027/25/23 devices contain 32K x 16 of embedded flash memory, segregated into four 8K x 16 sectors. The F28026/24/22 devices contain 16K x 16 of embedded flash memory, segregated into four 4K x 16 sectors. All devices also contain a single 1K x 16 of OTP memory at address range 0x3D 7800 – 0x3D 7BFF. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase/program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Addresses 0x3F 7FF0 – 0x3F 7FF5 are reserved for data variables and should not contain program code.

NOTE

The Flash and OTP wait-states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait-states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait-state, and OTP wait-state registers, see the *TMS320x2802x System Control and Interrupts Reference Guide* (literature number SPRUFN3).

3.3.6 M0, M1 SARAMs

All devices contain these two blocks of single access memory, each 1K x 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

3.3.7 L0 SARAM

The device contains 4K x 16 of single-access memory. This block is mapped to both program and data space.

3.3.8 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms.

Table 3-5. Boot Mode Selection

MODE	GPIO37/TDO	GPIO34/CMP2OUT	$\overline{\text{TRST}}$	MODE
3	1	1	0	GetMode
2	1	0	0	Wait (see Section 3.3.9 for description)
1	0	1	0	SCI
0	0	0	0	Parallel IO
EMU	x	x	1	Emulation Boot

3.3.8.1 Emulation Boot

When the emulator is connected, the GPIO37/TDO pin cannot be used for boot mode selection. In this case, the boot ROM detects that an emulator is connected and uses the contents of two reserved SARAM locations in the PIE vector table to determine the boot mode. If the content of either location is invalid, then the *Wait* boot option is used. All boot mode options can be accessed in emulation boot.

3.3.8.2 GetMode

The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. One of the following loaders can be specified: SCI, SPI, I2C, or OTP. If the content of either OTP location is invalid, then boot to flash is used

3.3.9 Security

The devices support high levels of security to protect the user firmware from being reverse engineered. The security features a 128-bit password (hardcoded for 16 wait-states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents via the JTAG port, executing code from external memory or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit KEY value that matches the value stored in the password locations within the Flash.

In addition to the CSM, the emulation code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to flash, user OTP, or L0 memory while the emulator is connected will trip the ECSL and break the emulation connection. To allow emulation of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct value into the lower 64 bits of the KEY register, which matches the value stored in the lower 64 bits of the password locations within the flash. Note that dummy reads of all 128 bits of the password in the flash must still be performed. If the lower 64 bits of the password locations are all ones (unprogrammed), then the KEY value does not need to match.

When initially debugging a device with the password locations in flash programmed (i.e., secured), the CPU will start running and may execute an instruction that performs an access to a protected ECSL area. If this happens, the ECSL will trip and cause the emulator connection to be cut.

The solution is to use the *Wait* boot option. This will sit in a loop around a software breakpoint to allow an emulator to be connected without tripping security. The user can then exit this mode once the emulator is connected by using one of the emulation boot options as described in the *TMS320x2802x Boot ROM Reference Guide* (SPRUFN6). Piccolo devices do not support a hardware wait-in-reset mode.

NOTE

- When the code-security passwords are programmed, all addresses between 0x3F7F80 and 0x3F7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If the code security feature is not used, addresses 0x3F7F80 through 0x3F7FEF may be used for code or data. Addresses 0x3F7FF0 – 0x3F7FF5 are reserved for data and should not contain program code.

The 128-bit password (at 0x3F 7FF8 – 0x3F 7FFF) must not be programmed to zeros. Doing so would permanently lock the device.

Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

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3.3.10 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F2802x, 33 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. It takes 8 CPU clock cycles to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled/disabled within the PIE block.

3.3.11 External Interrupts (XINT1-XINT3)

The devices support three masked external interrupts (XINT1-XINT3). Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled/disabled. These interrupts also contain a 16-bit free running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time stamp the interrupt. There are no dedicated pins for the external interrupts. XINT1, XINT2, and XINT3 interrupts can accept inputs from GPIO0 – GPIO31 pins.

3.3.12 Internal Zero Pin Oscillators, Oscillator, and PLL

The device can be clocked by either of the two internal zero-pin oscillators, an external oscillator, or by a crystal attached to the on-chip oscillator circuit (48-pin devices only). A PLL is provided supporting up to 12 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to the Electrical Specification section for timing details. The PLL block can be set in bypass mode.

3.3.13 Watchdog

Each device contains two watchdogs: CPU-Watchdog that monitors the core and NMI-Watchdog that is a missing clock-detect circuit. The user software must regularly reset the CPU-watchdog counter within a certain time frame; otherwise, the CPU-watchdog generates a reset to the processor. The CPU-watchdog can be disabled if necessary. The NMI-Watchdog engages only in case of a clock failure and can either generate an interrupt or a device reset.

3.3.14 Peripheral Clocking

The clocks to each individual peripheral can be enabled/disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I2C) can be scaled relative to the CPU clock.

3.3.15 Low-power Modes

The devices are full static CMOS devices. Three low-power modes are provided:

IDLE:	Place CPU in low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that need to function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
STANDBY:	Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
HALT:	This mode basically shuts down the device and places it in the lowest possible power consumption mode. If the internal zero-pin oscillators are used as the clock source, the HALT mode turns them off, by default. To keep these oscillators from shutting down, the INTOSCnHALTI bits in CLKCTL register may be used. The zero-pin oscillators may thus be used to clock the CPU-watchdog in this mode. If the on-chip crystal oscillator is used as the clock source, it is shut down in this mode. A reset or an external signal (through a GPIO pin) or the CPU-watchdog can wake the device from this mode.

3.3.16 Peripheral Frames 0, 1, 2 (PFn)

The device segregates peripherals into three sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Waitstate Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result Registers
PF1:	GPIO:	GPIO MUX Configuration and Control Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers
	eCAP:	Enhanced Capture Module and Registers
	Comparators:	Comparator Modules

PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Configuration Registers
	I2C:	Inter-Integrated Circuit Module and Registers
	XINT	External Interrupt Registers

3.3.17 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

3.3.18 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value. CPU-Timer 2 is connected to INT14 of the CPU. It can be clocked by any one of the following:

- SYSCLKOUT (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTSOC2)
- External clock source

CPU-Timer 1 is for general use and can be connected to INT13 of the CPU. CPU-Timer 0 is also for general use and is connected to the PIE block.

3.3.19 Control Peripherals

The devices support the following peripherals that are used for embedded control and communication:

ePWM:	The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support the HRPWM high resolution duty and period features. The type 1 module found on 2802x devices also supports increased dead-band resolution, enhanced SOC and interrupt generation, and advanced triggering including trip functions based on comparator outputs.
eCAP:	The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes. This peripheral can also be configured to generate an auxiliary PWM signal.
ADC:	The ADC block is a 12-bit converter. It has up to 13 single-ended channels pinned out, depending on the device. It contains two sample-and-hold units for simultaneous sampling.
Comparator:	Each comparator block consists of one analog comparator along with an internal 10-bit reference for supplying one input of the comparator.

3.3.20 Serial Port Peripherals

The devices support the following serial communication peripherals:

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multi-device communications are supported by the master/slave operation of the SPI. The SPI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

SCI: The serial communications interface is a two-wire asynchronous serial port, commonly known as UART. The SCI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

I2C: The inter-integrated circuit (I2C) module provides an interface between a MCU and other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus) specification version 2.1 and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to/from the MCU through the I2C module. The I2C contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

3.4 Register Map

The devices contain four peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus. See Table 3-6.

Peripheral Frame 1 These are peripherals that are mapped to the 32-bit peripheral bus. See Table 3-7.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 3-8.

Table 3-6. Peripheral Frame 0 Registers(1)

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED(2)
Device Emulation Registers	0x00 0880 - 0x00 09FF	384	Yes
FLASH Registers(3)	0x00 0A80 - 0x00 0ADF	96	Yes
Code Security Module Registers	0x00 0AE0 - 0x00 0AEF	16	Yes
ADC registers 0 wait read only	0x00 0B00 - 0x00 0B0F	16	No
CPU–TIMER0/1/2 Registers	0x00 0C00 - 0x00 0C3F	64	No
PIE Registers	0x00 0CE0 - 0x00 0CFF	32	No
PIE Vector Table	0x00 0D00 - 0x00 0DFF	256	No

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Code Security Module (CSM).

Table 3-7. Peripheral Frame 1 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
Comparator 1 registers	0x00 6400 - 0x00 641F	32	(1)
Comparator 2 registers	0x00 6420 - 0x00 643F	32	(1)
EPWM1 + HRPWM1 registers	0x00 6800 - 0x00 683F	64	(1)
EPWM2 + HRPWM2 registers	0x00 6840 - 0x00 687F	64	(1)
EPWM3 + HRPWM3 registers	0x00 6880 - 0x00 68BF	64	(1)
EPWM4 + HRPWM4 registers	0x00 68C0 - 0x00 68FF	64	(1)
ECAP1 registers	0x00 6A00 - 0x00 6A1F	32	No
GPIO registers	0x00 6F80 - 0x00 6FFF	128	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 3-8. Peripheral Frame 2 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
System Control Registers	0x00 7010 - 0x00 702F	32	Yes
SPI-A Registers	0x00 7040 - 0x00 704F	16	No
SCI-A Registers	0x00 7050 - 0x00 705F	16	No
NMI Watchdog Interrupt Registers	0x00 7060 - 0x00 706F	16	Yes
External Interrupt Registers	0x00 7070 - 0x00 707F	16	Yes
ADC Registers	0x00 7100 - 0x00 717F	32	(1)
I2C-A Registers	0x00 7900 - 0x00 793F	64	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

3.5 Device Emulation Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 3-9.

Table 3-9. Device Emulation Registers

NAME	ADDRESS RANGE	SIZE (x16)	DESCRIPTION			EALLOW PROTECTED
DEVICECNF	0x0880 0x0881	2	Device Configuration Register			Yes
CLASSID	0x0882	1	Class ID Register	TMS320F28027 TMS320F28026 TMS320F28025 TMS320F28024 TMS320F28023 TMS320F28022	0x00CF 0x00C7 0x00CF 0x00C7 0x00CF 0x00C7	No
REVID	0x0883	1	Revision ID Register	0x0000 - Silicon Rev. 0 - TMX		No

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3.6 Interrupts

Figure 3-4 shows how the various interrupt sources are multiplexed.

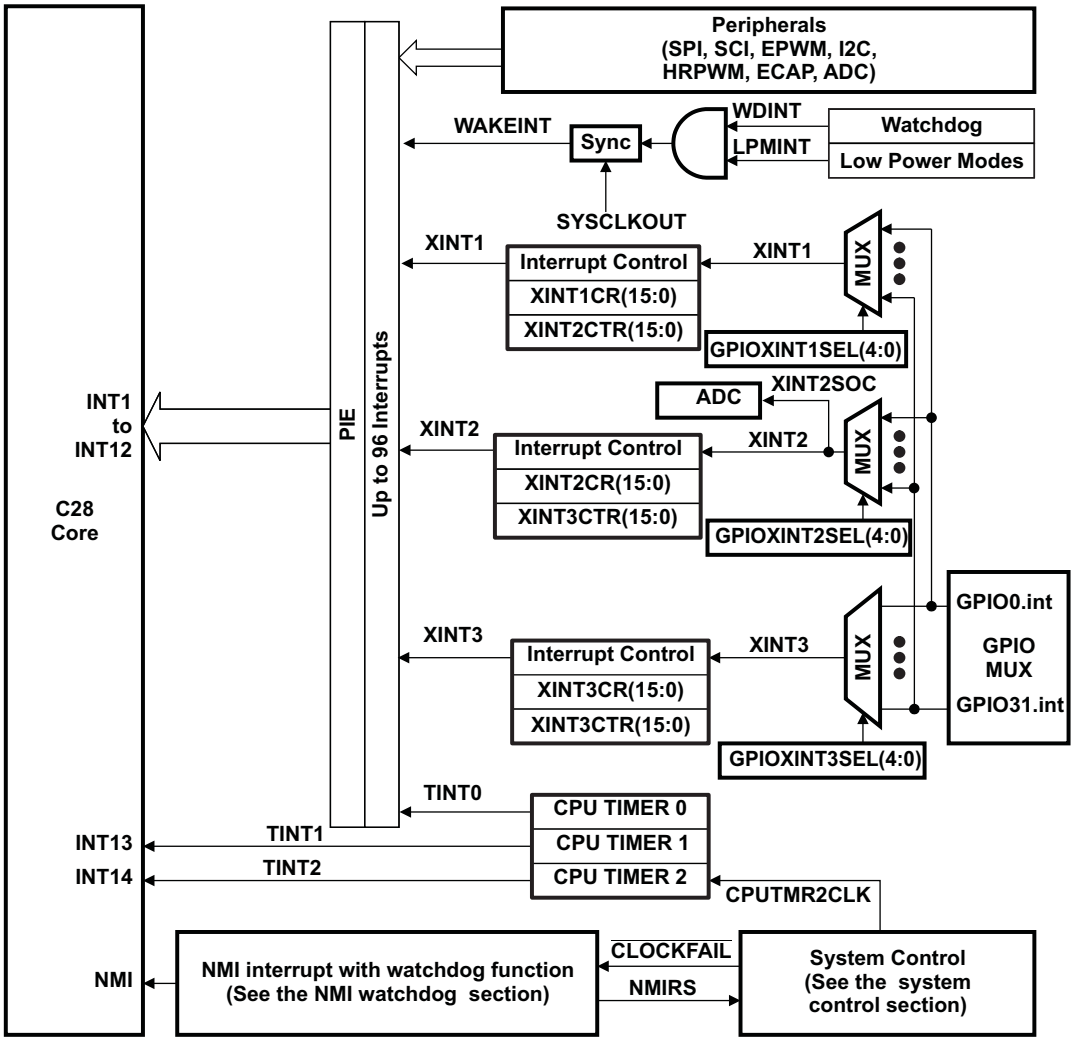

Figure 3-4. External and PIE Interrupt Sources

Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. Table 3-10 shows the interrupts used by 2802x devices.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine corresponding to the vector specified. TRAP #0 attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, TRAP #0 should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, TRAP #1 through TRAP #12 will transfer program control to the interrupt service routine corresponding to the first vector within the PIE group. For example: TRAP #1 fetches the vector from INT1.1, TRAP #2 fetches the vector from INT2.1, and so forth.

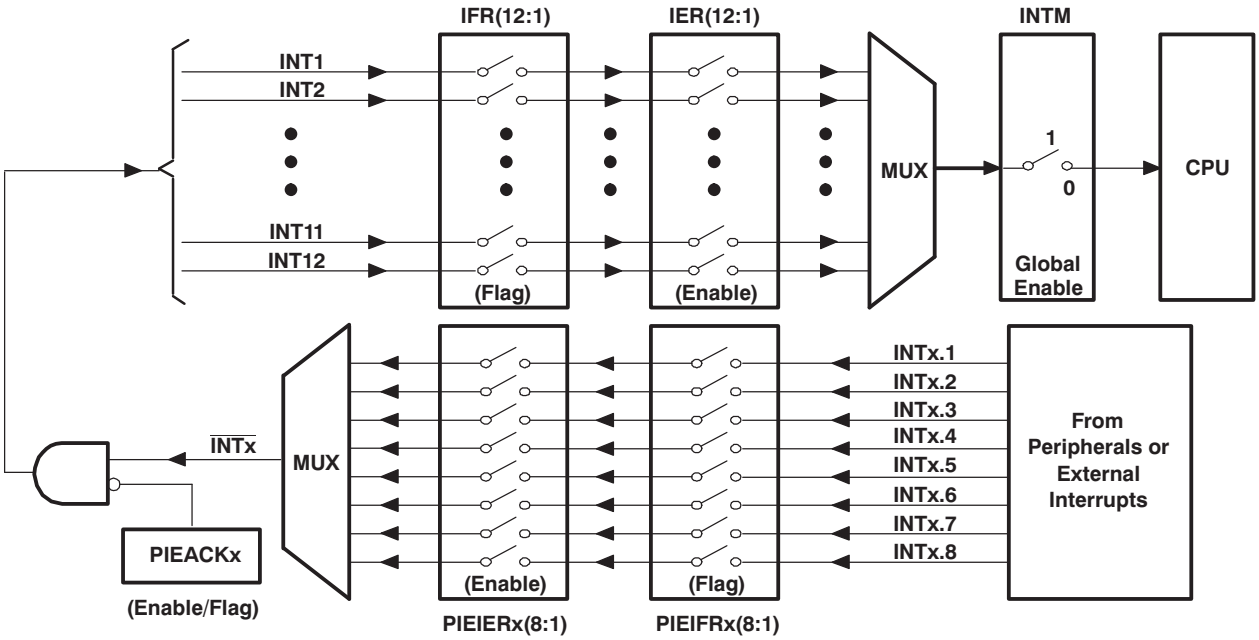

Figure 3-5. Multiplexing of Interrupts Using the PIE Block

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Table 3-10. PIE MUXed Peripheral Interrupt Vector Table

	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1.y	WAKEINT (LPM/WD) 0xD4E	TINT0 (TIMER 0) 0xD4C	ADCINT9 (ADC) 0xD4A	XINT2 Ext. int. 2 0xD48	XINT1 Ext. int. 1 0xD46	Reserved – 0xD44	ADCINT2 (ADC) 0xD42	ADCINT1 (ADC) 0xD40
INT2.y	Reserved – 0xD5E	Reserved – 0xD5C	Reserved – 0xD5A	Reserved – 0xD58	EPWM4_TZINT (ePWM4) 0xD56	EPWM3_TZINT (ePWM3) 0xD54	EPWM2_TZINT (ePWM2) 0xD52	EPWM1_TZINT (ePWM1) 0xD50
INT3.y	Reserved – 0xD6E	Reserved – 0xD6C	Reserved – 0xD6A	Reserved – 0xD68	EPWM4_INT (ePWM4) 0xD66	EPWM3_INT (ePWM3) 0xD64	EPWM2_INT (ePWM2) 0xD62	EPWM1_INT (ePWM1) 0xD60
INT4.y	Reserved – 0xD7E	Reserved – 0xD7C	Reserved – 0xD7A	Reserved – 0xD78	Reserved – 0xD76	Reserved – 0xD74	Reserved – 0xD72	ECAP1_INT (eCAP1) 0xD70
INT5.y	Reserved – 0xD8E	Reserved – 0xD8C	Reserved – 0xD8A	Reserved – 0xD88	Reserved – 0xD86	Reserved – 0xD84	Reserved – 0xD82	Reserved – 0xD80
INT6.y	Reserved – 0xD9E	Reserved – 0xD9C	Reserved – 0xD9A	Reserved – 0xD98	Reserved – 0xD96	Reserved – 0xD94	SPITXINTA (SPI-A) 0xD92	SPIRXINTA (SPI-A) 0xD90
INT7.y	Reserved – 0xDAE	Reserved – 0xDAC	Reserved – 0xDAA	Reserved – 0xDA8	Reserved – 0xDA6	Reserved – 0xDA4	Reserved – 0xDA2	Reserved – 0xDA0
INT8.y	Reserved – 0xDBE	Reserved – 0xDBC	Reserved – 0xDBA	Reserved – 0xDB8	Reserved – 0xDB6	Reserved – 0xDB4	I2CINT2A (I2C-A) 0xDB2	I2CINT1A (I2C-A) 0xDB0
INT9.y	Reserved – 0xDCE	Reserved – 0xDCC	Reserved – 0xDCA	Reserved – 0xDC8	Reserved – 0xDC6	Reserved – 0xDC4	SCITXINTA (SCI-A) 0xDC2	SCIRXINTA (SCI-A) 0xDC0
INT10.y	ADCINT8 (ADC) 0xDDE	ADCINT7 (ADC) 0xDDC	ADCINT6 (ADC) 0xDDA	ADCINT5 (ADC) 0xDD8	ADCINT4 (ADC) 0xDD6	ADCINT3 (ADC) 0xDD4	ADCINT2 (ADC) 0xDD2	ADCINT1 (ADC) 0xDD0
INT11.y	Reserved – 0xDEE	Reserved – 0xDEC	Reserved – 0xDEA	Reserved – 0xDE8	Reserved – 0xDE6	Reserved – 0xDE4	Reserved – 0xDE2	Reserved – 0xDE0
INT12.y	Reserved – 0xDFE	Reserved – 0xDFC	Reserved – 0xDFA	Reserved – 0xDF8	Reserved – 0xDF6	Reserved – 0xDF4	Reserved – 0xDF2	XINT3 Ext. Int. 3 0xDF0

Table 3-11. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

3.6.1 External Interrupts

Table 3-12. External Interrupt Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
XINT1CR	0x00 7070	1	XINT1 configuration register
XINT2CR	0x00 7071	1	XINT2 configuration register
XINT3CR	0x00 7072	1	XINT3 configuration register
XINT1CTR	0x00 7078	1	XINT1 counter register
XINT2CTR	0x00 7079	1	XINT2 counter register
XINT3CTR	0x00 707A	1	XINT3 counter register

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Each external interrupt can be enabled/disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the *TMS320x2802x System and Interrupts Reference Guide* (literature number SPRUFN3).

3.7 VREG/BOR/POR

Although the core and I/O circuitry operate on two different voltages, these devices have an on-chip voltage regulator (VREG) to generate the V_{DD} voltage from the V_{DDIO} supply. This eliminates the cost and space of a second external regulator on an application board. Additionally, internal power-on reset (POR) and brown-out reset (BOR) circuits monitor both the V_{DD} and V_{DDIO} rails during power-up and run mode, eliminating a need for any external voltage supervisory circuits.

3.7.1 On-chip Voltage Regulator (VREG)

A linear regulator generates the core voltage (V_{DD}) from the V_{DDIO} supply. Therefore, although capacitors are required on each V_{DD} pin to stabilize the generated voltage, power need not be supplied to these pins to operate the device. Conversely, the VREG can be disabled, should power or redundancy be the primary concern of the application.

3.7.1.1 Using the On-chip VREG

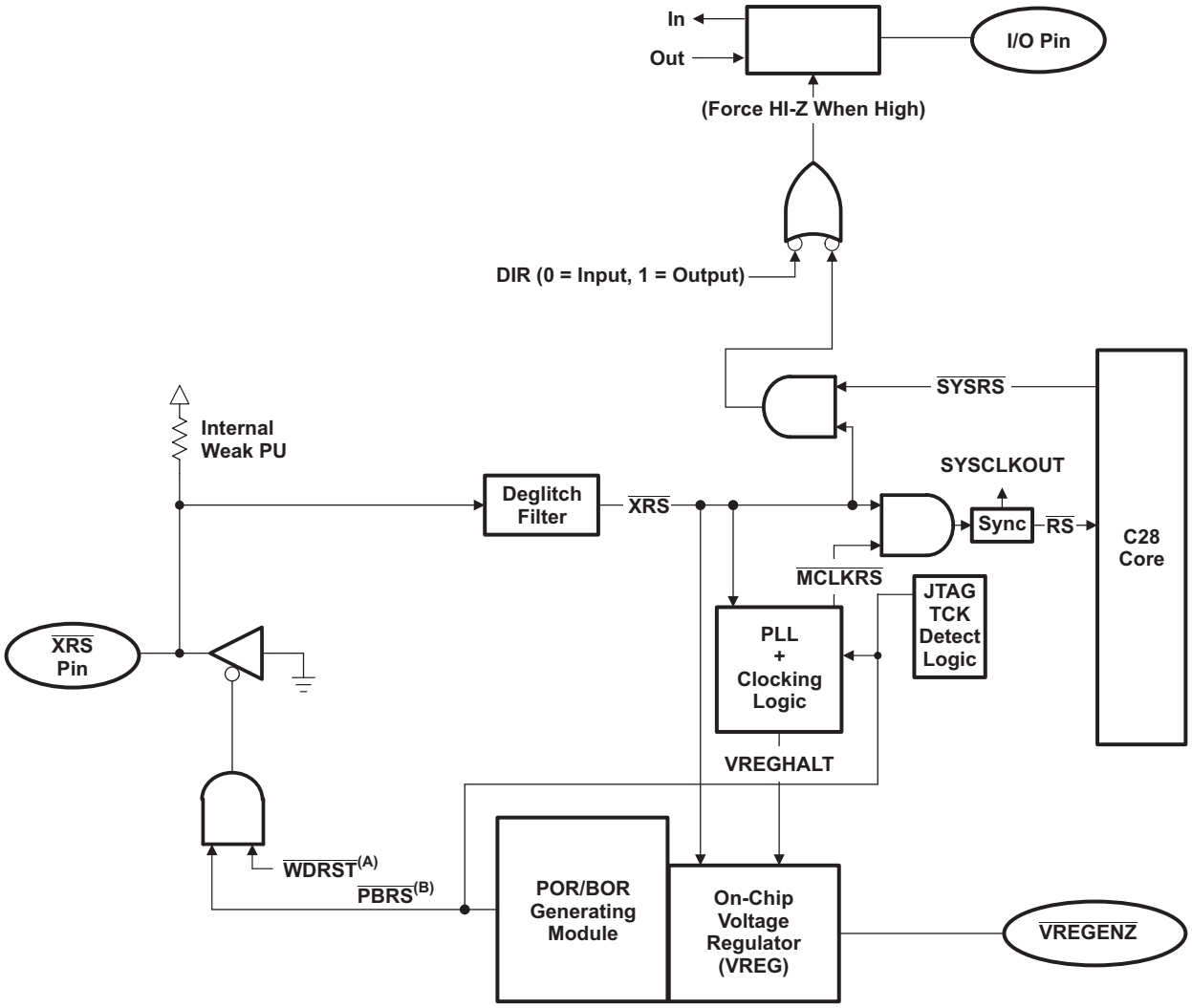
To utilize the on-chip VREG, the $\overline{\text{VREGENZ}}$ pin should be pulled low and the appropriate recommended operating voltage should be supplied to the V_{DDIO} and V_{DDA} pins. In this case, the V_{DD} voltage needed by the core logic will be generated by the VREG. Each V_{DD} pin requires on the order of 1.2 µF capacitance for proper regulation of the VREG. These capacitors should be located as close as possible to the V_{DD} pins.

3.7.1.2 Disabling the On-chip VREG

To conserve power, it is also possible to disable the on-chip VREG and supply the core logic voltage to the V_{DD} pins with a more efficient external regulator. To enable this option, the $\overline{\text{VREGENZ}}$ pin must be pulled high.

3.7.2 On-chip Power-On Reset (POR) and Brown-Out Reset (BOR) Circuit

Two on-chip supervisory circuits, the power-on reset (POR) and the brown-out reset (BOR) remove the burden of monitoring the V_{DD} and V_{DDIO} supply rails from the application board. The purpose of the POR is to create a clean reset throughout the device during the entire power-up procedure. The trip point is a looser, lower trip point than the BOR, which watches for dips in the V_{DD} or V_{DDIO} rail during device operation. The POR function is present on both V_{DD} and V_{DDIO} rails at all times. After initial device power-up, the BOR function is present on V_{DDIO} at all times, and on V_{DD} when the internal VREG is enabled ($\overline{\text{VREGENZ}}$ pin is pulled low). Both functions pull the $\overline{\text{XRS}}$ pin low when one of the voltages is below their respective trip point. See the Section 6 for the various trip points as well as the delay time from the voltage rising past the trip point and the release of the $\overline{\text{XRS}}$ pin. Figure 3-6 shows the VREG, POR, and BOR.



A. $\overline{\text{WDRST}}$ is the reset signal from the CPU-watchdog.

B. $\overline{\text{PBRS}}$ is the reset signal from the POR/BOR module.

Figure 3-6. VREG + POR + BOR + Reset Signal Connectivity

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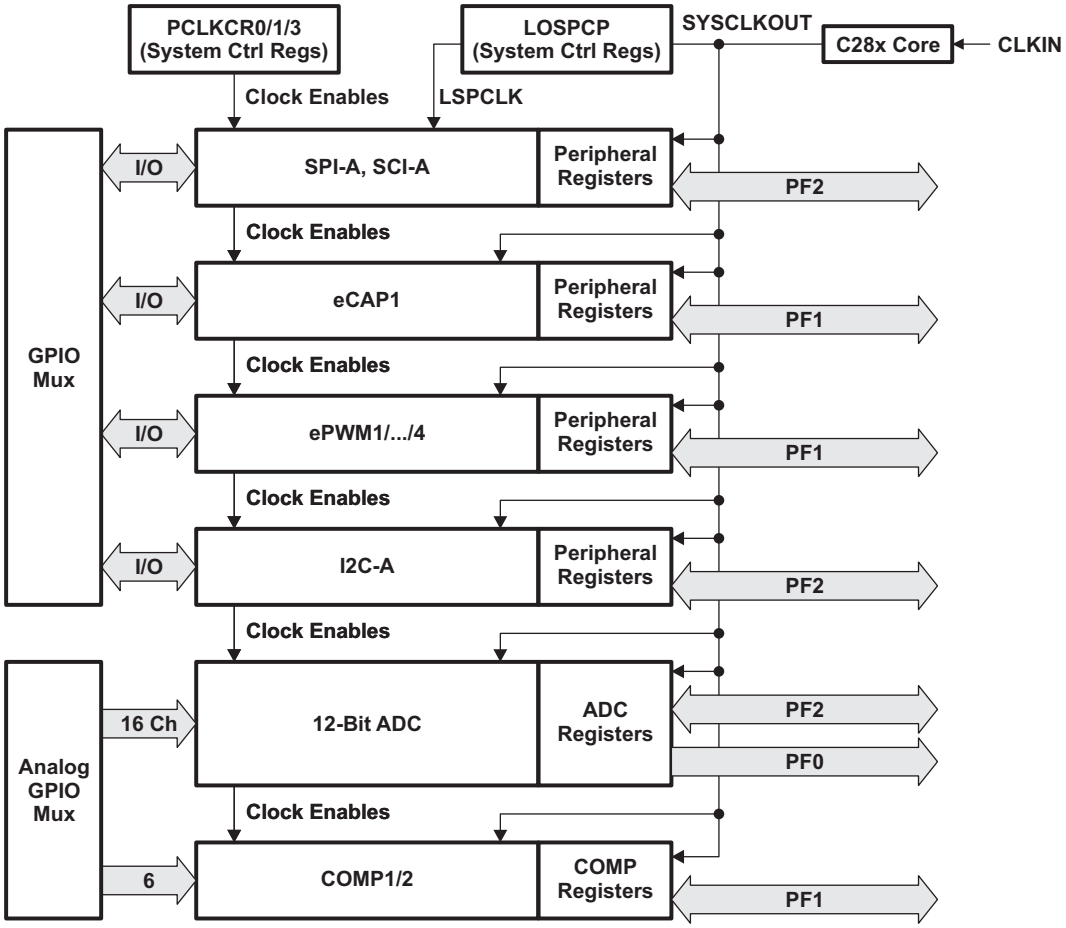
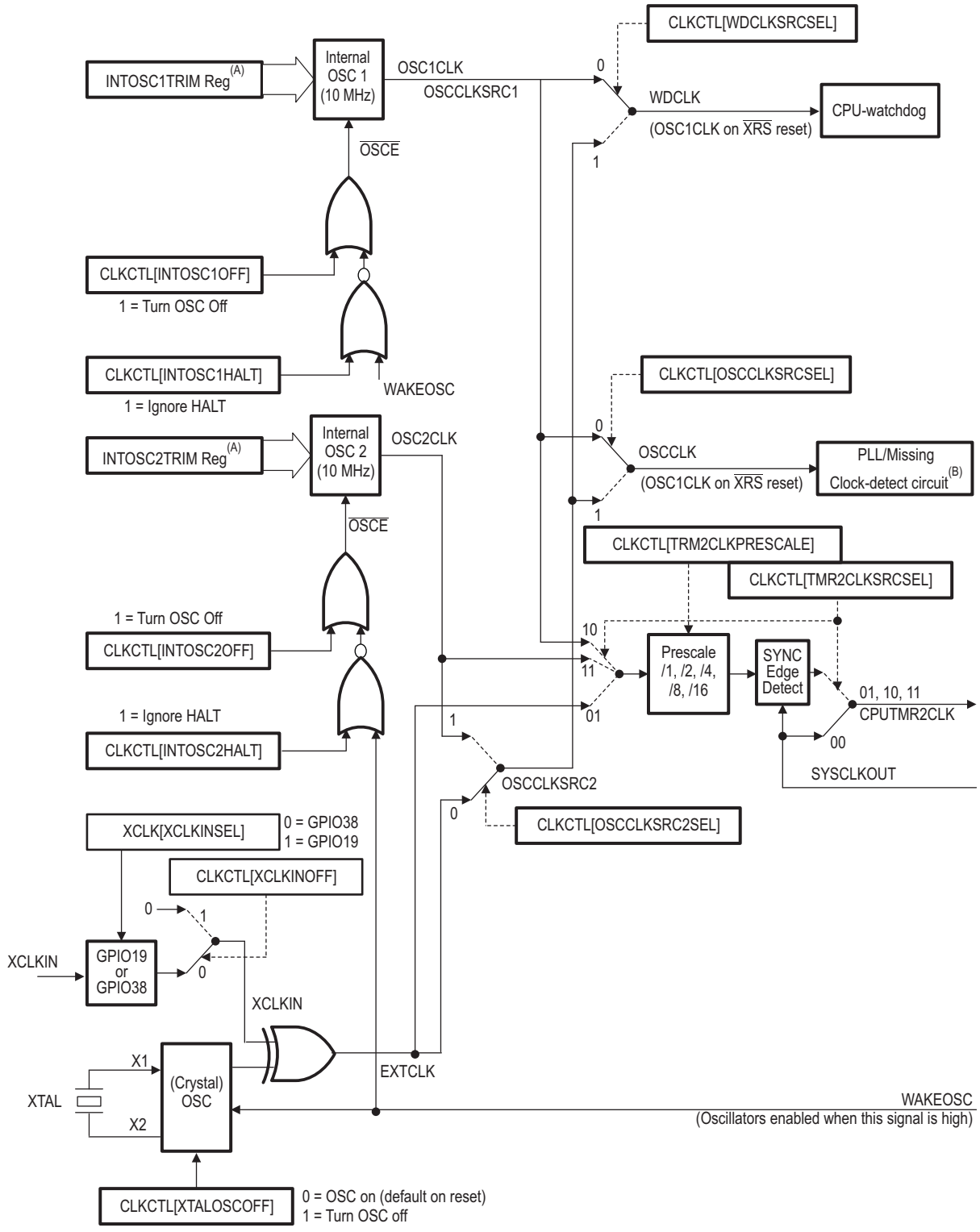
3.8 System Control

This section describes the oscillator and clocking mechanisms, the watchdog function and the low power modes. Figure 3-7 shows the various clock domains that are discussed. Figure 3-8 shows the various clock sources (both internal and external) that can provide a clock for device operation.



A. CLKIN is the clock into the CPU. It is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 3-7. Clock and Reset Domains



A. Register loaded from TI OTP-based calibration function.

B. See Section 3.8.4 for details on missing clock detection.

Figure 3-8. Clock Tree

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3.8.1 Internal Zero Pin Oscillators

The F2802x devices contain two independent internal zero pin oscillators. By default both oscillators are turned on at power up, and internal oscillator 1 is the default clock source at this time. For power savings, unused oscillators may be powered down by the user. The center frequency of these oscillators is determined by their respective oscillator trim registers, written to in the calibration routine as part of the boot ROM execution. See the electrical section for more information on these oscillators.

3.8.2 External Reference Oscillator Clock Option

The typical specifications for the external quartz crystal for a frequency of 10 MHz are listed below:

- Fundamental mode, parallel resonant
- C_L (load capacitance) = 12 pF
- $C_{L1} = C_{L2}$ = 24 pF
- C_{shunt} = 6 pF
- ESR range = 30 to 60 Ω

TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the MCU chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start up and stability over the entire operating range.

Table 3-13. PLL, Clocking, Watchdog, and Low-Power Mode Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION(1)
XCLK	0x00 7010	1	XCLKOUT Control
PLLSTS	0x00 7011	1	PLL Status Register
CLKCTL	0x00 7012	1	Clock Control Register
PLLLOCKPRD	0x00 7013	1	PLL Lock Period
INTOSC1TRIM	0x00 7014	1	Internal Oscillator 1 Trim Register
INTOSC2TRIM	0x00 7016	1	Internal Oscillator 2 Trim Register
LOSPCP	0x00 701B	1	Low-Speed Peripheral Clock Prescaler Register
PCLKCR0	0x00 701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x00 701D	1	Peripheral Clock Control Register 1
LPMCR0	0x00 701E	1	Low Power Mode Control Register 0
PCLKCR3	0x00 7020	1	Peripheral Clock Control Register 3
PLLCR	0x00 7021	1	PLL Control Register
SCSR	0x00 7022	1	System Control and Status Register
WDCNTR	0x00 7023	1	Watchdog Counter Register
WDKEY	0x00 7025	1	Watchdog Reset Key Register
WDCR	0x00 7029	1	Watchdog Control Register

(1) All registers in this table are EALLOW protected.

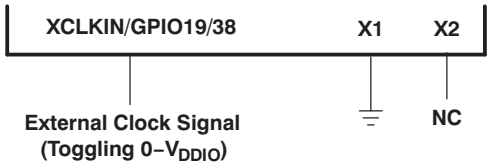
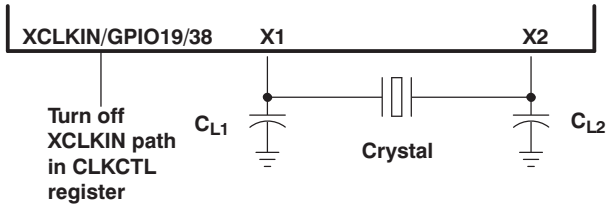


Figure 3-9. Using a 3.3-V External Oscillator



A. X1/X2 pins are available in 48-pin package only.

Figure 3-10. Using the On-chip Crystal Oscillator

3.8.3 PLL-Based Clock Module

The devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 4-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. It can be re-enabled (if need be) after the PLL module has stabilized, which takes 1 ms. The input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) is at least 50 MHz.

Table 3-14. PLL Settings

PLLCR[DIV] VALUE(1) (2)	SYSCLKOUT (CLKIN)		
	PLLSTS[DIVSEL] = 0 or 1(3)	PLLSTS[DIVSEL] = 2	PLLSTS[DIVSEL] = 3
0000 (PLL bypass)	OSCCLK/4 (Default)(1)	OSCCLK/2	OSCCLK
0001	(OSCCLK * 1)/4	(OSCCLK * 1)/2	–
0010	(OSCCLK * 2)/4	(OSCCLK * 2)/2	–
0011	(OSCCLK * 3)/4	(OSCCLK * 3)/2	–
0100	(OSCCLK * 4)/4	(OSCCLK * 4)/2	–
0101	(OSCCLK * 5)/4	(OSCCLK * 5)/2	–
0110	(OSCCLK * 6)/4	(OSCCLK * 6)/2	–
0111	(OSCCLK * 7)/4	(OSCCLK * 7)/2	–
1000	(OSCCLK * 8)/4	(OSCCLK * 8)/2	–
1001	(OSCCLK * 9)/4	(OSCCLK * 9)/2	–
1010	(OSCCLK * 10)/4	(OSCCLK * 10)/2	–
1011	(OSCCLK * 11)/4	(OSCCLK * 11)/2	–
1100	(OSCCLK * 12)/4	(OSCCLK * 12)/2	–

(1) The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to their default state by the $\overline{\text{XRS}}$ signal or a watchdog reset only. A reset issued by the debugger or the missing clock detect logic has no effect.
(2) This register is EALLOW protected. See the *TMS320x2802x System and Interrupts Reference Guide* (literature number SPRUFN3) for more information.
(3) By default, PLLSTS[DIVSEL] is configured for /4. (The boot ROM changes this to /1.) PLLSTS[DIVSEL] must be 0 before writing to the PLLCR and should be changed only after PLLSTS[PLLLOCKS] = 1.

Table 3-15. CLKIN Divide Options

PLLSTS [DIVSEL]	CLKIN DIVIDE
0	/4
1	/4
2	/2
3	/1(1)

(1) This mode can be used only when the PLL is bypassed or off.

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The PLL-based clock module provides four modes of operation:

- I**NTOSC1 (Internal zero-pin Oscillator 1):** This is the on-chip internal oscillator 1. This can provide the clock for the Watchdog block, core and CPU-Timer 2
- **INTOSC2 (Internal zero-pin Oscillator 2):** This is the on-chip internal oscillator 2. This can provide the clock for the Watchdog block, core and CPU-Timer 2. Both INTOSC1 and INTOSC2 can be independently chosen for the Watchdog block, core and CPU-Timer 2.
- **Crystal/Resonator Operation:** The on-chip (crystal) oscillator enables the use of an external crystal/resonator attached to the device to provide the time base. The crystal/resonator is connected to the X1/X2 pins. Some devices may not have the X1/X2 pins. See Table 2-2 for details.
- **External clock source operation:** If the on-chip (crystal) oscillator is not used, this mode allows it to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. Note that the XCLKIN is multiplexed with GPIO19 or GPIO38 pin. The XCLKIN input can be selected as GPIO19 or GPIO38 via the XCLKINSEL bit in XCLK register. The CLKCTL[XCLKINOFF] bit disables this clock input (forced low). If the clock source is not used or the respective pins are used as GPIOs, the user should disable at boot time.

Before changing clock sources, ensure that the target clock is present. If a clock is not present, then that clock source must be disabled (using the CLKCTL register) before switching clocks.

Table 3-16. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[DIVSEL]	CLKIN AND SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{XRS}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL itself is bypassed but the PLL is not turned off.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Enable	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0, 1 2	OSCCLK*n/4 OSCCLK*n/2

3.8.4 Loss of Input Clock (NMI watchdog function)

The 2802x devices may be clocked from either one of the internal zero-pin oscillators (INTOSC1/INTOSC2), the on-chip crystal oscillator, or from an external clock input. Regardless of the clock source, in PLL-enabled and PLL-bypass mode, if the input clock to the PLL vanishes, the PLL will issue a limp-mode clock at its output. This limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1-5 MHz.

When the limp mode is activated, a $\overline{CLOCKFAIL}$ signal is generated that is latched as an NMI interrupt. Depending on how the NMIRESETSEL bit has been configured, a reset to the device can be fired immediately or the NMI watchdog counter can issue a reset when it overflows. In addition to this, the Missing Clock Status (MCLKSTS) bit is set. The NMI interrupt could be used by the application to detect the input clock failure and initiate necessary corrective action such as switching over to an alternative clock source (if available) or initiate a shut-down procedure for the system.

If the software does not respond to the clock-fail condition, the NMI watchdog triggers a reset after a preprogrammed time interval. Figure 3-11 shows the interrupt mechanisms involved.

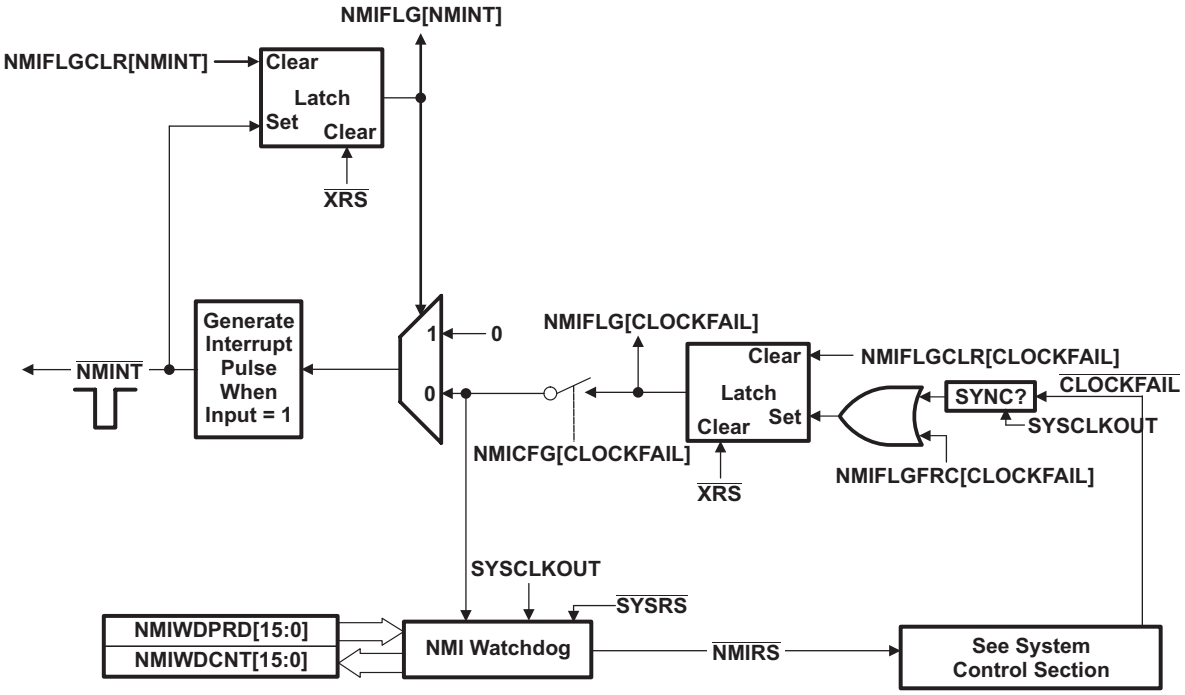


Figure 3-11. NMI-watchdog

3.8.5 CPU-Watchdog Module

The CPU-watchdog module on the 2802x device is similar to the one used on the 281x/280x/283xx devices. This module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user must disable the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register that resets the watchdog counter. Figure 3-12 shows the various functional blocks within the watchdog module.

Normally, when the input clocks are present, the CPU-watchdog counter decrements to initiate a CPU-watchdog reset or WDINT interrupt. However, when the external input clock fails, the CPU-watchdog counter stops decrementing (i.e., the watchdog counter does not change with the limp-mode clock).

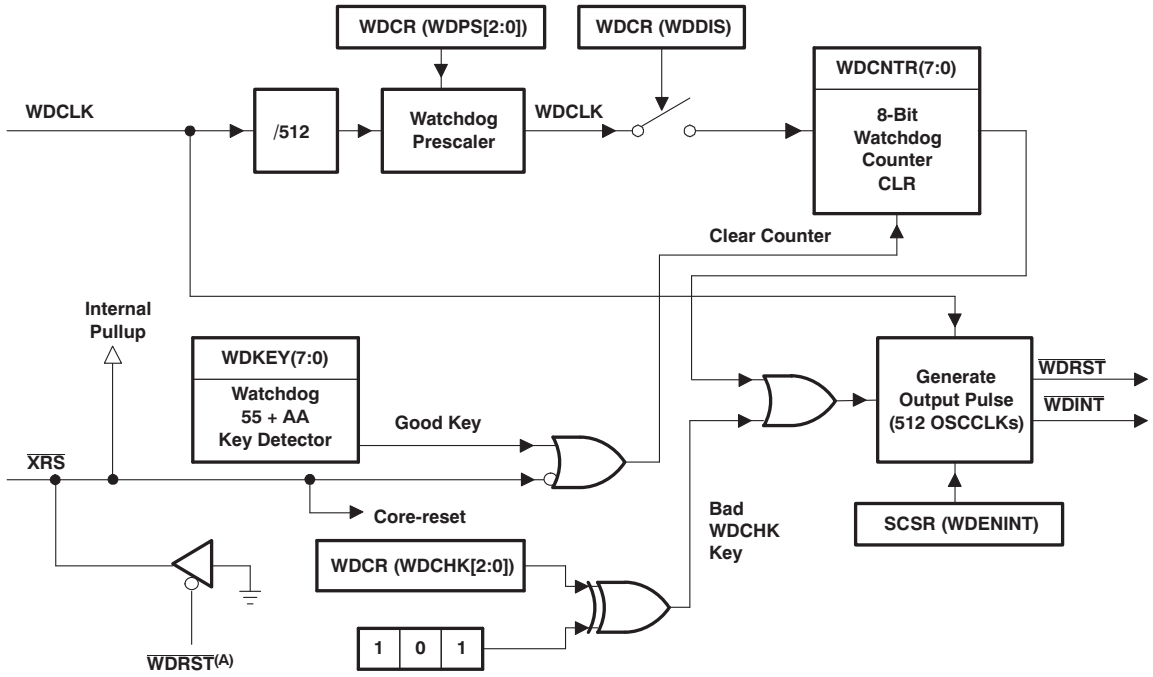
NOTE

The CPU-watchdog counter is different from the NMI watchdog. It is the legacy watchdog counter that is present in all 28x devices.

NOTE

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the MCU will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{\text{XRS}}$ pin of the MCU, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the flash memory.

ADVANCE INFORMATION



A. The WDRST signal is driven low for 512 OSCCLK cycles.

Figure 3-12. CPU-watchdog Module

The WDINT signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the CPU-watchdog. This module will run off OSCCLK. The WDINT signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section Section 3.9, Low-Power Modes Block, for more details.

In IDLE mode, the WDINT signal can generate an interrupt to the CPU, via the PIE, to take the CPU out of IDLE mode.

In HALT mode, the CPU-watchdog can be used to wake up the device through a device reset.

3.9 Low-power Modes Block

Table 3-17 summarizes the various modes.

Table 3-17. Low-power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On	XRS, CPU-watchdog interrupt, any enabled interrupt
STANDBY	01	On (CPU-watchdog still running)	Off	Off	XRS, CPU-watchdog interrupt, GPIO Port A signal, debugger(2)
HALT(3)	1X	Off (on-chip crystal oscillator and PLL turned off, zero-pin oscillator and CPU-watchdog state dependent on user code.)	Off	Off	XRS, GPIO Port A signal, debugger(2), CPU-watchdog

(1) The Exit column lists which signals or under what conditions the low power mode is exited. A low signal, on any of the signals, exits the low power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the low-power mode will not be exited and the device will go back into the indicated low power mode.
(2) The JTAG port can still function even if the CPU clock (CLKIN) is turned off.
(3) The WDCLK must be active for the device to go into HALT mode.

The various low-power modes operate as follows:

IDLE Mode:	This mode is exited by any enabled interrupt that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.
STANDBY Mode:	Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signal(s) will wake the device in the GPIOLPMSEL register. The selected signal(s) are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.
HALT Mode:	CPU-watchdog, $\overline{\text{XRS}}$, and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

NOTE

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the *TMS320x2802x System and Interrupts Reference Guide* (literature number SPRUFN3) for more details.

ADVANCE INFORMATION

4 Peripherals

4.1 Analog Block

A 12-bit ADC core is implemented that has different timings than the 12-bit ADC used on F280x/F2833x. The ADC wrapper is modified to incorporate the new timings and also other enhancements to improve the timing control of start of conversions.

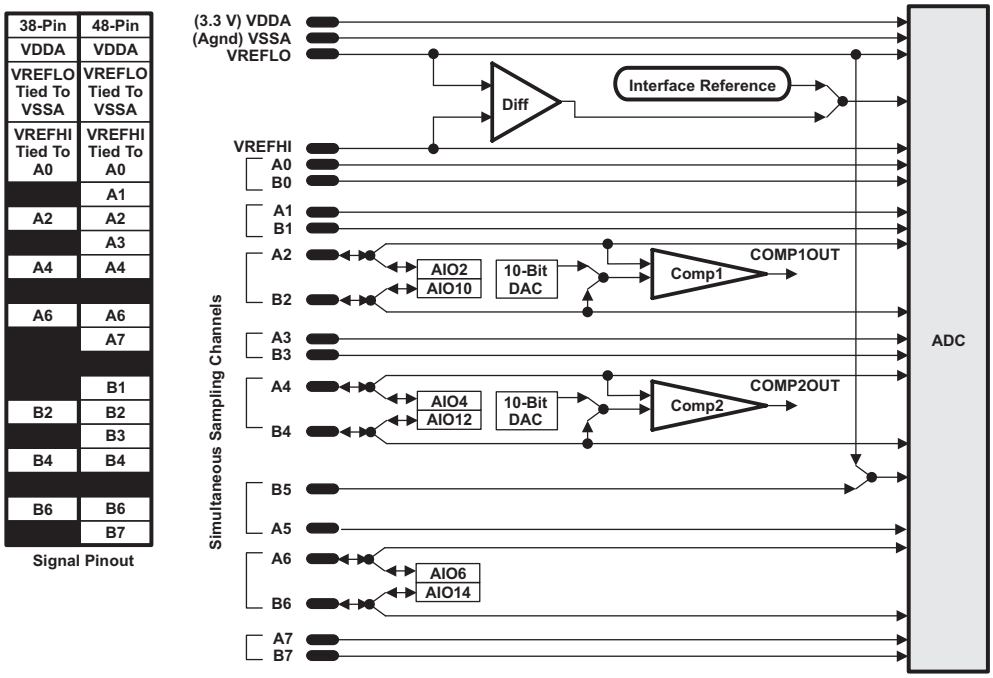


Figure 4-1. Analog Pin Configurations

Figure 4-2 shows the interaction of the analog module with the rest of the F2802x system.

4.1.1 ADC

Table 4-1. ADC Configuration and Control Registers

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCCTL1	0x7100	1	Yes	Control 1 Register
ADCINTFLG	0x7104	1	No	Interrupt Flag Register
ADCINTFLGCLR	0x7105	1	No	Interrupt Flag Clear Register
ADCINTOVF	0x7106	1	No	Interrupt Overflow Register
ADCINTOVFCLR	0x7107	1	No	Interrupt Overflow Clear Register
ADCINTSEL1AND2	0x7108	1	Yes	Interrupt 1 and 2 Selection Register
ADCINTSEL3AND4	0x7109	1	Yes	Interrupt 3 and 4 Selection Register
ADCINTSEL5AND6	0x710A	1	Yes	Interrupt 5 and 6 Selection Register
ADCINTSEL7AND8	0x710B	1	Yes	Interrupt 7 and 8 Selection Register
ADCINTSEL9AND10	0x710C	1	Yes	Interrupt 9 Selection Register (reserved Interrupt 10 Selection)
ADCSOCPRIORITYCTL	0x7110	1	Yes	SOC Priority Control Register
ADCSAMPLEMODE	0x7112	1	Yes	Sampling Mode Register
ADCINTSOCSEL1	0x7114	1	Yes	Interrupt SOC Selection 1 Register (for 8 channels)
ADCINTSOCSEL2	0x7115	1	Yes	Interrupt SOC Selection 2 Register (for 8 channels)

Table 4-1. ADC Configuration and Control Registers (continued)

REGISTER NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
ADCSOCFLG1	0x7118	1	No	SOC Flag 1 Register (for 16 channels)
ADCSOCFRC1	0x711A	1	No	SOC Force 1 Register (for 16 channels)
ADCSOCOVF1	0x711C	1	No	SOC Overflow 1 Register (for 16 channels)
ADCSOCOVFCLR1	0x711E	1	No	SOC Overflow Clear 1 Register (for 16 channels)
ADCSOC0CTL to ADCSOC15CTL	0x7120 - 0x712F	1	Yes	SOC0 Control Register to SOC15 Control Register
ADCREFTRIM	0x7140	1	Yes	Reference Trim Register
ADCOFFTRIM	0x7141	1	Yes	Offset Trim Register
ADCREV	0x714F	1	No	Revision Register

Table 4-2. ADC Result Registers (mapped to PF0)

Name	Address	Size (x16)	EALLOW Protected	Description
ADCRESULT0 to ADCRESULT15	0xB00 - 0xB0F	1	No	ADC Result 0 Register to ADC Result 15 Register

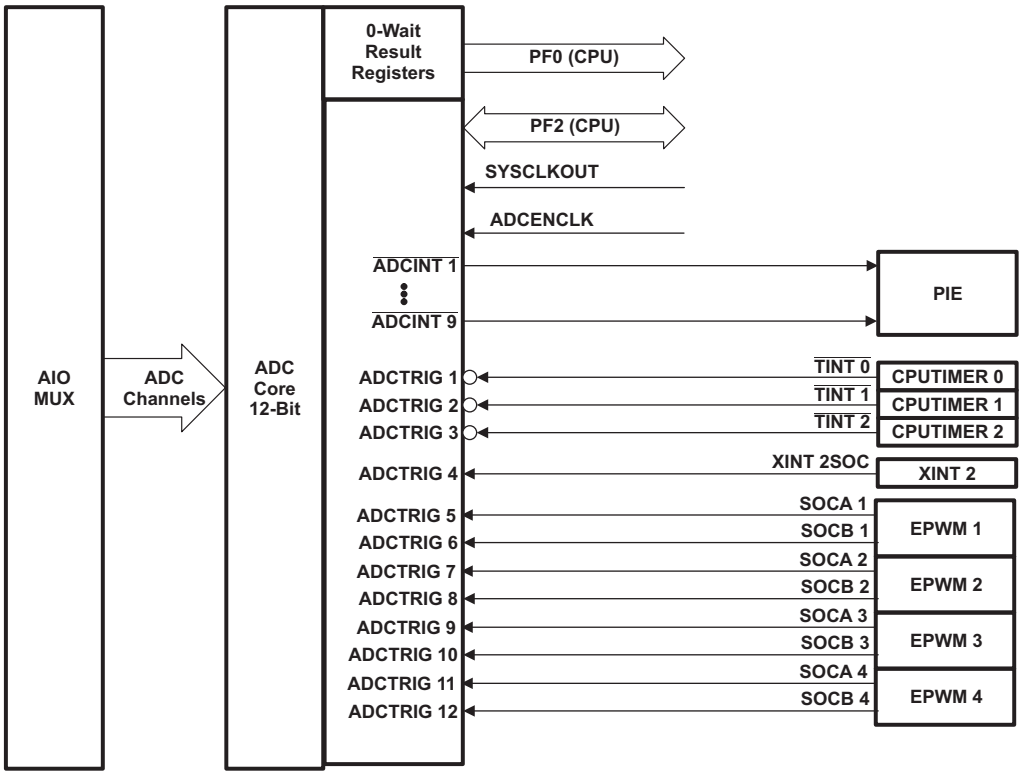


Figure 4-2. ADC Connections

ADVANCE INFORMATION

4.1.2 ADC MUX

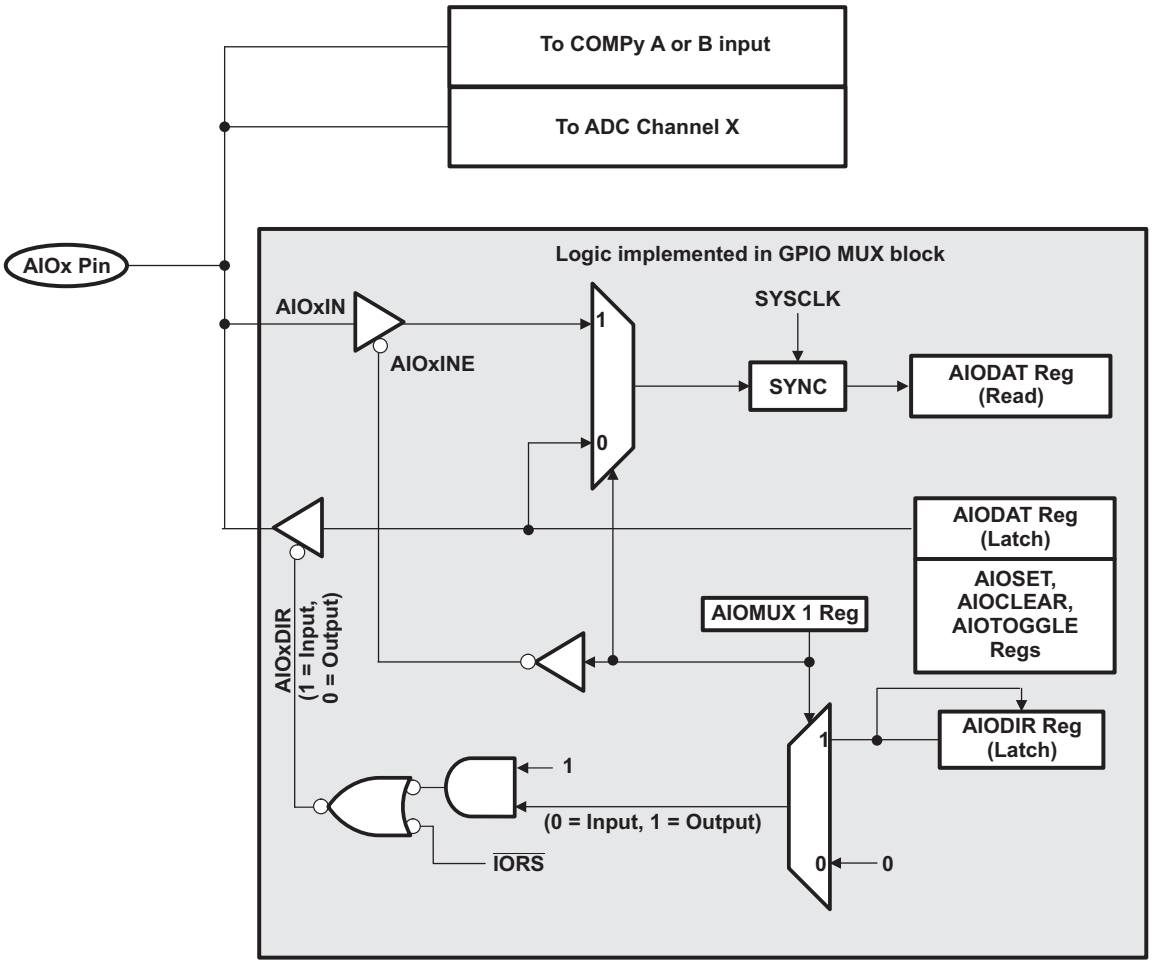


Figure 4-3. ADC MUX

The ADC channel and Comparator functions are always available. The digital I/O function is available only when the respective bit in the AIOMUX1 register is set to 1. In this mode, reading the AIODAT register reflects the actual pin state.

The digital I/O function is disabled when the respective bit in the AIOMUX1 register is cleared to 0. In this mode, reading the AIODAT register reflects the output latch of the AIODAT register and the input digital I/O buffer is disabled to prevent analog signals from generating noise.

On reset, the digital function is disabled. If the pin is used as an analog input, users should keep the AIO function disabled for that pin.

4.1.3 Comparator Block

Figure 4-4 shows the interaction of the Comparator modules with the rest of the system

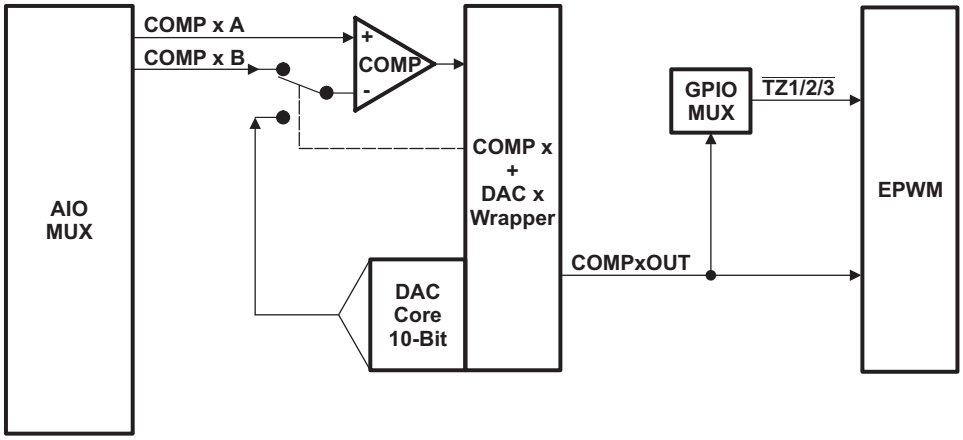


Figure 4-4. Comparator Block Diagram

Table 4-3. Comparator Control Registers

REGISTER NAME	COMP1 ADDRESS	COMP2 ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
COMPCTL	0x6400	0x6420	1	Yes	Comparator Control Register
COMPSTS	0x6402	0x6422	1	No	Comparator Status Register
DACVAL	0x6406	0x6426	1	Yes	DAC Value Register

ADVANCE INFORMATION

4.1 Serial Peripheral Interface (SPI) Module

The device includes the four-pin serial peripheral interface (SPI) module. One SPI module (SPI-A) is available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

NOTE: All four pins can be used as GPIO if the SPI module is not used.

- Two operational modes: master and slave
  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \quad \text{when SPIBRR = 3 to 127}$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \quad \text{when SPIBRR = 0,1, 2}$$

- Data word length: one to sixteen data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: Located in control register frame beginning at address 7040h.

NOTE

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced feature:

- 4-level transmit/receive FIFO
- Delayed transmit control
- Bi-directional 3 wire SPI mode support

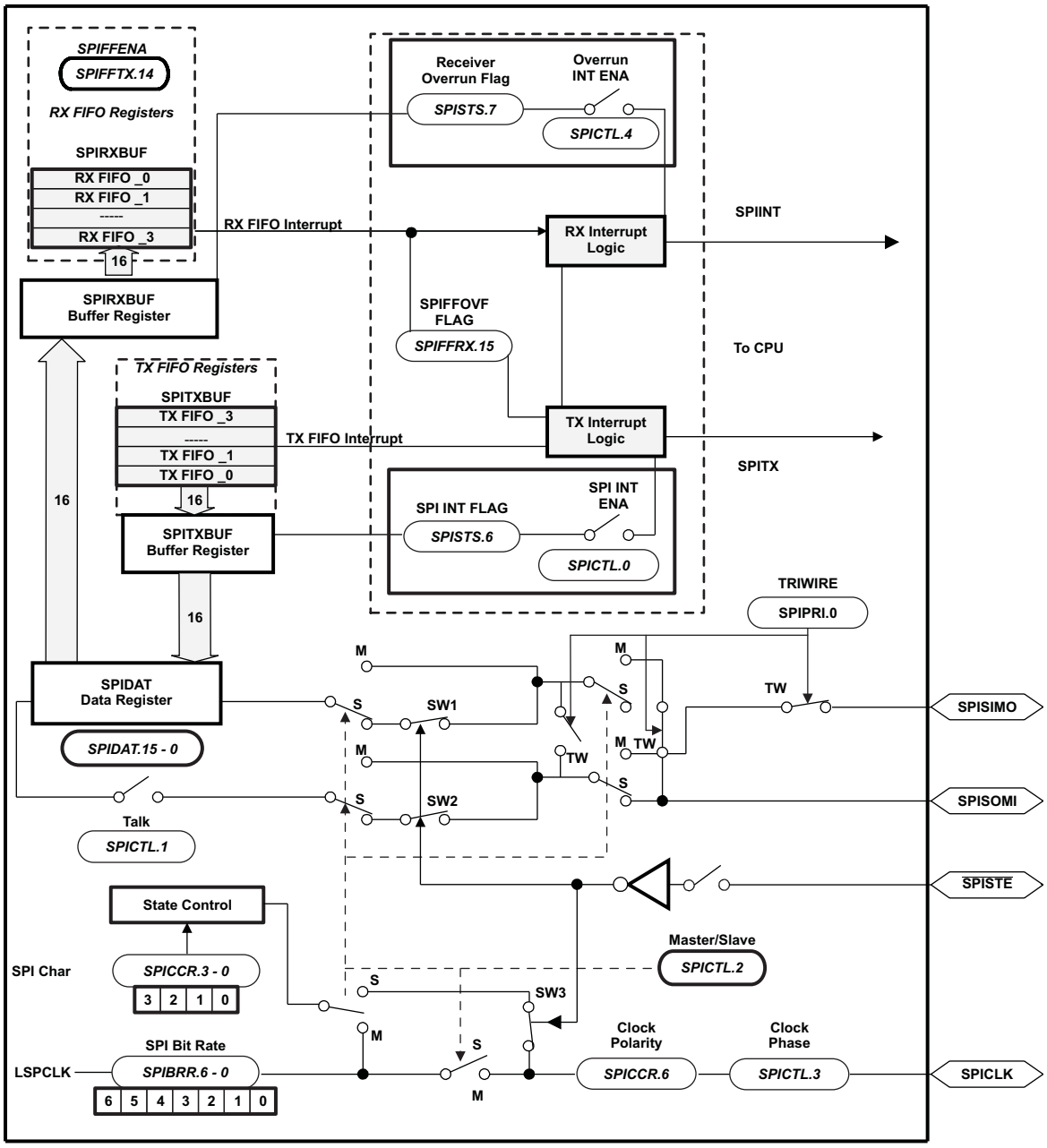
The SPI port operation is configured and controlled by the registers listed in Table 4-4.

Table 4-4. SPI-A Registers

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION(1)
SPICCR	0x7040	1	No	SPI-A Configuration Control Register
SPICTL	0x7041	1	No	SPI-A Operation Control Register
SPISTS	0x7042	1	No	SPI-A Status Register
SPIBRR	0x7044	1	No	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	No	SPI-A Receive Emulation Buffer Register
SPIRXBUF	0x7047	1	No	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	No	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	No	SPI-A Serial Data Register
SPIFFTX	0x704A	1	No	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	No	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	No	SPI-A FIFO Control Register
SPIPRI	0x704F	1	No	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Figure 4-5 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

Figure 4-5. SPI Module Block Diagram (Slave Mode)

4.2 Serial Communications Interface (SCI) Module

The devices include one serial communications interface (SCI) module (SCI-A). The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin
    NOTE: Both pins can be used as GPIO if not used for SCI.
  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \quad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format

NOTE

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7-0), and the upper byte (15-8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 4-level transmit/receive FIFO

The SCI port operation is configured and controlled by the registers listed in Table 4-5.

ADVANCE INFORMATION

Table 4-5. SCI-A Registers(1)

NAME	ADDRESS	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
SCICCRA	0x7050	1	No	SCI-A Communications Control Register
SCICTL1A	0x7051	1	No	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	No	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	No	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	No	SCI-A Control Register 2
SCIRXSTA	0x7055	1	No	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	No	SCI-A Receive Emulation Data Buffer Register
SCIRXBUFA	0x7057	1	No	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	No	SCI-A Transmit Data Buffer Register
SCIFFTXA(2)	0x705A	1	No	SCI-A FIFO Transmit Register
SCIFFRXA(2)	0x705B	1	No	SCI-A FIFO Receive Register
SCIFFCTA(2)	0x705C	1	No	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	No	SCI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Figure 4-6 shows the SCI module block diagram.

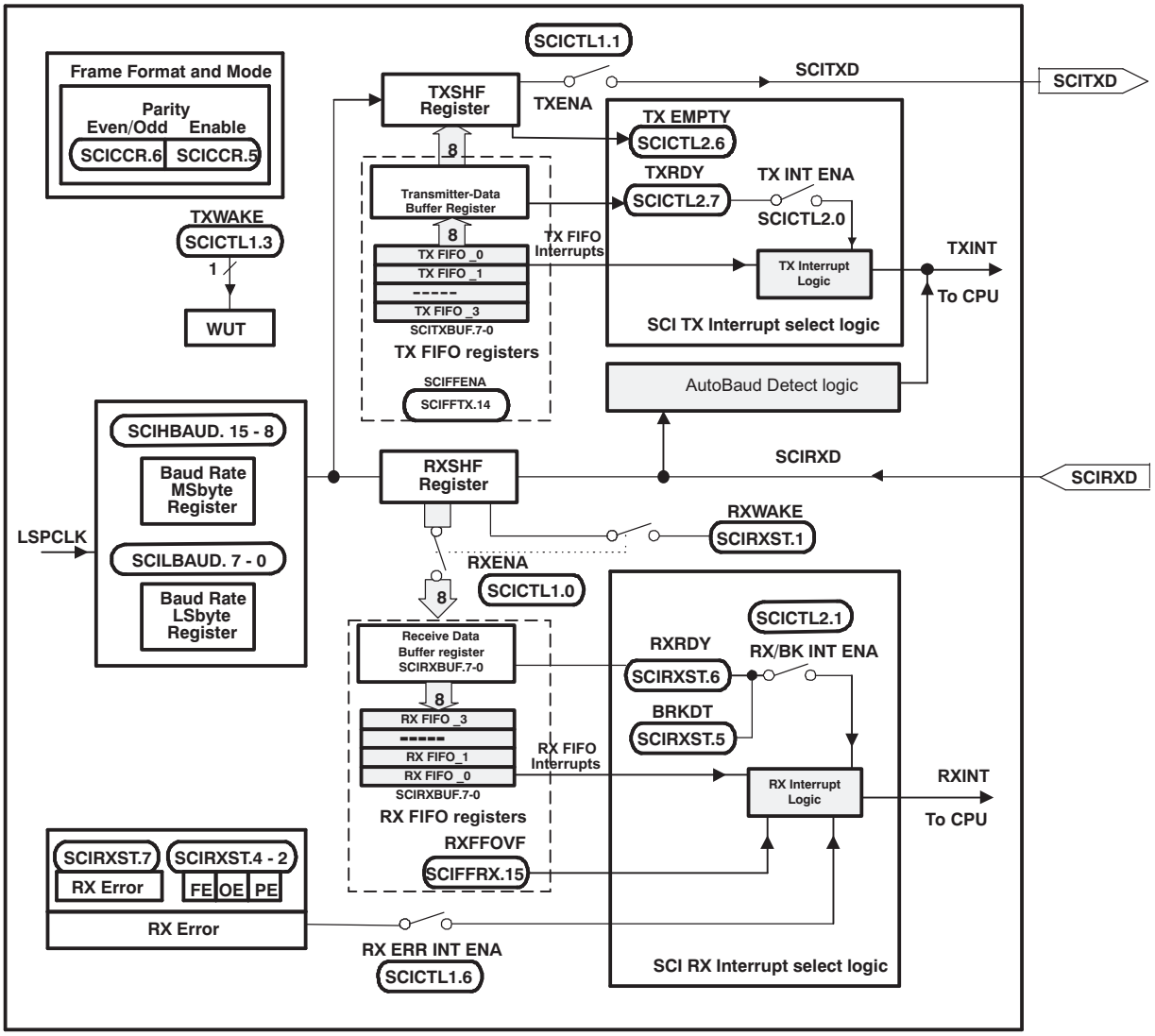


Figure 4-6. Serial Communications Interface (SCI) Module Block Diagram

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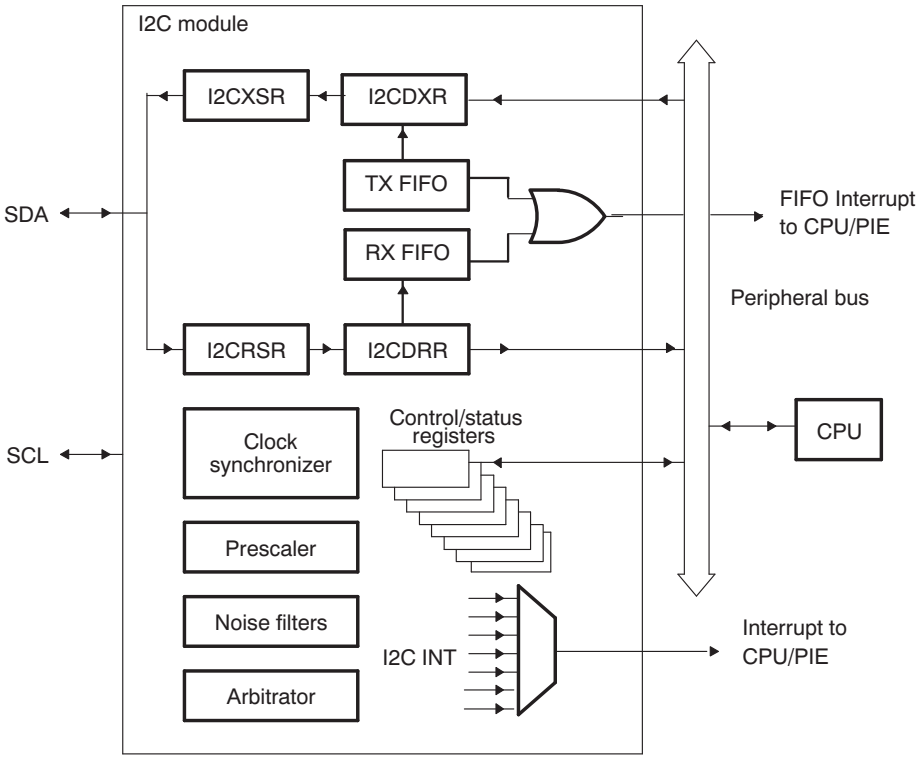
4.3 Inter-Integrated Circuit (I2C)

The device contains one I2C Serial Port. Figure 4-7 shows how the I2C peripheral module interfaces within the device.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode



A. The I2C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I2C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 4-7. I2C Peripheral Module Interfaces

The registers in Table 4-6 configure and control the I2C port operation.

Table 4-6. I2C-A Registers

NAME	ADDRESS	EALLOW PROTECTED	DESCRIPTION
I2COAR	0x7900	No	I2C own address register
I2CIER	0x7901	No	I2C interrupt enable register
I2CSTR	0x7902	No	I2C status register
I2CCLKL	0x7903	No	I2C clock low-time divider register
I2CCLKH	0x7904	No	I2C clock high-time divider register
I2CCNT	0x7905	No	I2C data count register
I2CDRR	0x7906	No	I2C data receive register
I2CSAR	0x7907	No	I2C slave address register
I2CDXR	0x7908	No	I2C data transmit register
I2CMDR	0x7909	No	I2C mode register
I2CISRC	0x790A	No	I2C interrupt source register
I2CPSC	0x790C	No	I2C prescaler register
I2CFFTX	0x7920	No	I2C FIFO transmit register
I2CFFRX	0x7921	No	I2C FIFO receive register
I2CRSR	–	No	I2C receive shift register (not accessible to the CPU)
I2CXSR	–	No	I2C transmit shift register (not accessible to the CPU)

4.4 Enhanced PWM Modules (ePWM1/2/3/4)

The devices contain up to four enhanced PWM Modules (ePWM). Figure 4-8 shows a block diagram of multiple ePWM modules. Figure 4-8 shows the signal interconnections with the ePWM. See the *TMS320x2802x Enhanced Pulse Width Modulator (ePWM) Module Reference Guide* (literature number SPRUGE9) for more details.

Table 4-7 shows the complete ePWM register set per module.

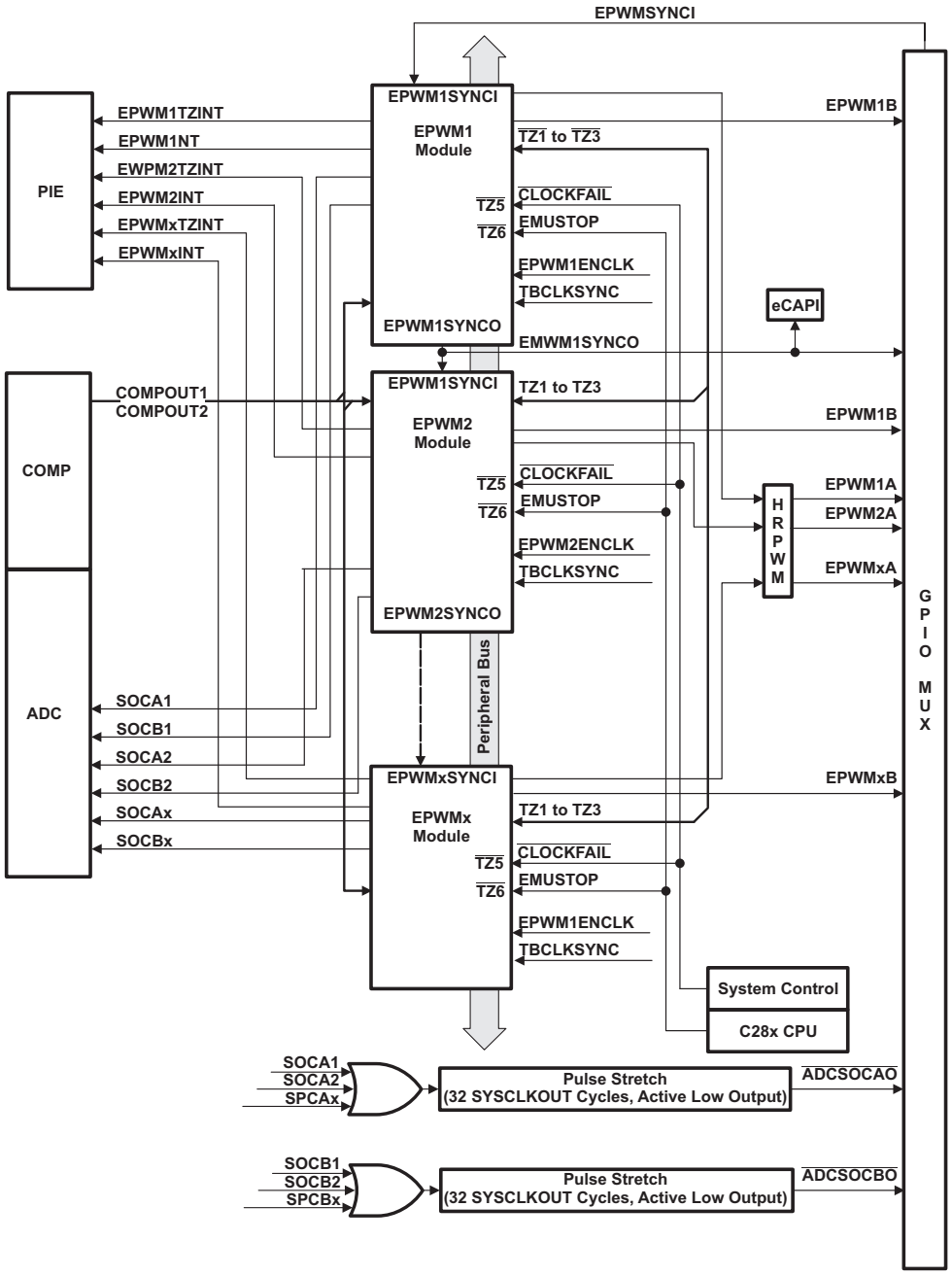


Figure 4-8. ePWM

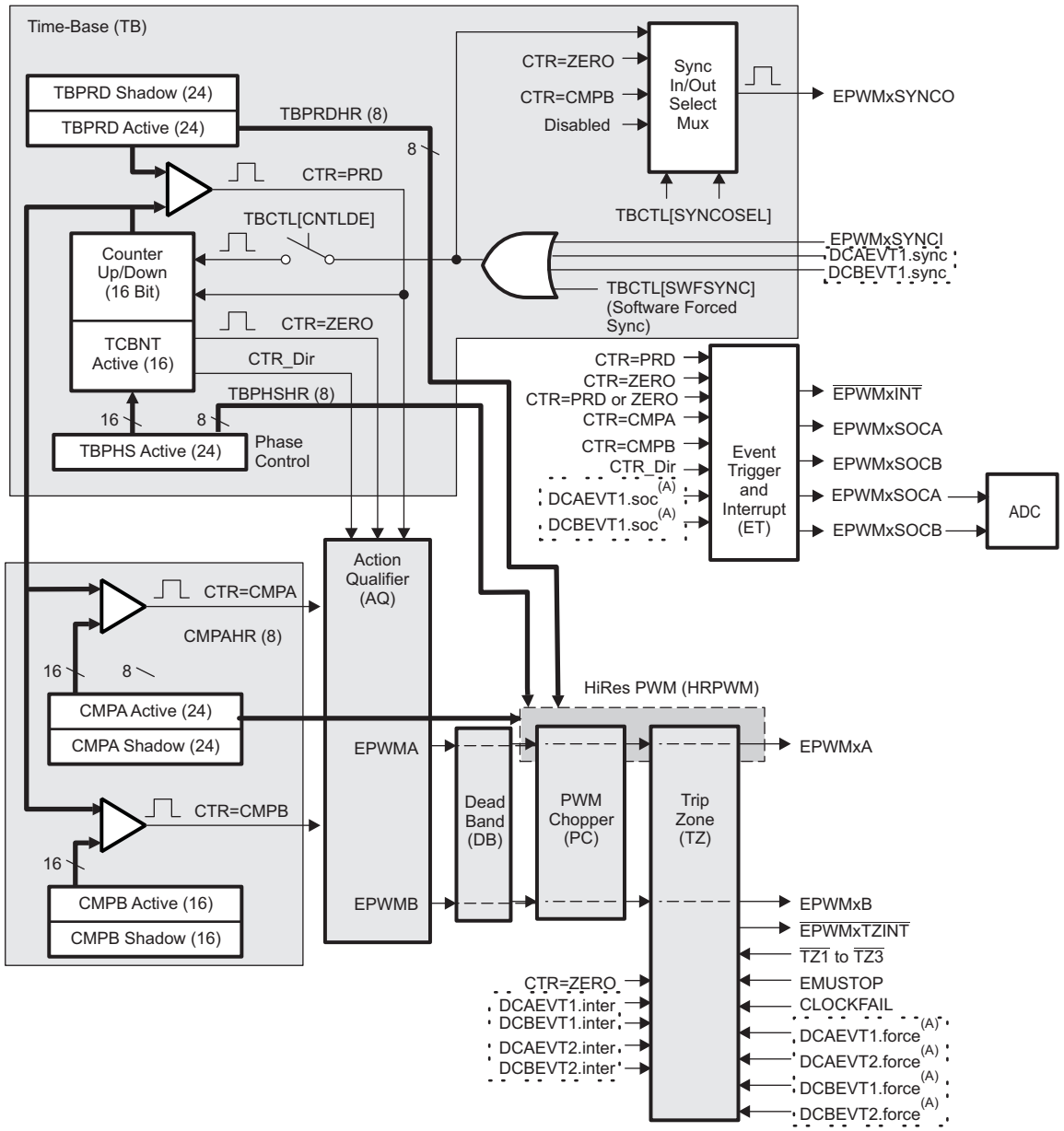
Table 4-7. ePWM Control and Status Registers

NAME	EPWM1	EPWM2	EPWM3	EPWM4	SIZE (x16) / #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	1 / 0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	1 / 0	Time Base Status Register
TBPHSHR	0x6802	0x6842	0x6882	0x68C2	1 / 0	Time Base Phase HRPWM Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	1 / 0	Time Base Phase Register
TBCTR	0x6804	0x6844	0x6884	0x68C4	1 / 0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	1 / 1	Time Base Period Register Set
TBPRDHR	0x6806	0x6846	0x6886	0x68C6	1 / 1	Time Base Period High Resolution Register(1)
CMPCTL	0x6807	0x6847	0x6887	0x68C7	1 / 0	Counter Compare Control Register
CMPAHR	0x6808	0x6848	0x6888	0x68C8	1 / 1	Time Base Compare A HRPWM Register
CMPA	0x6809	0x6849	0x6889	0x68C9	1 / 1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	1 / 1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	1 / 0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	1 / 0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	1 / 0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	1 / 1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	1 / 1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	1 / 0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	1 / 0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	1 / 0	Trip Zone Select Register(1)
TZDCSEL	0x6813	0x6853	0x6893	0x98D3	1 / 0	Trip Zone Digital Compare Register
TZCTL	0x6814	0x6854	0x6894	0x68D4	1 / 0	Trip Zone Control Register(1)
TZEINT	0x6815	0x6855	0x6895	0x68D5	1 / 0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6816	0x6856	0x6896	0x68D6	1 / 0	Trip Zone Flag Register (1)
TZCLR	0x6817	0x6857	0x6897	0x68D7	1 / 0	Trip Zone Clear Register(1)
TZFRC	0x6818	0x6858	0x6898	0x68D8	1 / 0	Trip Zone Force Register(1)
ETSEL	0x6819	0x6859	0x6899	0x68D9	1 / 0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	1 / 0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	1 / 0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	1 / 0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	1 / 0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	1 / 0	PWM Chopper Control Register
HRCNFG	0x6820	0x6860	0x68A0	0x68E0	1 / 0	HRPWM Configuration Register(1)

(1) Registers that are EALLOW protected.

NAME	EPWM1	EPWM2	EPWM3	EPWM4	SIZE (x16) / #SHADOW	DESCRIPTION
HRPWR	0x6821	-	-	-	1 / 0	HRPWM Power Register
HRMSTEP	0x6826	-	-	-	1 / 0	HRPWM MEP Step Register
HRPCTL	0x6828	0x6868	0x68A8	0x68E8	1 / 0	High resolution Period Control Register(1)
TBPRDHRM	0x682A	0x686A	0x68AA	0x68EA	1 / W(2)	Time Base Period HRPWM Register Mirror
TBPRDM	0x682B	0x686B	0x68AB	0x68EB	1 / W(2)	Time Base Period Register Mirror
CMPAHRM	0x682C	0x686C	0x68AC	0x68EC	1 / W(2)	Compare A HRPWM Register Mirror
CMPAM	0x682D	0x686D	0x68AD	0x68ED	1 / W(2)	Compare A Register Mirror
DCTRIPSEL	0x6830	0x6870	0x68B0	0x68F0	1 / 0	Digital Compare Trip Select Register (1)
DCACTL	0x6831	0x6871	0x68B1	0x68F1	1 / 0	Digital Compare A Control Register(1)
DCBCTL	0x6832	0x6872	0x68B2	0x68F2	1 / 0	Digital Compare B Control Register(1)
DCFCTL	0x6833	0x6873	0x68B3	0x68F3	1 / 0	Digital Compare Filter Control Register(1)
DCCAPCT	0x6834	0x6874	0x68B4	0x68F4	1 / 0	Digital Compare Capture Control Register(1)
DCFOFFSET	0x6835	0x6875	0x68B5	0x68F5	1 / 1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6836	0x6876	0x68B6	0x68F6	1 / 0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6837	0x6877	0x68B7	0x68F7	1 / 0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6838	0x6878	0x68B8	0x68F8	1 / 0	Digital Compare Filter Window Counter Register
DCCAP	0x6839	0x6879	0x68B9	0x68F9	1 / 1	Digital Compare Counter Capture Register

(2) W = Write to shadow register



A. These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and $\overline{TZ}$ signals.

Figure 4-9. ePWM Sub-Modules Showing Critical Internal Signal Interconnections

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4.5 High-Resolution PWM (HRPWM)

This module combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be utilized in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled via extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities, when available on a particular device, are offered only on the A signal path of an ePWM module (i.e., on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

NOTE

Between 40 to 50 MHz SYSCLKOUT under worst case process, voltage, and temperature (maximum voltage and minimum temperature) conditions, the MEP step delay may decrease to a point such that the maximum of 254 MEP steps may not cover 1 full SYSCLKOUT cycle. In other words, high-resolution edge control will not be available for the full range of a SYSCLKOUT cycle. If running SFO calibration software, the SFO function will return an error code of “2” when this occurs. See the device-specific HRPWM Reference Guide for more information on this error condition.

4.6 Enhanced CAP Modules (eCAP1)

The device contains an enhanced capture (eCAP) module. Figure 4-10 shows a functional block diagram of a module.

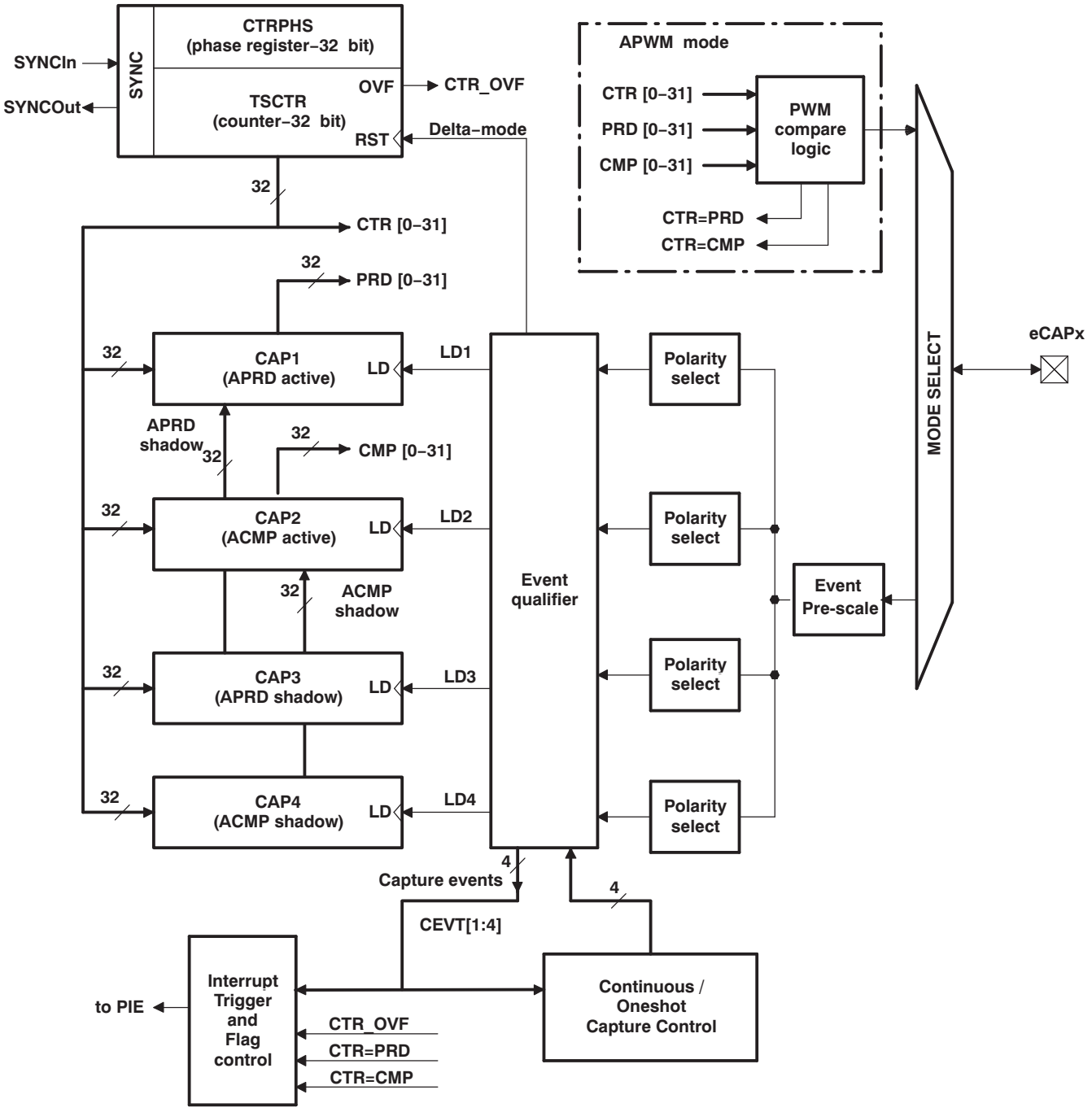

Figure 4-10. eCAP Functional Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

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Table 4-8. eCAP Control and Status Registers

NAME	ECAP1	SIZE (x16)	EALLOW PROTECTED	DESCRIPTION
TSCTR	0x6A00	2		Time-Stamp Counter
CTRPHS	0x6A02	2		Counter Phase Offset Value Register
CAP1	0x6A04	2		Capture 1 Register
CAP2	0x6A06	2		Capture 2 Register
CAP3	0x6A08	2		Capture 3 Register
CAP4	0x6A0A	2		Capture 4 Register
Reserved	0x6A0C- 0x6A12	8		Reserved
ECCTL1	0x6A14	1		Capture Control Register 1
ECCTL2	0x6A15	1		Capture Control Register 2
ECEINT	0x6A16	1		Capture Interrupt Enable Register
ECFLG	0x6A17	1		Capture Interrupt Flag Register
ECCLR	0x6A18	1		Capture Interrupt Clear Register
ECFRC	0x6A19	1		Capture Interrupt Force Register
Reserved	0x6A1A- 0x6A1F	6		Reserved

4.7 JTAG Port

On the 2802x device, the JTAG port is reduced to 5 pins ($\overline{\text{TRST}}$, TCK, TDI, TMS, TDO). TCK, TDI, TMS and TDO pins are also GPIO pins. The $\overline{\text{TRST}}$ signal selects either JTAG or GPIO operating mode for the pins in Figure 4-11.

NOTE

In 2802x devices, the JTAG pins may also be used as GPIO pins. Care should be taken in the board design to ensure that the circuitry connected to these pins do not affect the emulation capabilities of the JTAG pin function. Any circuitry connected to these pins should not prevent the emulator from driving (or being driven by) the JTAG pins for successful debug.

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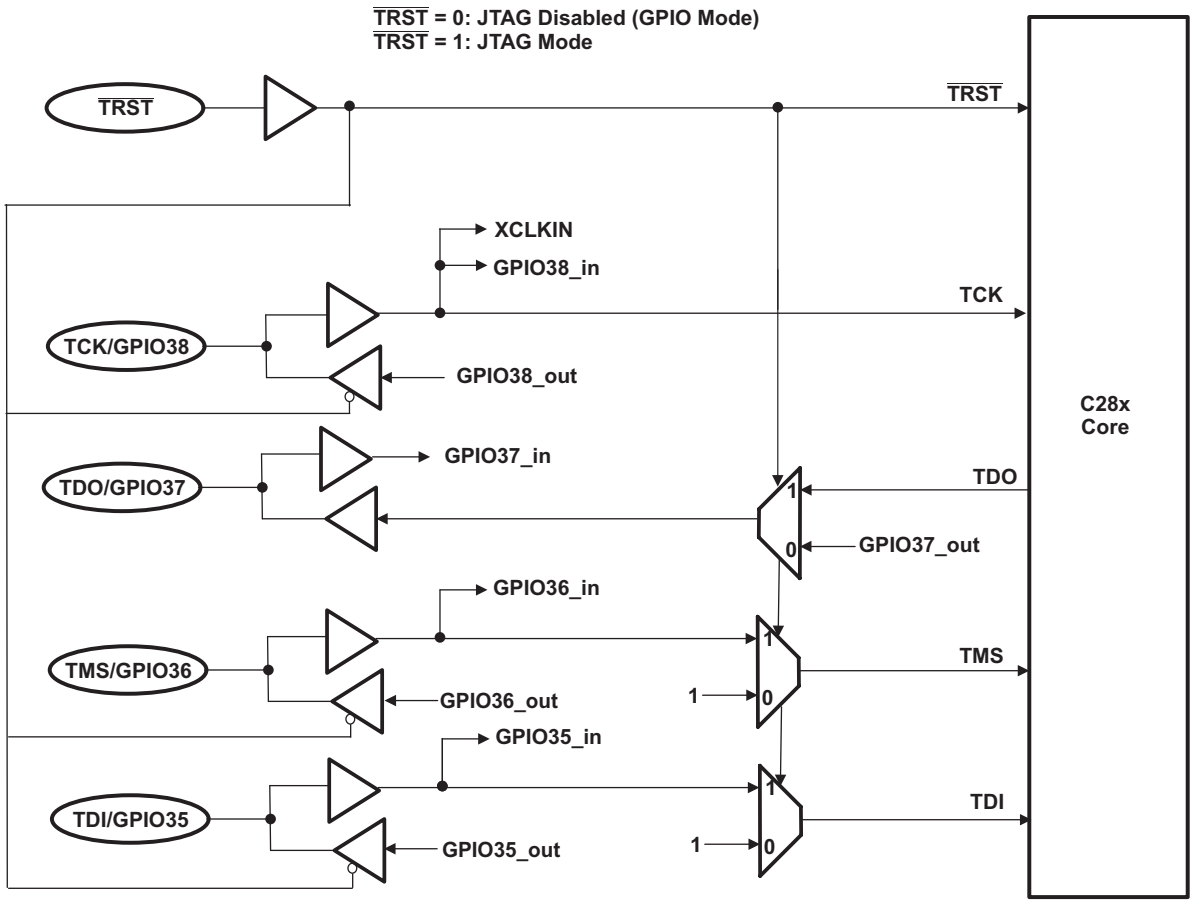

Figure 4-11. JTAG/GPIO Multiplexing

4.8 GPIO MUX

The GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging I/O capability.

The device supports 22 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 4-9 shows the GPIO register mapping.

Table 4-9. GPIO Registers

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16-31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pull Up Disable Register (GPIO0 to 31)
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 38)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 38)
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 38)

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Table 4-9. GPIO Registers (continued)

NAME	ADDRESS	SIZE (x16)	DESCRIPTION
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 38)
GPBPUD	0x6F9C	2	GPIO B Pull Up Disable Register (GPIO32 to 38)
AIOMUX1	0x6FB6	2	Analog, I/O mux 1 register (AIO0 - AIO15)
AIODIR	0x6FBA	2	Analog, I/O Direction Register (AIO0-AIO15)
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO A Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO A Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO A Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO A Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO B Data Register (GPIO32 to 38)
GPBSET	0x6FCA	2	GPIO B Data Set Register (GPIO32 to 38)
GPBCLEAR	0x6FCC	2	GPIO B Data Clear Register (GPIO32 to 38)
GPBTOGGLE	0x6FCE	2	GPIO B Data Toggle Register (GPIO32 to 38)
AIODAT	0x6FD8	2	Analog I/O Data Register (AIO0 - AIO15)
AIOSET	0x6FDA	2	Analog I/O Data Set Register (AIO0 - AIO15)
AIOCLEAR	0x6FDC	2	Analog I/O Data Clear Register (AIO0 - AIO15)
AIOTOGGLE	0x6FDE	2	Analog I/O Data Toggle Register (AIO0 - AIO15)
GPIO INTERRUPT AND LOW POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT3SEL	0x6FE3	1	XINT3 GPIO Input Select Register (GPIO0 to 31)
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)

NOTE

There is a two-SYSCLKOUT cycle delay from when the write to the GPxMUXn/AIOMUXn and GPxQSELn registers occurs to when the action is valid.

Table 4-10. GPIOA MUX

	DEFAULT AT RESET PRIMARY I/O FUNCTION	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPAMUX1 REGISTER BITS	**(GPAMUX1 BITS = 00)**	**(GPAMUX1 BITS = 01)**	**(GPAMUX1 BITS = 10)**	**(GPAMUX1 bits = 11)**
1-0	GPIO0	EPWM1A (O)	Reserved(1)	Reserved(1)
3-2	GPIO1	EPWM1B (O)	Reserved	COMP1OUT (O)
5-4	GPIO2	EPWM2A (O)	Reserved(1)	Reserved(1)
7-6	GPIO3	EPWM2B (O)	Reserved	COMP2OUT (O)
9-8	GPIO4	EPWM3A (O)	Reserved(1)	Reserved(1)
11-10	GPIO5	EPWM3B (O)	Reserved	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPIO7	EPWM4B (O)	SCIRXDA (I)	Reserved
17-16	Reserved	Reserved	Reserved	Reserved
19-18	Reserved	Reserved	Reserved	Reserved
21-20	Reserved	Reserved	Reserved	Reserved
23-22	Reserved	Reserved	Reserved	Reserved
25-24	GPIO12	$\overline{TZ1}$ (I)	SCITXDA (O)	Reserved
27-26	Reserved	Reserved	Reserved	Reserved
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved
GPAMUX2 REGISTER BITS	**(GPAMUX2 BITS = 00)**	**(GPAMUX2 BITS = 01)**	**(GPAMUX2 BITS = 10)**	**(GPAMUX2 BITS = 11)**
1-0	GPIO16	SPISIMOA (I/O)	Reserved	$\overline{TZ2}$ (I)
3-2	GPIO17	SPISOMIA (I/O)	Reserved	$\overline{TZ3}$ (I)
5-4	GPIO18	SPICLKA (I/O)	SCITXDA (O)	XCLKOUT (O)
7-6	GPIO19/XCLKIN	$\overline{SPISTEA}$ (I/O)	SCIRXDA (I)	ECAP1 (I/O)
9-8	Reserved	Reserved	Reserved	Reserved
11-10	Reserved	Reserved	Reserved	Reserved
13-12	Reserved	Reserved	Reserved	Reserved
15-14	Reserved	Reserved	Reserved	Reserved
17-16	Reserved	Reserved	Reserved	Reserved
19-18	Reserved	Reserved	Reserved	Reserved
21-20	Reserved	Reserved	Reserved	Reserved
23-22	Reserved	Reserved	Reserved	Reserved
25-24	GPIO28	SCIRXDA (I)	SDAA (I/OC)	$\overline{TZ2}$ (O)
27-26	GPIO29	SCITXDA (O)	SCLA (I/OC)	$\overline{TZ3}$ (O)
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved

(1) The word reserved means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.

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Table 4-11. GPIOB MUX

	DEFAULT AT RESET PRIMARY I/O FUNCTION	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPBMUX1 REGISTER BITS	(GPBMUX1 BITS = 00)	(GPBMUX1 BITS = 01)	(GPBMUX1 BITS = 10)	(GPBMUX1 BITS = 11)
1-0	GPIO32	SDAA (I/OC)	EPWMSYNCI (I)	$\overline{\text{ADCSOCAO}}$ (O)
3-2	GPIO33	SCLA (I/OC)	EPWMSYNCO (O)	$\overline{\text{ADCSOCBO}}$ (O)
5-4	GPIO34	COMP2OUT (O)	Reserved	Reserved
7-6	GPIO35 (TDI)	Reserved	Reserved	Reserved
9-8	GPIO36 (TMS)	Reserved	Reserved	Reserved
11-10	GPIO37 (TDO)	Reserved	Reserved	Reserved
13-12	GPIO38/XCLKIN (TCK)	Reserved	Reserved	Reserved
15-14	Reserved	Reserved	Reserved	Reserved
17-16	Reserved	Reserved	Reserved	Reserved
19-18	Reserved	Reserved	Reserved	Reserved
21-20	Reserved	Reserved	Reserved	Reserved
23-22	Reserved	Reserved	Reserved	Reserved
25-24	Reserved	Reserved	Reserved	Reserved
27-26	Reserved	Reserved	Reserved	Reserved
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved

Table 4-12. Analog MUX

		DEFAULT AT RESET
	AIOx AND PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2 AND PERIPHERAL SELECTION 3
AIOMUX1 REGISTER BITS	AIOMUX1 BITS = 0,x	AIOMUX1 BITS = 1,x
1-0	A0 (I)	A0 (I)
3-2	A1 (I)	A1 (I)
5-4	AIO2 (I/O)	A2 (I), COMPA1 (I)
7-6	A3 (I)	A3 (I)
9-8	AIO4 (I/O)	A4 (I), COMPA2 (I)
11-10	A5 (I)	A5 (I)
13-12	AIO6 (I/O)	A6 (I)
15-14	A7 (I)	A7 (I)
17-16	B0 (I)	B0 (I)
19-18	B1 (I)	B1 (I)
21-20	AIO10 (I/O)	B2 (I), COMPB1 (I)
23-22	B3 (I)	B3 (I)
25-24	AIO12 (I/O)	B4 (I), COMPB2 (I)
27-26	B5 (I)	B5 (I)
29-28	AIO14 (I/O)	B6 (I)
31-30	B7 (I)	B7 (I)

The user can select the type of input qualification for each GPIO pin via the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2=0, 0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2=0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.
- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. It specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 4-18 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2=1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multi-level multiplexing that is required on the device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.

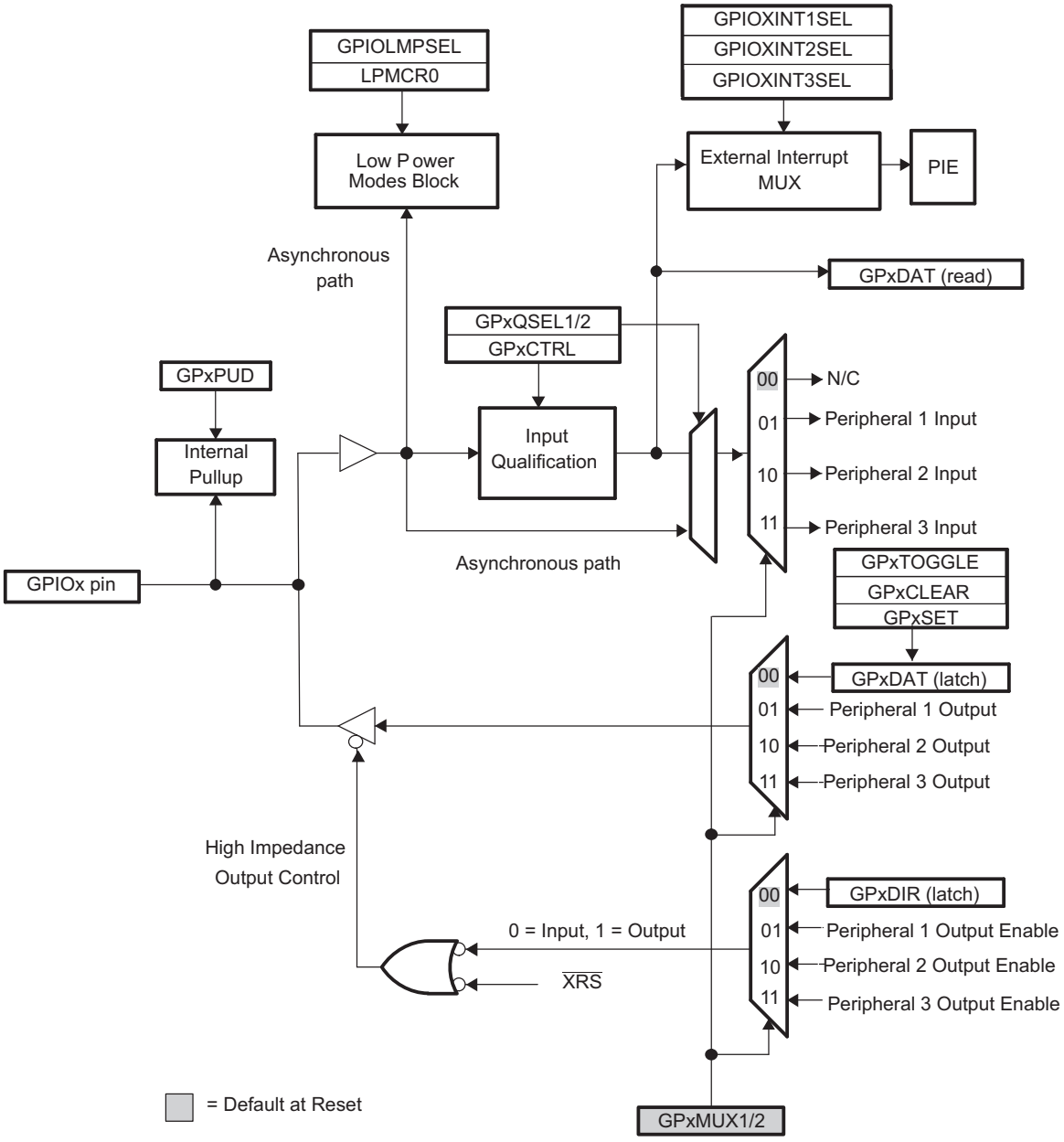

Figure 4-12. GPIO Multiplexing

5 Device Support

Texas Instruments (TI) offers an extensive line of development tools for the C28x™ generation of MCUs, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules.

The following products support development of 2802x-based applications:

Software Development Tools

- Code Composer Studio™ Integrated Development Environment (IDE)
  - C/C++ Compiler
  - Code generation tools
  - Assembler/Linker
  - Cycle Accurate Simulator
- Application algorithms
- Sample applications code

Hardware Development Tools

- Development and evaluation boards
- JTAG-based emulators - XDS510™ Class, XDS100
- Flash programming tools
- Power supply
- Documentation and cables

5.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (e.g., **TMS**320F28025). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications

TMP Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification

TMS Fully qualified production device

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing

TMDS Fully qualified development-support product

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:
"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

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Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, DA) and temperature range (for example, A). Figure 5-1 provides a legend for reading the complete device name for any family member.

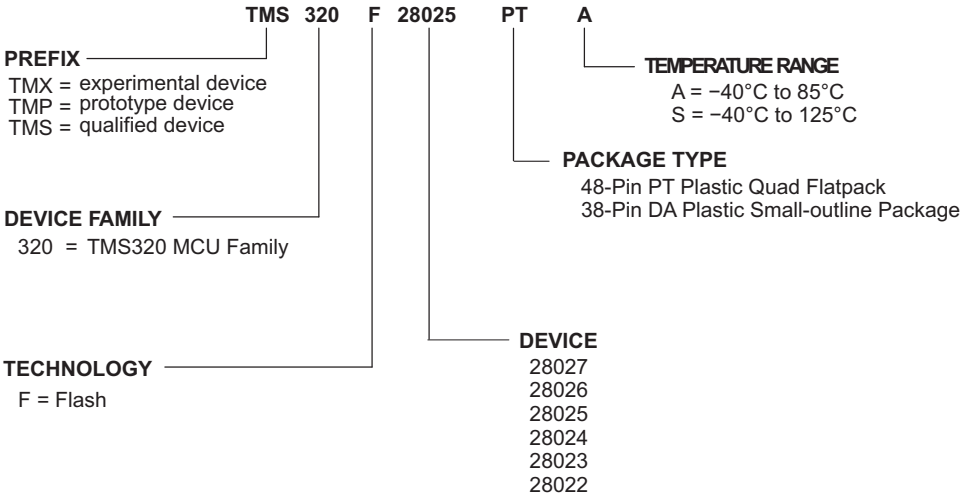

Figure 5-1. Device Nomenclature

5.2 Related Documentation

Extensive documentation supports all of the TMS320™ MCU family generations of devices from product announcement through applications development. The types of documentation available include: data sheets and data manuals, with design specifications; and hardware and software applications.

Table 5-1 shows the peripheral reference guides appropriate for use with the devices in this data manual. See the *TMS320x28xx, 28xxx DSP Peripheral Reference Guide* (SPRU566) for more information on types of peripherals.

Table 5-1. TMS320F2802x Peripheral Selection Guide

Peripheral	Lit. No.	Type(1)	28027, 28026, 28025, 28024, 28023, 28022
TMS320x2802x Piccolo System Control and Interrupts	SPRUFN3	-	X
TMS320x2802x Piccolo Analog-to-Digital Converter and Comparator	SPRUGE5	3/0(2)	X
TMS320x2802x Piccolo Serial Communications Interface (SCI)	SPRUGH1	0	X
TMS320x2802x Piccolo Serial Peripheral Interface (SPI)	SPRUG71	1	X
TMS320x2802x Piccolo Boot ROM	SPRUFN6	-	X
TMS320x2802x Piccolo Enhanced Pulse Width Modulator Module (ePWM)	SPRUGE9	1	X
TMS320x2802x Piccolo Enhanced Capture Module (eCAP)	SPRUFZ8	0	X
TMS320x2802x Piccolo Inter-Integrated Circuit (I2C)	SPRUFZ9	0	X
TMS320x2802x Piccolo High-Resolution Pulse-Width Modulator (HRPWM)	SPRUGE8	1	X

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the peripheral reference guides.
(2) The ADC module is Type 3 and the comparator module is Type 0.

The following documents can be downloaded from the TI website (www.ti.com):

Data Manual

SPRS523 TMS320F28022, 28023, 28024, 28025, 28026, 28027 Microcontrollers (MCUs) contains the pinout, signal descriptions, as well as electrical and timing specifications for the 2802x devices.

SPRZ292 TMS320x28022, 28023, 28024, 28025, 28026, 28027 Piccolo DSP Silicon Errata describes known advisories on silicon and provides workarounds.

CPU User's Guides

SPRU430 TMS320C28x DSP CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). It also describes emulation features available on these DSPs.

Peripheral Guides

SPRU566 TMS320x28xx, 28xxx DSP Peripheral Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

SPRUFN3 TMS320x2802x Piccolo System Control and Interrupts Reference Guide describes the various interrupts and system control features of the C2802x microcontrollers (MCUs).

SPRUFN6 TMS320x2802x Piccolo Boot ROM Reference Guide describes the purpose and features of the bootloader (factory-programmed boot-loading software) and provides examples of code. It also describes other contents of the device on-chip boot ROM and identifies where all of the information is located within that memory.

SPRUGE5 TMS320x2802x Piccolo Analog-to-Digital Converter (ADC) and Comparator Reference Guide describes how to configure and use the on-chip ADC module, which is a 12-bit pipelined ADC.

SPRUGE9 TMS320x2802x Piccolo Enhanced Pulse Width Modulator (ePWM) Module Reference Guide describes the main areas of the enhanced pulse width modulator that include digital motor control, switch mode power supply control, UPS (uninterruptible power supplies), and other forms of power conversion.

SPRUGE8 TMS320x2802x Piccolo High-Resolution Pulse Width Modulator (HRPWM) describes the operation of the high-resolution extension to the pulse width modulator (HRPWM).

SPRUGH1 TMS320x2802x Piccolo Serial Communications Interface (SCI) Reference Guide describes how to use the SCI.

SPRUFZ8 TMS320x2802x Piccolo Enhanced Capture (eCAP) Module Reference Guide describes the enhanced capture module. It includes the module description and registers.

SPRUG71 TMS320x2802x Piccolo Serial Peripheral Interface (SPI) Reference Guide describes the SPI - a high-speed synchronous serial input/output (I/O) port - that allows a serial bit stream of programmed length (one to sixteen bits) to be shifted into and out of the device at a programmed bit-transfer rate.

SPRUFZ9 TMS320x2802x Piccolo Inter-Integrated Circuit (I2C) Reference Guide describes the features and operation of the inter-integrated circuit (I2C) module.

Tools Guides

SPRU513 TMS320C28x Assembly Language Tools User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

SPRU514 TMS320C28x Optimizing C Compiler User's Guide describes the TMS320C28x™ C/C++

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compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

SPRU608 The TMS320C28x Instruction Set Simulator Technical Overview describes the simulator, available within the Code Composer Studio for TMS320C2000 IDE, that simulates the instruction set of the C28x™ core.

6 Electrical Specifications

6.1 Absolute Maximum Ratings[1][2]

Unless otherwise noted, the list of absolute maximum ratings are specified over operating temperature ranges.

Supply voltage range, V_{DDIO} (I/O and Flash)	with respect to V_{SS}	– 0.3 V to 4.6 V
Supply voltage range, V_{DD}	with respect to V_{SS}	– 0.3 V to 2.5 V
Analog voltage range, V_{DDA}	with respect to V_{SSA}	– 0.3 V to 4.6 V
Input voltage range, V_{IN} (3.3 V)		– 0.3 V to 4.6 V
Output voltage range, V_O		– 0.3 V to 4.0 V
Input clamp current, I_{IK} (V_{IN} < 0 or V_{IN} > V_{DDIO})[3]		± 20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{DDIO})		± 20 mA
Operating ambient temperature ranges	T_A: A version	– 40°C to 85°C
	T_A: S version	– 40°C to 125°C
Junction temperature range, T_j		– 40°C to 150°C
Storage temperature range, T_{stg}		– 65°C to 150°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Section 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted.
(3) Continuous clamp current per pin is ± 2 mA.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		2.97	3.3	3.63	V
Device supply voltage CPU, V_{DD} (When internal VREG is disabled and 1.8 V is supplied externally)		1.71	1.8	1.995	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA}		2.97	3.3	3.63	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)	28022, 28023, 28024, 28025	2		40	MHz
	28026, 28027	2		60	
High-level input voltage, V_{IH}(3.3 V)		2		V_{DDIO}	V
Low-level input voltage, V_{IL} (3.3 V)				0.8	V
High-level output source current, V_{OH} = $V_{OH(MIN)}$, I_{OH}	All GPIO pins		– 4		mA
	Group 2[1]		– 8		mA
Low-level output sink current, V_{OL} = $V_{OL(MAX)}$, I_{OL}	All GPIO pins		4		mA
	Group 2[1]		8		mA
Ambient temperature, T_A	T_A: A version	– 40		85	°C
	T_A: S version	– 40		125	°C
Junction temperature, T_J				125	°C

(1) Group 2 pins are as follows: GPIO16, GPIO17, GPIO18, GPIO19, GPIO28, GPIO29, GPIO36, GPIO37

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6.3 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		$I_{OH} = I_{OH}MAX$		2.4			V
			I_{OH} = 50 µA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		$I_{OL} = I_{OL}MAX$				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All I/Os (including $\overline{XRS}$)		– 100		µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				± 2	
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DDIO}$				± 2	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, $V_{IN} = V_{DDIO}$			100		
I_{OZ}	Output current, pullup or pulldown disabled		$V_O = V_{DDIO}$ or 0 V				± 2	µA
C_I	Input capacitance					2		pF

6.4 Current Consumption

Table 6-1. TMS320F2802x Current Consumption at 40-MHz SYSCLKOUT

MODE	TEST CONDITIONS	VREG ENABLED				VREG DISABLED					
		I_{DDIO}		I_{DDA}		I_{DD}		I_{DDIO} (1)		I_{DDA} (2)	
		TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP (3)	MAX	TYP	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3/4 • eCAP • SCI-A • SPI-A • ADC • I2C • COMP1/2 • CPU Timer0/1/2 All PWM pins are toggled at 40 kHz. All I/O pins are left unconnected. (4) Code is running out of flash with 1 wait-state. XCLKOUT is turned off.	75 mA		13 mA		60 mA		15 mA		15 mA	
IDLE	Flash is powered down. XCLKOUT is turned off. All peripheral clocks are off. (5)	14 mA		100 µA		15 mA		200 µA		100 µA	
STANDBY	Flash is powered down. Peripheral clocks are off.	4 mA		25 µA		4 mA		200 µA		25 µA	
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled.	100 µA		25 µA		50 µA		50 µA		25 µA	

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) In order to realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(3) The TYP numbers are applicable over room temperature and nominal voltage.
(4) The following is done in a loop:
- Data is continuously transmitted out of SPI-A and SCI-A ports.
- The hardware multiplier is exercised.
- Watchdog is reset.
- ADC is performing coninuous conversion.
- COMP1/2 are continuously switching voltages.
- GPIO17 is toggled.

(5) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.

Table 6-2. TMS320F2802x Current Consumption at 60-MHz SYSCLKOUT

MODE	TEST CONDITIONS	VREG ENABLED				VREG DISABLED					
		I_{DDIO}		I_{DDA}		I_{DD}		I_{DDIO} (1)		I_{DDA} (2)	
		TYP(3)	MAX	TYP(3)	MAX	TYP(3)	MAX	TYP(3)	MAX	TYP	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1/2/3/4 • eCAP1 • SCI-A • SPI-A • ADC • I2C • COMP1/2 • CPU-TIMER0/1/2 All PWM pins are toggled at 60 kHz. All I/O pins are left unconnected.(4)(5) Code is running out of flash with 2 wait-states. XCLKOUT is turned off.	92 mA		13 mA		76 mA		15 mA		13 mA	
IDLE	Flash is powered down. XCLKOUT is turned off. All peripheral clocks are turned off.	20 mA		100 µA		20 mA		200 µA		100 µA	
STANDBY	Flash is powered down. Peripheral clocks are off.	5 mA		25 µA		4 mA		200 µA		25 µA	
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled.	100 µA		25 µA		50 µA		50 µA		25 µA	

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) In order to realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(3) The TYP numbers are applicable over room temperature and nominal voltage.
(4) The following is done in a loop:
- Data is continuously transmitted out of SPI-A and SCI-A ports.
- The hardware multiplier is exercised.
- Watchdog is reset.
- ADC is performing coninuous conversion.
- COMP1/2 are continuously switching voltages.
- GPIO17 is toggled.

(5) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.

NOTE

The peripheral - I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

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6.4.1 Reducing Current Consumption

The 2802x devices incorporate a method to reduce the device current consumption. Since each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. Table 6-3 indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 6-3. Typical Current Consumption by Various Peripherals (at 60 MHz)(1)

PERIPHERAL MODULE(2)	I_{DD} CURRENT REDUCTION (mA)
ADC	2(3)
I2C	3
ePWM	2
eCAP	2
SCI	2
SPI	2
COMP/DAC	1
HRPWM	3
CPU-TIMER	1
Internal zero-pin oscillator	0.5

(1) All peripheral clocks are disabled upon reset. Writing to/reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.
(3) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well.

NOTE

I_{DDIO} current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

NOTE

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 45 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

Following are other methods to reduce power consumption further:

- The flash module may be powered down if code is run off SARAM. This results in a current reduction of 18 mA (typical) in the V_{DD} rail and 13 mA (typical) in the V_{DDIO} rail.
- Savings in I_{DDIO} may be realized by disabling the pullups on pins that assume an output function.

6.4.2 Current Consumption Graphs (VREG Enabled)

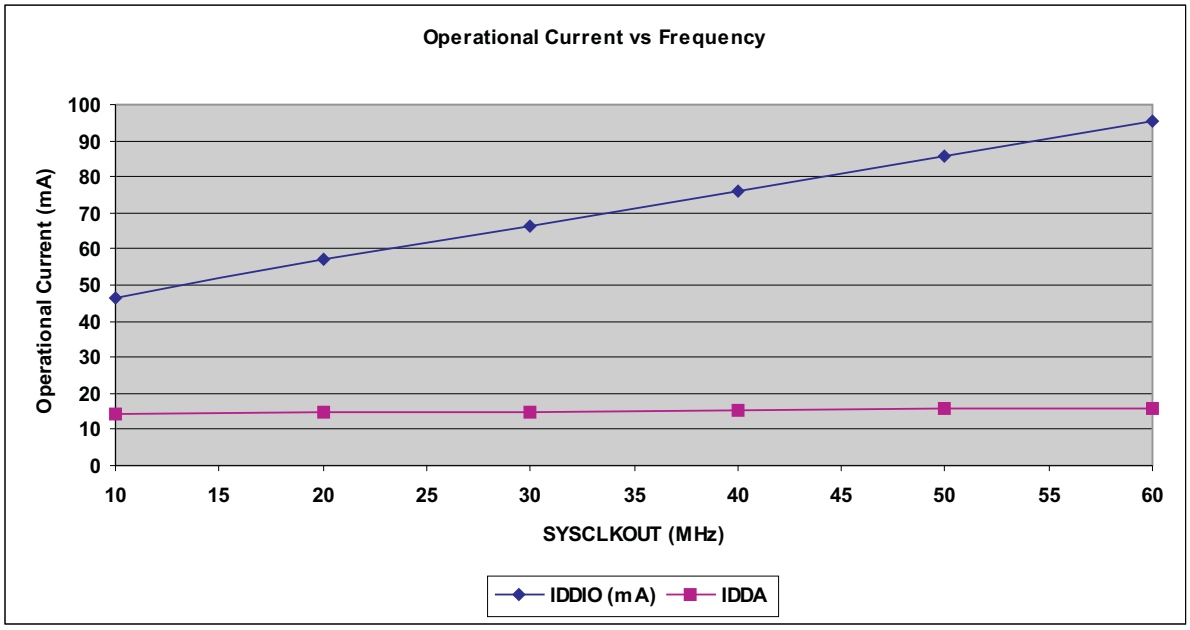


Figure 6-1. Typical Operational Current Versus Frequency (F2802x)

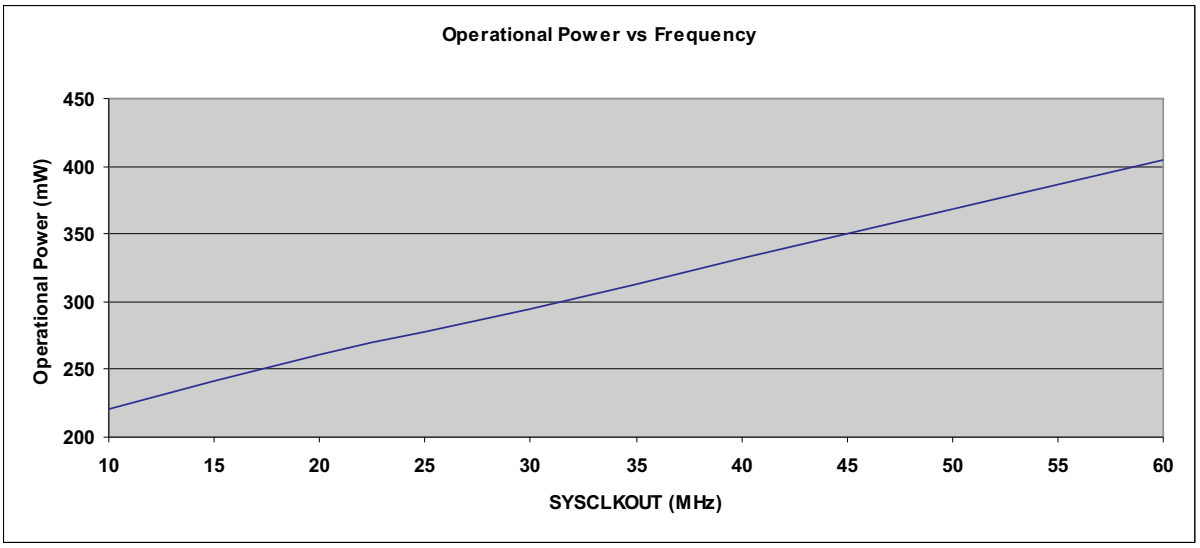
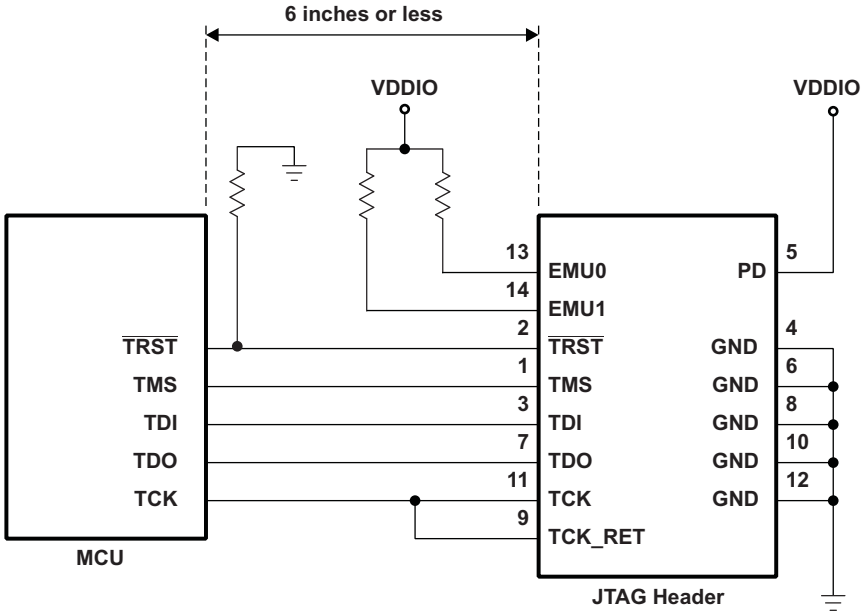


Figure 6-2. Typical Operational Power Versus Frequency (F2802x)

6.5 Emulator Connection Without Signal Buffering for the MCU

Figure 6-3 shows the connection between the MCU and JTAG header for a single-processor configuration. If the distance between the JTAG header and the MCU is greater than 6 inches, the emulation signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 6-3 shows the simpler, no-buffering situation. For the pullup/pulldown resistor values, see the pin description section.



A. See Figure 4-11 for JTAG/GPIO multiplexing.

Figure 6-3. Emulator Connection Without Signal Buffering for the MCU

NOTE

The 2802x devices do not have EMU0/EMU1 pins. For designs that have a JTAG Header on-board, the EMU0/EMU1 pins on the header must be tied to V_{DDIO} through a 4.7 kΩ (typical) resistor.

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6.6 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:		Letters and symbols and their meanings:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

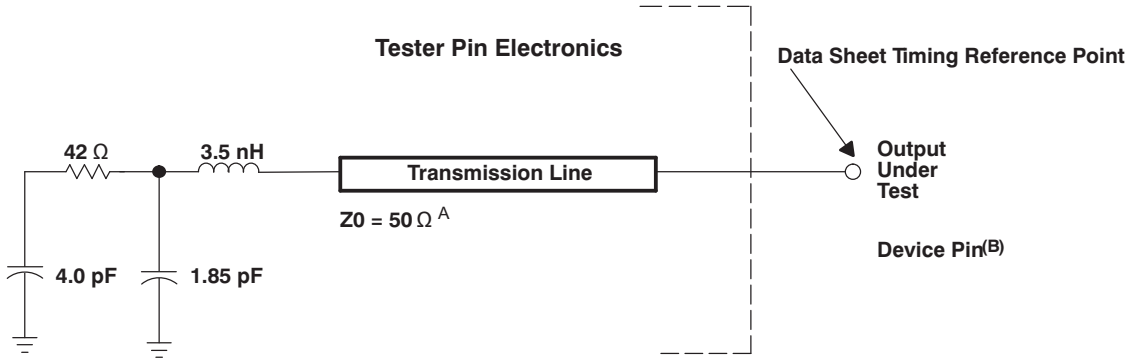
6.6.1 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

6.6.2 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



A. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

B. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 6-4. 3.3-V Test Load Circuit

6.6.3 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the 2802x MCUs. Table 6-4 and Table 6-5 list the cycle times of various clocks.

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Table 6-4. 2802x Clock Table and Nomenclature (40-MHz Devices)

		MIN	NOM	MAX	UNIT
Internal zero-pin oscillator 1 (INTOSC1)	$t_{c(ZPOSC1)}$, Cycle time		100		ns
	Frequency		10		MHz
Internal zero-pin oscillator 2 (INTOSC2)	$t_{c(ZPOSC2)}$, Cycle time		100		ns
	Frequency		10		MHz
On-chip crystal oscillator (X1/X2 pins)	$t_{c(OSC)}$, Cycle time	28.6		50	ns
	Frequency	20		35	MHz
XCLKIN	$t_{c(CI)}$, Cycle time	25		250	ns
	Frequency	4		40	MHz
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	25		500	ns
	Frequency	2		40	MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time	50		2000	ns
	Frequency	0.5		20	MHz
LSPCLK(1)	$t_{c(LCO)}$, Cycle time	25	100(2)		ns
	Frequency		10(2)	40	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	25			ns
	Frequency			40	MHz

(1) Lower LSPCLK will reduce device power consumption.
(2) This is the default reset value if SYSCLKOUT = 40 MHz.

Table 6-5. 2802x Clock Table and Nomenclature (60-MHz Devices)

		MIN	NOM	MAX	UNIT
Internal zero-pin oscillator 1 (INTOSC1)	$t_{c(ZPOSC1)}$, Cycle time		100		ns
	Frequency		10		MHz
Internal zero-pin oscillator 2 (INTOSC2)	$t_{c(ZPOSC2)}$, Cycle time		100		ns
	Frequency		10		MHz
On-chip crystal oscillator (X1/X2 pins)	$t_{c(OSC)}$, Cycle time	28.6		50	ns
	Frequency	20		35	MHz
XCLKIN	$t_{c(CI)}$, Cycle time	16.67		250	ns
	Frequency	4		60	MHz
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	16.67		500	ns
	Frequency	2		60	MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time	50		2000	ns
	Frequency	0.5		20	MHz
LSPCLK(1)	$t_{c(LCO)}$, Cycle time	16.67	66.7(2)		ns
	Frequency		15(2)	60	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	16.67			ns
	Frequency			60	MHz

(1) Lower LSPCLK will reduce device power consumption.
(2) This is the default reset value if SYSCLKOUT = 60 MHz.

6.7 Clock Requirements and Characteristics

Table 6-6. Input Clock Frequency

PARAMETER				MIN	TYP	MAX	UNIT
f_x	Input clock frequency	Resonator (X1/X2)		20		35	MHz
		Crystal (X1/X2)		20		35	
		External oscillator/clock source (XCLKIN pin)	40-MHz device	4		40	
			60-MHz device	4		60	
f_l	Limp mode SYSCLKOUT frequency range (with /2 enabled)				1-5		MHz

Table 6-7. XCLKIN Timing Requirements - PLL Enabled

NO.			MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN	33.3	200	ns
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45	55	%

Table 6-8. XCLKIN Timing Requirements - PLL Disabled

NO.				MIN	MAX	UNIT
C8	$t_{c(CI)}$	Cycle time, XCLKIN	40-MHz device	25	250	ns
			60-MHz device	16.67	250	
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 60 MHz		2	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 60 MHz		2	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$		45	55	%
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$		45	55	%

The possible configuration modes are shown in Table 3-16.

Table 6-9. XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)(1)(2)

NO.	PARAMETER			MIN	TYP	MAX	UNIT
C1	$t_{c(XCO)}$	Cycle time, XCLKOUT	40-MHz device	50			ns
			60-MHz device	50			
C3	$t_{f(XCO)}$	Fall time, XCLKOUT			2		ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT			2		ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low		H-2		H+2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high		H-2		H+2	ns
	t_p	PLL lock time				1 (3)	ms

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$
(3) The PLLLOCKPRD register must be updated based on the number of OSCCLK cycles.

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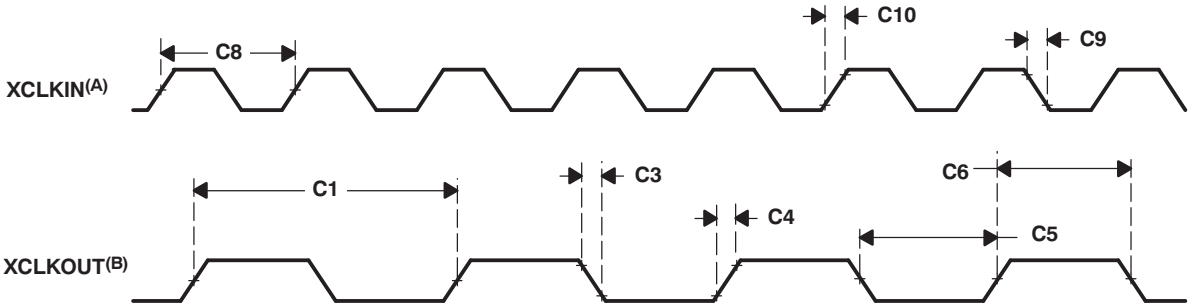


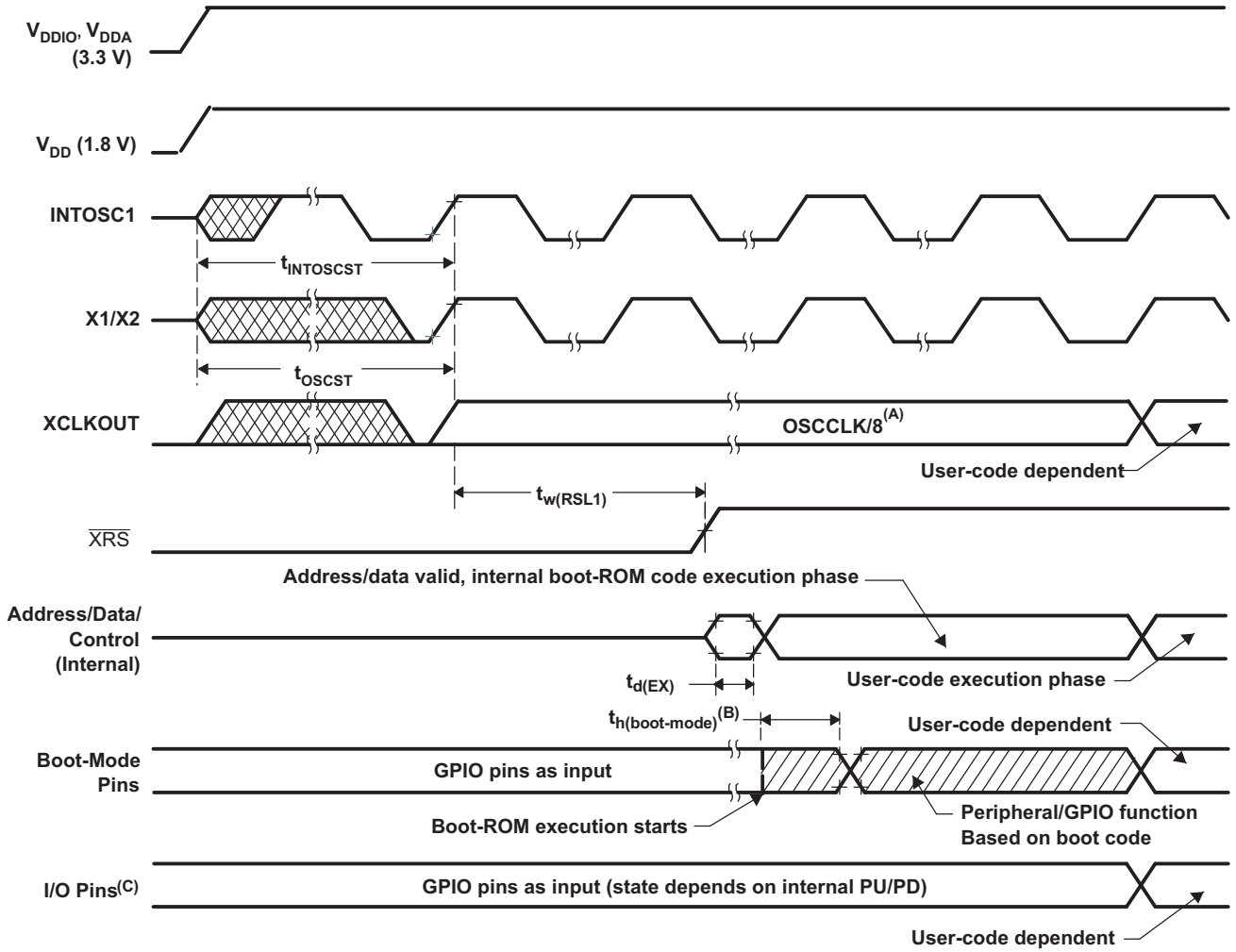
A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.

B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 6-5. Clock Timing

6.8 Power Sequencing

There is no power sequencing requirement. However, it is recommended that no voltage larger than a diode drop (0.7 V) should be applied to any pin prior to powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.



A. Upon power up, SYSCLKOUT is OSCCLK/2. Since the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. This explains why XCLKOUT = OSCCLK/8 during this phase.

B. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

C. See Section 6.8 for requirements to ensure a high-impedance state for GPIO pins during power-up.

Figure 6-6. Power-on Reset

Table 6-10. Reset ($\overline{XRS}$) Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{h(boot-mode)}$	Hold time for boot-mode pins	TBD			cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{XRS}$ low on warm reset		$8t_{c(OSCCLK)}$		cyclies

Table 6-11. Reset ($\overline{XRS}$) Switching Characteristics

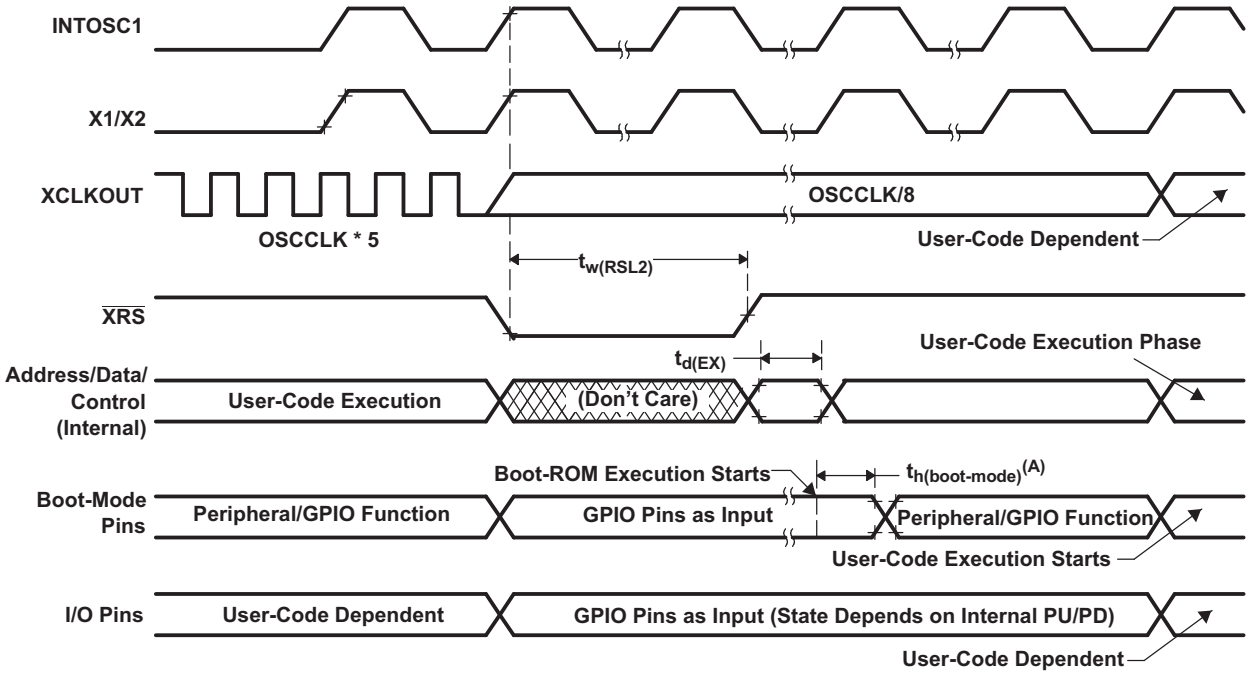
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{XRS}$ driven by device			600		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog			$512t_{c(OSCCLK)}$		cycles

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(EX)}$	Delay time, address/data valid after $\overline{XRS}$ high			$32t_{c(OSCCLK)}$		cycles
$t_{INTOSCST}$	Start up time, internal zero-pin oscillator			3		µs
t_{OSCST} (1)	On-chip crystal, oscillator start-up time		1	10		ms

(1) Dependent on crystal/resonator and board design.



A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 6-7. Warm Reset

Figure 6-8 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and SYSCLKOUT = OSCCLK x 2. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, SYSCLKOUT = OSCCLK/2. After the PLL lock-up is complete,SYSCLKOUT reflects the new operating frequency, OSCCLK x 4.

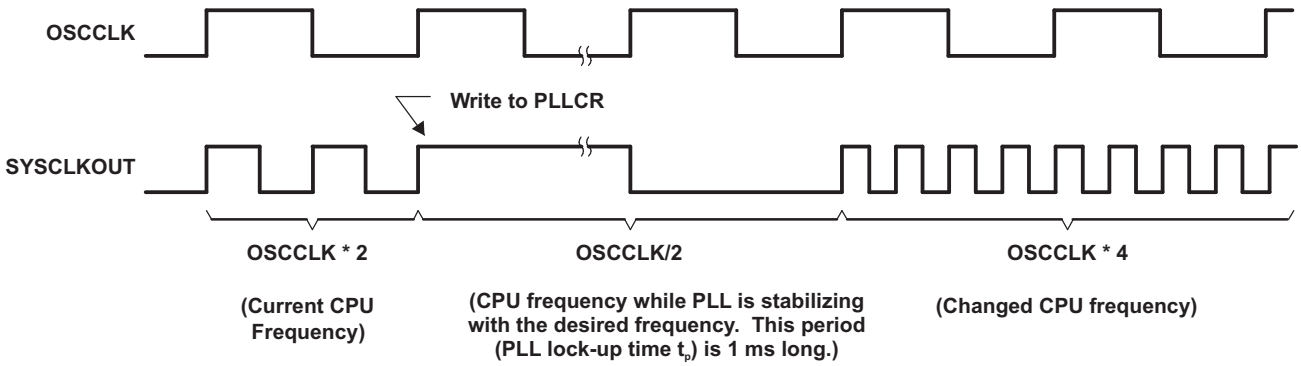


Figure 6-8. Example of Effect of Writing Into PLLCR Register

6.9 General-Purpose Input/Output (GPIO)

6.9.1 GPIO - Output Timing

Table 6-12. General-Purpose Output Switching Characteristics

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		8	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		8	ns
t_{fGPO}	Toggling frequency			20	MHz

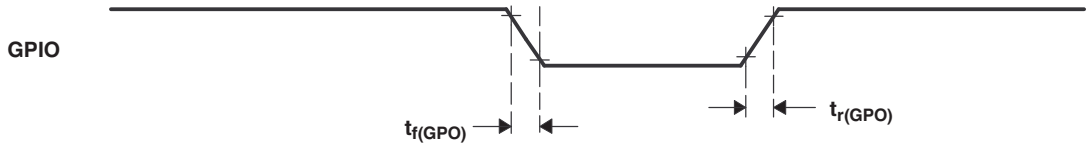
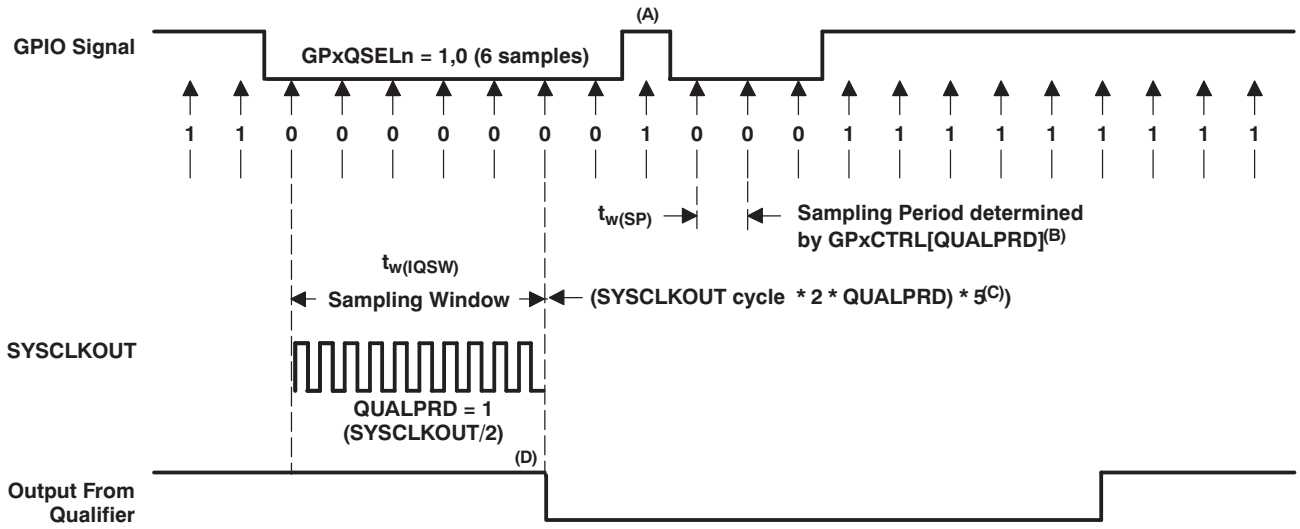


Figure 6-9. General-Purpose Output Timing

6.9.2 GPIO - Input Timing



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (i.e., at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).

B. The qualification period selected via the GPxCTRL register applies to groups of 8 GPIO pins.

C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.

D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 x QUALPRD x 2) SYSCLKOUT cycles. This would ensure 5 sampling periods for detection to occur. Since external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 6-10. Sampling Mode

Table 6-13. General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SCO)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SCO)}$ * QUALPRD		cycles

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Table 6-13. General-Purpose Input Timing Requirements (continued)

			MIN	MAX	UNIT
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) - 1)		cycles
$t_{w(GPI)}$(2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SCO)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SCO)}$		cycles

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.9.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = SYSCLKOUT/(2 * QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLKOUT, if QUALPRD = 0

Sampling period = SYSCLKOUT cycle x 2 x QUALPRD, if QUALPRD ≠ 0

In the above equations, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle, if QUALPRD = 0

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 2, if QUALPRD = 0

Case 2:

Qualification using 6 samples

Sampling window width = (SYSCLKOUT cycle x 2 x QUALPRD) x 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) x 5, if QUALPRD = 0

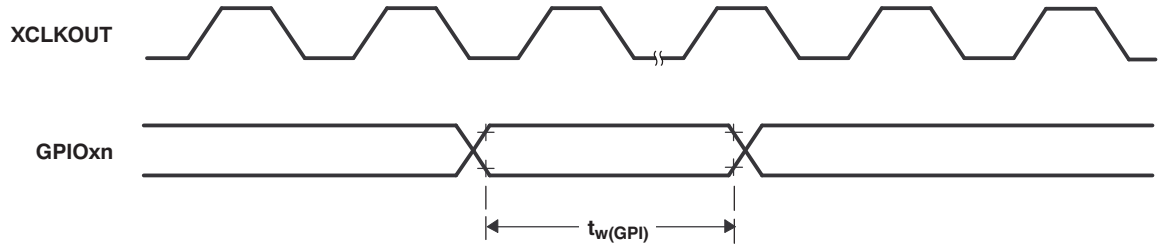


Figure 6-11. General-Purpose Input Timing

6.9.4 Low-Power Mode Wakeup Timing

Table 6-14 shows the timing requirements, Table 6-15 shows the switching characteristics, and Figure 6-12 shows the timing diagram for IDLE mode.

Table 6-14. IDLE Mode Timing Requirements(1)

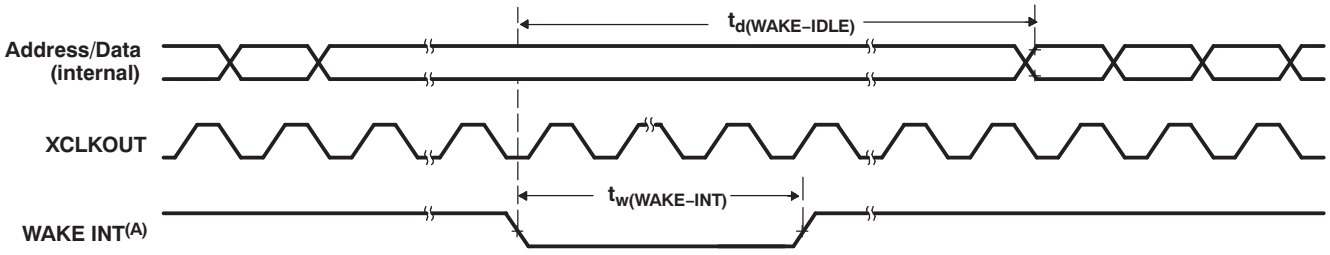
			MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SCO)}$			cycles
		With input qualifier	$5t_{c(SCO)} + t_{w(IQSW)}$			

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-15. IDLE Mode Switching Characteristics(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume (2)					
	• Wake-up from Flash – Flash module in active state	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from Flash – Flash module in sleep state	Without input qualifier			$1050t_{c(SCO)}$	cycles
		With input qualifier			$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake-up from SARAM	Without input qualifier			$20t_{c(SCO)}$	cycles
		With input qualifier			$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Table 6-13.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up) signal involves additional latency.



A. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$ or $\overline{\text{XRS}}$.

Figure 6-12. IDLE Entry and Exit Timing

Table 6-16. STANDBY Mode Timing Requirements

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification	$3t_{c(OSCCLK)}$			cycles
		With input qualification(1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$			

(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

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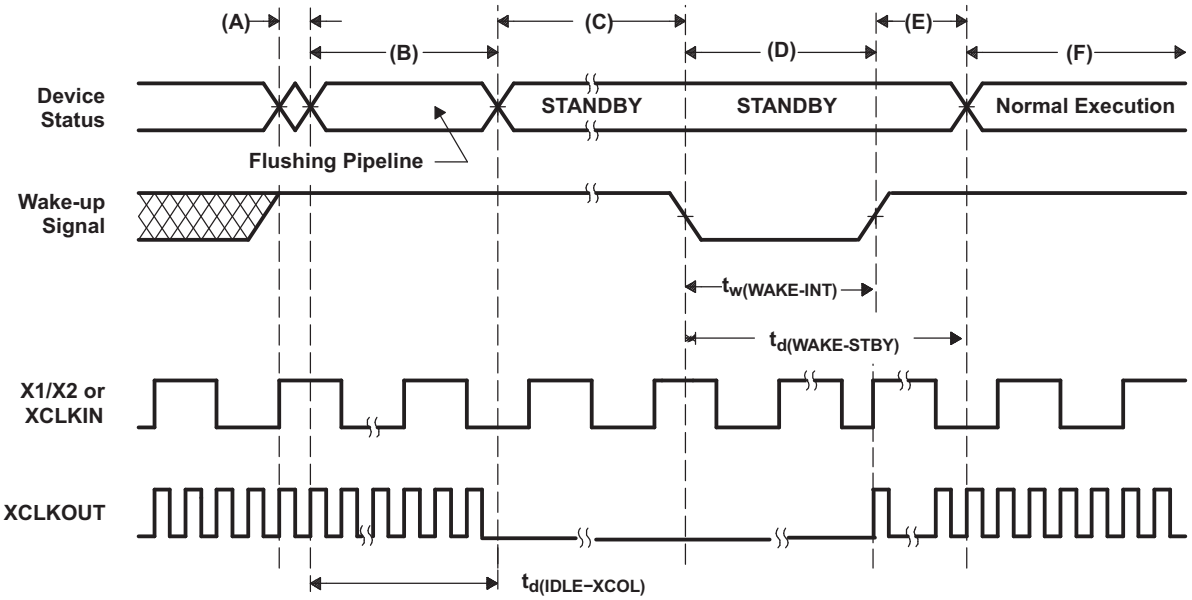
Table 6-17. STANDBY Mode Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low		$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)					cycles
	• Wake up from flash – Flash module in active state	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier			$1125t_{c(SCO)}$	cycles
		With input qualifier			$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from SARAM	Without input qualifier			$100t_{c(SCO)}$	cycles
		With input qualifier			$100t_{c(SCO)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. execution of an ISR (triggered by the wake up signal) involves additional latency.



A. IDLE instruction is executed to put the device into STANDBY mode.

B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for approximately 32 cycles before being turned off. This 32-cycle delay enables the CPU pipe and any other pending operations to flush properly.

C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode.

D. The external wake-up signal is driven active.

E. After a latency period, the STANDBY mode is exited.

F. Normal execution resumes. The device will respond to the interrupt (if enabled).

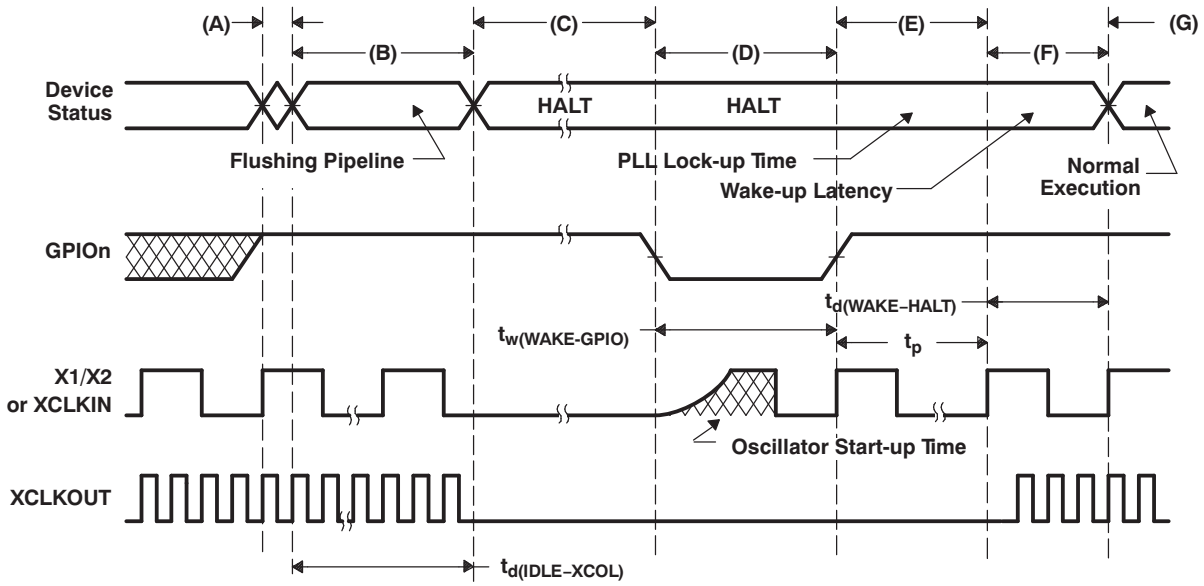
Figure 6-13. STANDBY Entry and Exit Timing Diagram

Table 6-18. HALT Mode Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$			cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wakeup signal	$t_{oscst} + 8t_{c(OSCCLK)}$			cycles

Table 6-19. HALT Mode Switching Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low	$32t_{c(SCO)}$		$45t_{c(SCO)}$	cycles
t_p	PLL lock-up time			1	ms
$t_{d(WAKE-HALT)}$	Delay time, PLL lock to program execution resume • Wake up from flash – Flash module in sleep state			$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM			$35t_{c(SCO)}$	cycles



A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for approximately 32 cycles before the oscillator is turned off and the CLKIN to the core is stopped. This 32-cycle delay enables the CPU pipe and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power.

D. When the GPIOn pin is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Since the falling edge of the GPIO pin asynchronously begins the wakeup procedure, care should be taken to maintain a low noise environment prior to entering and during HALT mode.

E. When GPIOn is deactivated, it initiates the PLL lock sequence, which takes 131,072 OSCCLK (X1/X2 or X1 or XCLKIN) cycles.

F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.

G. Normal operation resumes.

Figure 6-14. HALT Wake-Up Using GPIOn

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6.10 Enhanced Control Peripherals

6.10.1 Enhanced Pulse Width Modulator (ePWM) Timing

PWM refers to PWM outputs on ePWM1-6. Table 6-20 shows the PWM timing requirements and Table 6-21, switching characteristics.

Table 6-20. ePWM Timing Requirements(1)

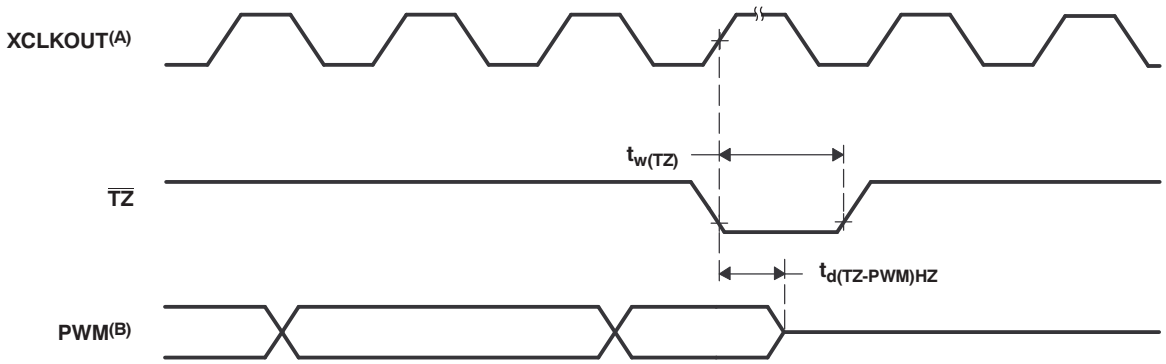
		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(SYCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-21. ePWM Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		20		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

6.10.2 Trip-Zone Input Timing



A. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 6-15. PWM Hi-Z Characteristics

Table 6-22. Trip-Zone input Timing Requirements(1)

			MIN	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZx}$ input low	Asynchronous	$1t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-23 shows the high-resolution PWM switching characteristics.

Table 6-23. High Resolution PWM Characteristics at SYSCLKOUT = (60 - 100 MHz)

	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(1) (2)		150	310	ps

(1) Maximum MEP step size is based on worst-case process, maximum temperature and maximum voltage. MEP step size will increase with low voltage and high temperature and decrease with voltage and cold temperature.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.
(2) Between 40 to 50 MHz SYSCLKOUT under worst case process, voltage, and temperature (maximum voltage and minimum temperature) conditions, the MEP step delay may decrease to a point such that the maximum of 254 MEP steps may not cover 1 full SYSCLKOUT cycle. In other words, high-resolution edge control will not be available for the full range of a SYSCLKOUT cycle. If running SFO calibration software, the SFO function will return an error code of “2” when this occurs. See the device-specific HRPWM Reference Guide for more information on this error condition.

Table 6-24 shows the eCAP timing requirement and Table 6-25 shows the eCAP switching characteristics.

Table 6-24. Enhanced Capture (eCAP) Timing Requirement(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

Table 6-25. eCAP Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low		20		ns

6.10.3 External Interrupt Timing

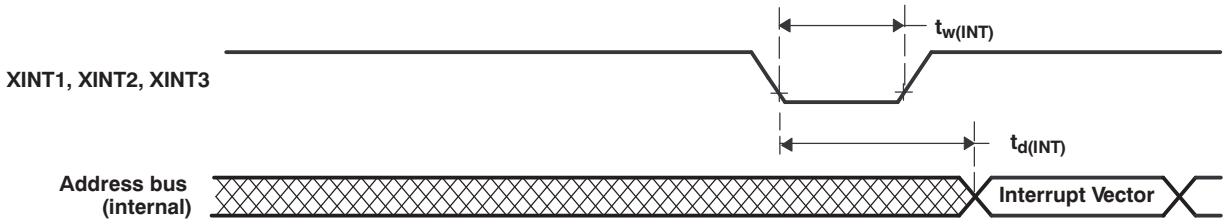


Figure 6-16. External Interrupt Timing

Table 6-26. External Interrupt Timing Requirements(1)

		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(INT)}$(2)	Pulse duration, INT input low/high	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.
(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

Table 6-27. External Interrupt Switching Characteristics(1)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{w(IQSW)} + 12t_{c(SCO)}$	cycles

(1) For an explanation of the input qualifier parameters, see Table 6-13.

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6.10.4 I2C Electrical Specification and Timing

Table 6-28. I2C Timing

		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately		400	kHz
v_{il}	Low level input voltage			0.3 V_{DDIO}	V
V_{ih}	High level input voltage		0.7 V_{DDIO}		V
V_{hys}	Input hysteresis		0.05 V_{DDIO}		V
V_{ol}	Low level output voltage	3 mA sink current	0	0.4	V
t_{LOW}	Low period of SCL clock	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately	1.3		µs
t_{HIGH}	High period of SCL clock	I2C clock module frequency is between 7 MHz and 12 MHz and I2C prescaler and clock divider registers are configured appropriately	0.6		µs
I_I	Input current with an input voltage between 0.1 V_{DDIO} and 0.9 V_{DDIO} MAX		-10	10	µA

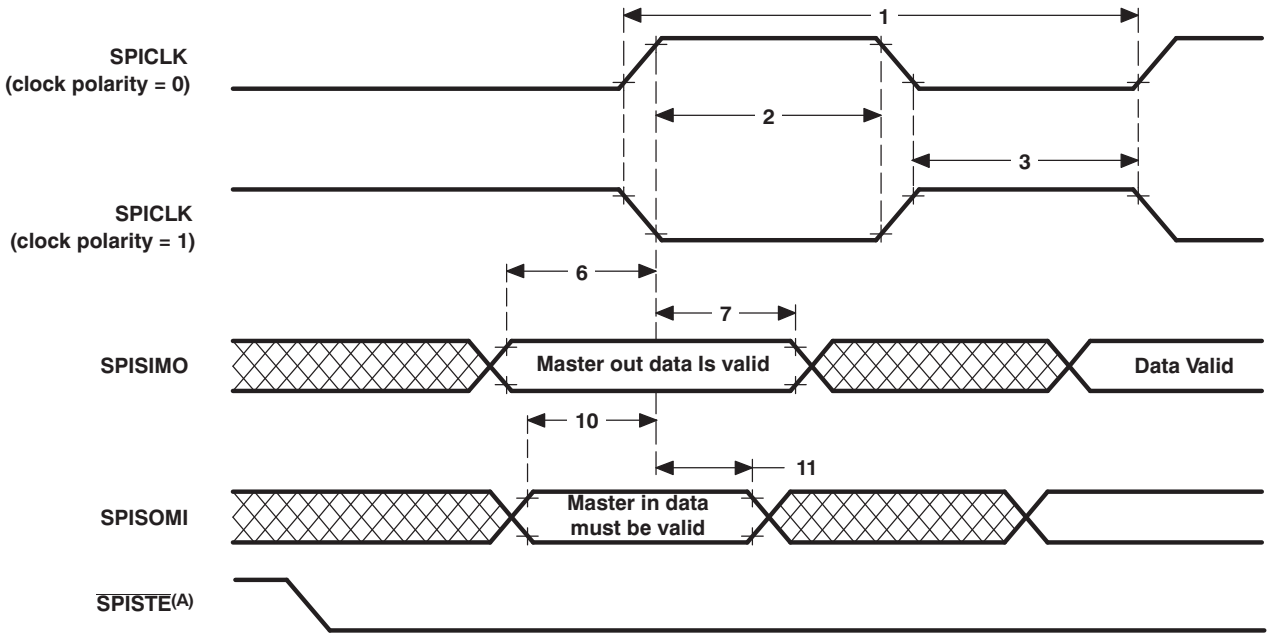
6.10.5 Serial Peripheral Interface (SPI) Master Mode Timing

Table 6-29 lists the master mode timing (clock phase = 0) and Table 6-30 lists the timing (clock phase = 1). Figure 6-17 and Figure 6-18 show the timing waveforms.

Table 6-29. SPI Master Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$ - 10	$0.5t_{c(SPC)}M$ - $0.5t_{c(LCO)}$	ns
	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ - 10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$ - 10	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$	
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}$ - 10	$0.5_{tc(SPC)M}$	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$-10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5_{tc(SPC)M}$ - 10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$- 10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	
4	$t_{d(SPCH-SIMO)M}$	Delay time, SPICLK high to SPISIMO valid (clock polarity = 0)		10		10	ns
	$t_{d(SPCL-SIMO)M}$	Delay time, SPICLK low to SPISIMO valid (clock polarity = 1)		10		10	
5	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$ -10		
	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$ -10		
8	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 0)	35		35		ns
	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 1)	35		35		ns
9	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.25t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$- $0.5t_{c(LCO)}$- 10		
	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.25t_{c(SPC)M}$ - 10		$0.5t_{c(SPC)M}$- $0.5t_{c(LCO)}$- 10		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MAX, slave mode receive 10-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).



A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and nonFIFO modes.

Figure 6-17. SPI Master Mode External Timing (Clock Phase = 0)

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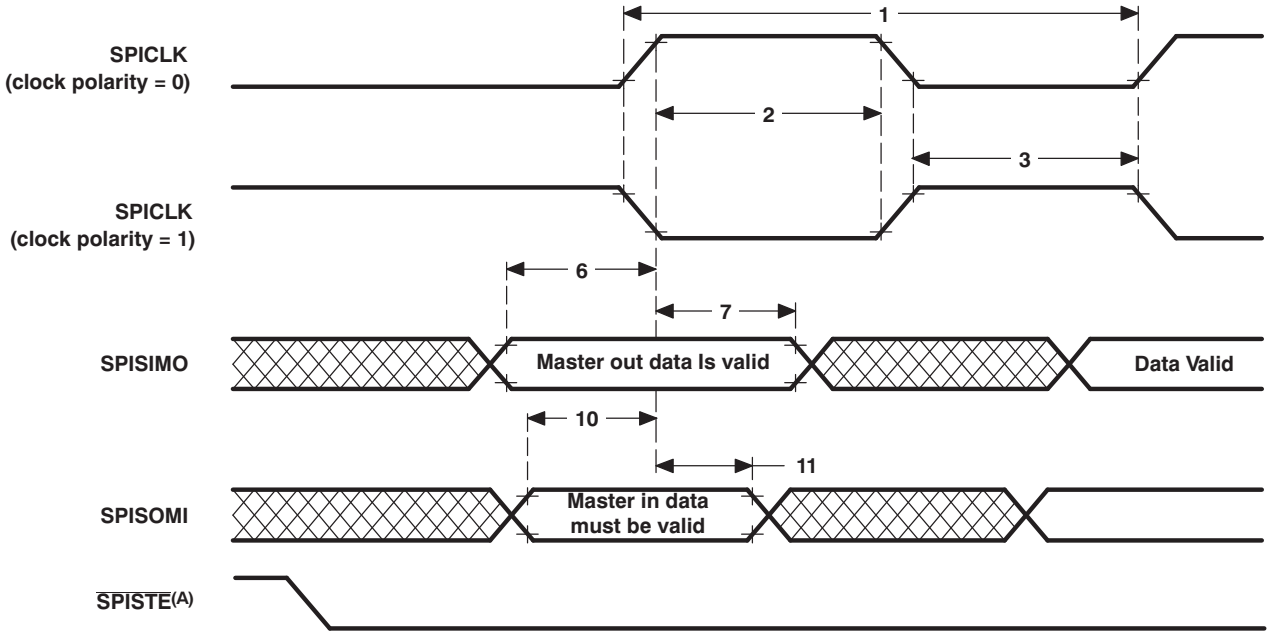
Table 6-30. SPI Master Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)(5)

NO.			SPI WHEN (SPIBRR + 1) IS EVEN OR SPIBRR = 0 OR 2		SPI WHEN (SPIBRR + 1) IS ODD AND SPIBRR > 3		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LCO)}$	$128t_{c(LCO)}$	$5t_{c(LCO)}$	$127t_{c(LCO)}$	ns
2	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c\ (LCO)}$-10	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO)}$	ns
	$t_{w(SPCL))M}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ - $0.5t_{c\ (LCO)}$-10	$0.5t_{c(SPC)M}$ - $0.5t_{c(LCO}$	ns
3	$t_{w(SPCL)M}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$ - 10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	ns
	$t_{w(SPCH)M}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10	$0.5t_{c(SPC)M}$	$0.5_{tc(SPC)M}$ + $0.5t_{c(LCO)}$ -10	$0.5t_{c(SPC)M}$ + $0.5t_{c(LCO)}$	ns
6	$t_{su(SIMO-SPCH)M}$	Setup time, SPISIMO data valid before SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ - 10		ns
	$t_{su(SIMO-SPCL)M}$	Setup time, SPISIMO data valid before SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ - 10		ns
7	$t_{v(SPCH-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ - 10		ns
	$t_{v(SPCL-SIMO)M}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ -10		ns
10	$t_{su(SOMI-SPCH)M}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	35		35		ns
	$t_{su(SOMI-SPCL)M}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1)	35		35		ns
11	$t_{v(SPCH-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 0)	$0.25t_{c(SPC)M}$ -10		$0.5t_{c(SPC)M}$ -10		ns
	$t_{v(SPCL-SOMI)M}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 1)	$0.25_{tc(SPC)M}$ -10		$0.5_{tc(SPC)M}$ -10		ns

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 20 MHz MAX, master mode receive 10 MHz MAX
Slave mode transmit 10 MHz MAX, slave mode receive 10 MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



A. In the master mode, $\overline{\text{SPISTE}}$ goes active $0.5t_{c(SPC)}$ (minimum) before valid SPI clock edge. On the trailing end of the word, the $\overline{\text{SPISTE}}$ will go inactive $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit, except that $\overline{\text{SPISTE}}$ stays active between back-to-back transmit words in both FIFO and nonFIFO modes.

Figure 6-18. SPI Master Mode External Timing (Clock Phase = 1)

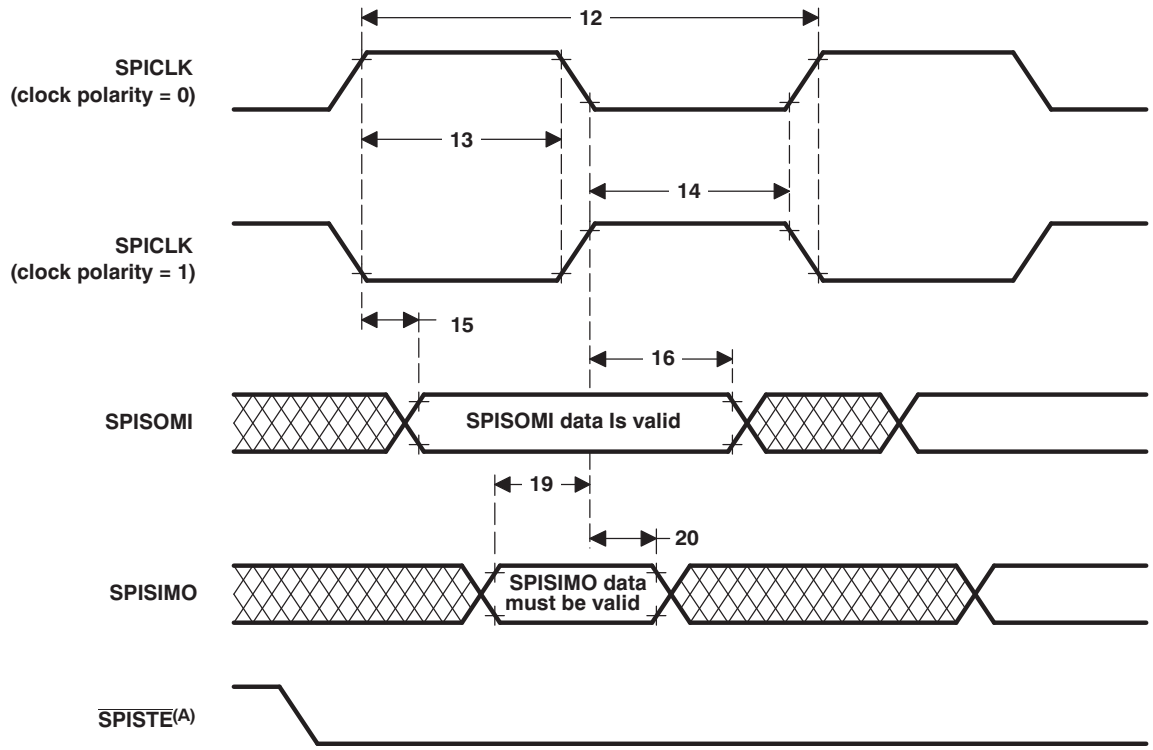
6.10.6 SPI Slave Mode Timing

Table 6-31 lists the slave mode external timing (clock phase = 0) and Table 6-32 (clock phase = 1). Figure 6-19 and Figure 6-20 show the timing waveforms.

Table 6-31. SPI Slave Mode External Timing (Clock Phase = 0)(1)(2)(3)(4)(5)

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
15	$t_{d(SPCH-SOMI)S}$	Delay time, SPICLK high to SPISOMI valid (clock polarity = 0)		35	ns
	$t_{d(SPCL-SOMI)S}$	Delay time, SPICLK low to SPISOMI valid (clock polarity = 1)		35	ns
16	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.75t_{c(SPC)S}$		ns
19	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 0)	35		ns
	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 1)	35		ns
20	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S-10}$		ns
	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S-10}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).



A. In the slave mode, the $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ (minimum) before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-19. SPI Slave Mode External Timing (Clock Phase = 0)

Table 6-32. SPI Slave Mode External Timing (Clock Phase = 1)(1)(2)(3)(4)

NO.			MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$8t_{c(LCO)}$		ns
13	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
14	$t_{w(SPCL)S}$	Pulse duration, SPICLK low (clock polarity = 0)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
	$t_{w(SPCH)S}$	Pulse duration, SPICLK high (clock polarity = 1)	$0.5t_{c(SPC)S}$ - 10	$0.5t_{c(SPC)S}$	ns
17	$t_{su(SOMI-SPCH)S}$	Setup time, SPISOMI before SPICLK high (clock polarity = 0)	$0.125t_{c(SPC)S}$		ns
	$t_{su(SOMI-SPCL)S}$	Setup time, SPISOMI before SPICLK low (clock polarity = 1	$0.125t_{c(SPC)S}$		ns
18	$t_{v(SPCH-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK low (clock polarity = 0)	$0.75t_{c(SPC)S}$		ns
	$t_{v(SPCL-SOMI)S}$	Valid time, SPISOMI data valid after SPICLK high (clock polarity = 1)	$0.75t_{c(SPC)S}$		ns
21	$t_{su(SIMO-SPCH)S}$	Setup time, SPISIMO before SPICLK high (clock polarity = 0)	35		ns
	$t_{su(SIMO-SPCL)S}$	Setup time, SPISIMO before SPICLK low (clock polarity = 1)	35		ns
22	$t_{v(SPCH-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK high (clock polarity = 0)	$0.5t_{c(SPC)S-10}$		ns
	$t_{v(SPCL-SIMO)S}$	Valid time, SPISIMO data valid after SPICLK low (clock polarity = 1)	$0.5t_{c(SPC)S-10}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 20-MHz MAX, master mode receive 10-MHz MAX
Slave mode transmit 10-MHz MAX, slave mode receive 10-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

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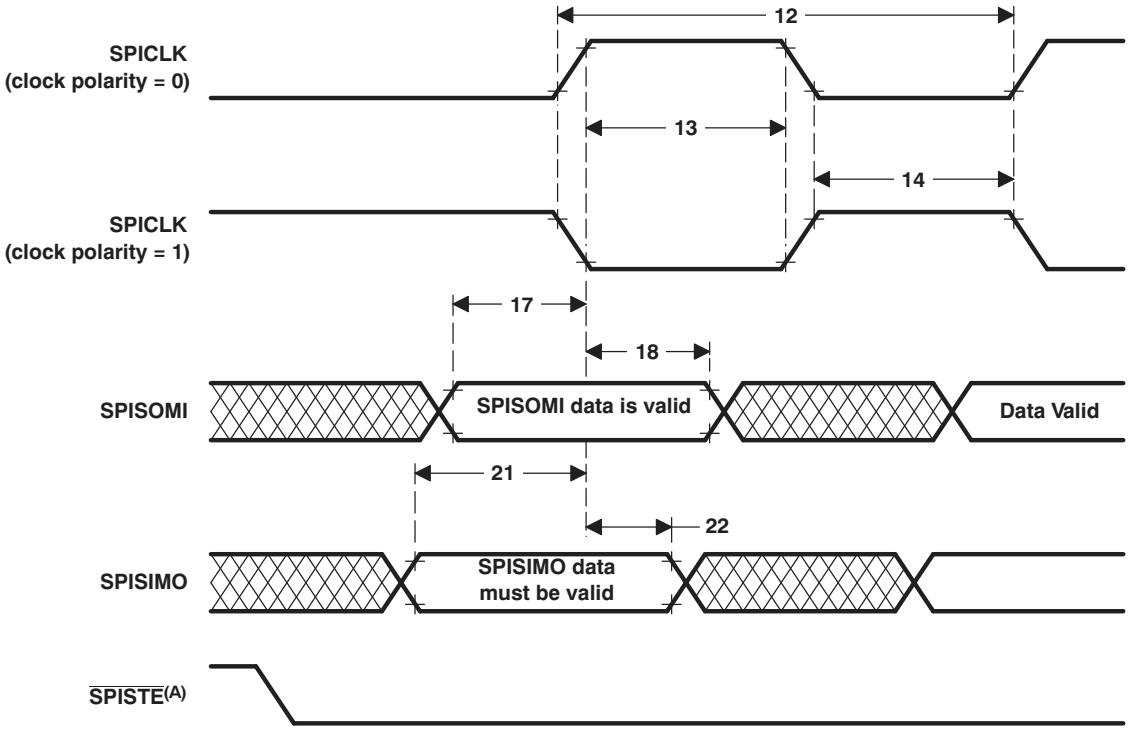

A. In the slave mode, the $\overline{\text{SPISTE}}$ signal should be asserted low at least $0.5t_{c(SPC)}$ before the valid SPI clock edge and remain low for at least $0.5t_{c(SPC)}$ after the receiving edge (SPICLK) of the last data bit.

Figure 6-20. SPI Slave Mode External Timing (Clock Phase = 1)

6.10.6.1 On-chip Comparator/DAC

Table 6-33. Electrical Characteristics of the Comparator/DAC

CHARACTERISTIC	MIN	TYP	MAX	UNITS
Comparator				
Comparator Input Range		$V_{SSA} – V_{DDA}$		V
Comparator response time to PWM Trip Zone (Async)		30		ns
Input Offset		±5		mV
Input Hysteresis		35		mV
DAC				
DAC Output Range		$V_{SSA} – V_{DDA}$		V
DAC resolution		10		bits
DAC settling time		2		us
DAC Gain		–1.5		%
DAC Offset		10		mV
No Missing Codes		Yes		
INL		±3		LSB

6.10.7 On-Chip Analog-to-Digital Converter

Table 6-34. ADC Electrical Characteristics (over recommended operating conditions)

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution		12			Bits
ADC clock	40-MHz device				MHz
	60-MHz device	0.001		60	MHz
ACCURACY					
INL (Integral nonlinearity)	60-MHz clock (4.62 MSPS)		±2		LSB
DNL (Differential nonlinearity)			±1		LSB
Offset error (1)			±10		LSB
Overall gain error with internal reference			±10		LSB
Overall gain error with external reference			±10		LSB
Channel-to-channel offset variation			±4		LSB
Channel-to-channel gain variation			±4		LSB
ANALOG INPUT					
Analog input voltage (2) with internal reference		0		3.3	V
Analog input voltage (2) with external reference		V_{REFLO}		V_{REFHI}	V
V_{REFLO} input voltage			(3)		V
V_{REFHI} input voltage (with $V_{REFLO} = V_{SSA}$)		1.98		V_{DDA}	V
Temperature coefficient			50		PPM/°C
Input capacitance			10		pF
Input leakage current			±5		µA

(1) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and V_{REFHI} - V_{REFLO} for external reference.
(2) Voltages above V_{DDA} + 0.3 V or below V_{SS} - 0.3 V applied to an analog input pin may temporarily affect the conversion of another pin. To avoid this, the analog inputs should be kept within these limits.
(3) VREFLO is always connected to V_{SSA}.

6.10.7.1 ADC Power-Up Control Bit Timing

Table 6-35. ADC Power-Up Delays

PARAMETER(1)		MIN	TYP	MAX	UNIT
$t_{d(PWD)}$	Delay time for the ADC to be stable after power up			1	ms

(1) Timings maintain compatibility to the ADC module. The 2802x ADC supports driving all 3 bits at the same time $t_{d(PWD)}$ ms before first conversion.

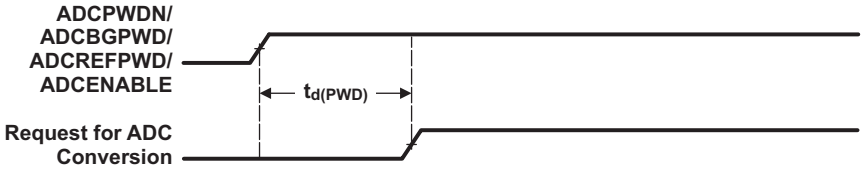

Figure 6-21. ADC Conversion Timing

ADVANCE INFORMATION

6.10.7.1.1 ADC Sequential and Simultaneous Timings

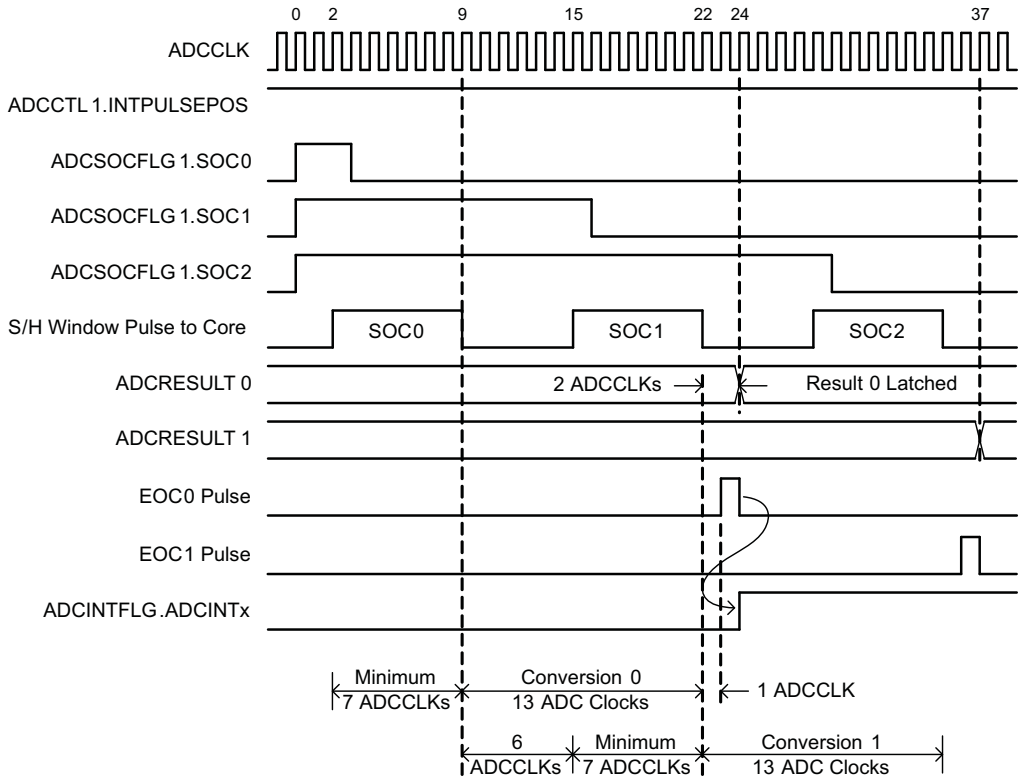

Figure 6-22. Timing Example For Sequential Mode / Late Interrupt Pulse

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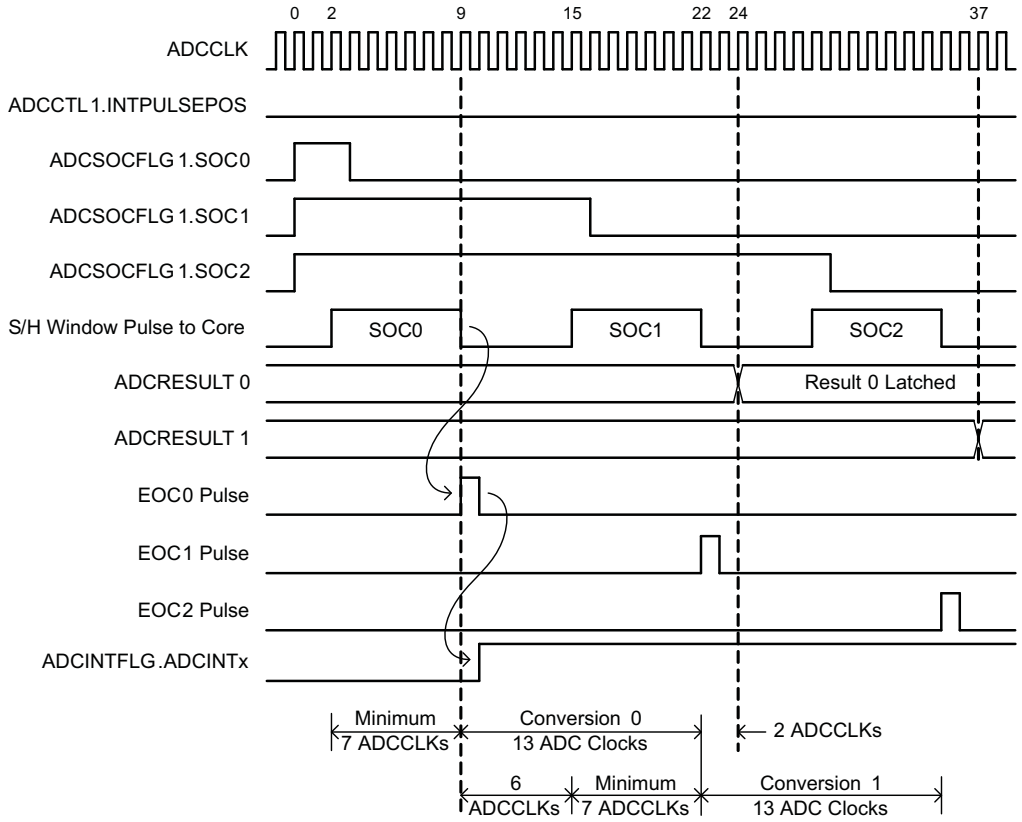

Figure 6-23. Timing Example For Sequential Mode / Early Interrupt Pulse

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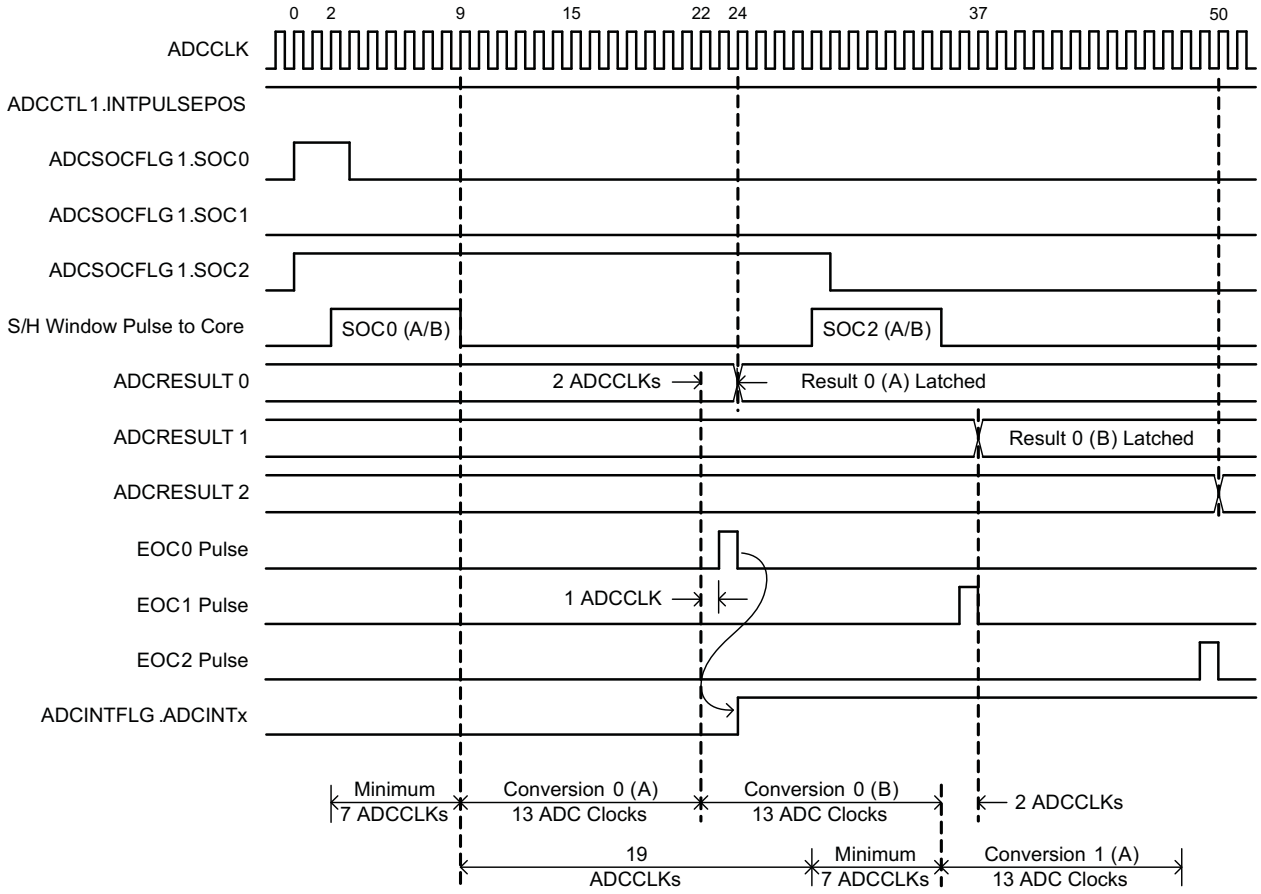


Figure 6-24. Timing Example For Simultaneous Mode / Late Interrupt Pulse

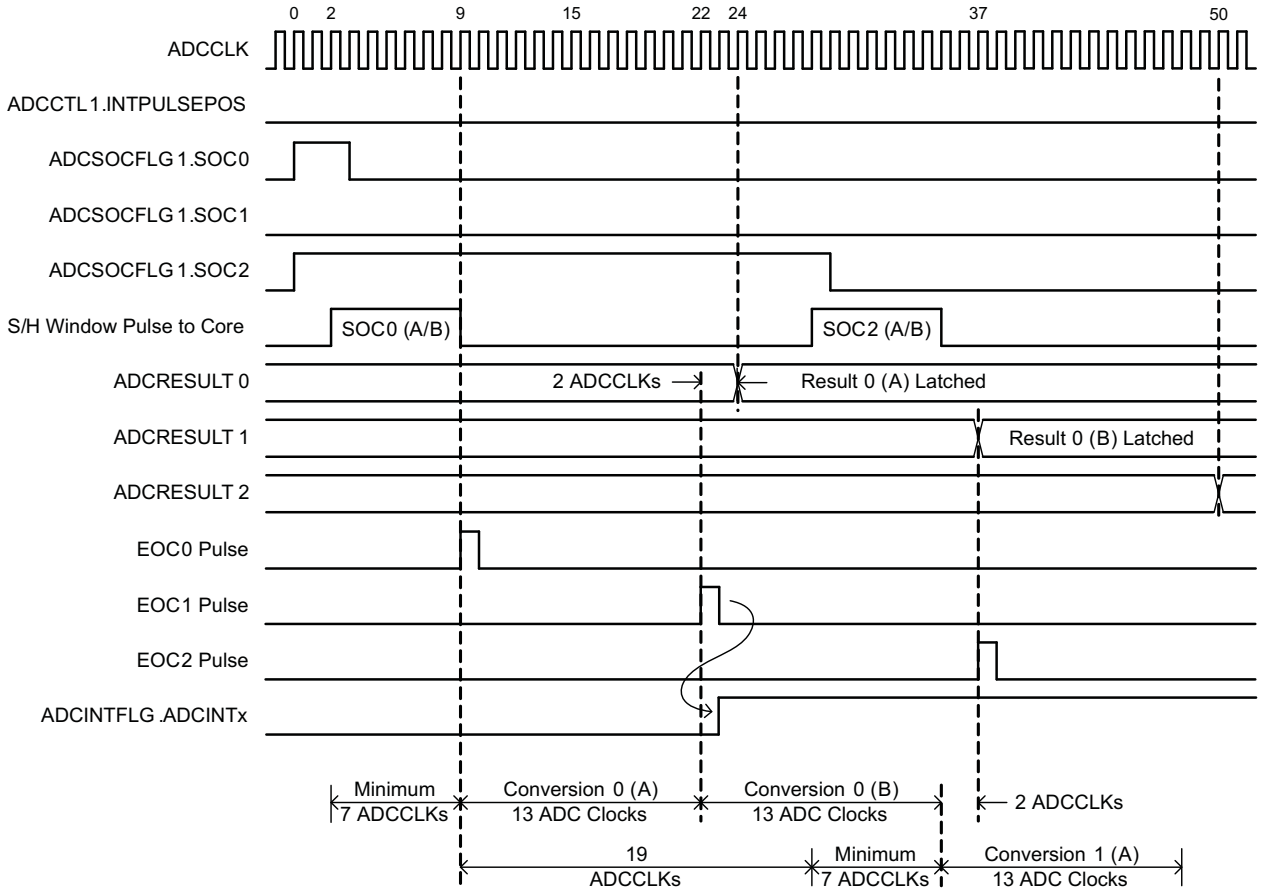


Figure 6-25. Timing Example For Simultaneous Mode/Early Interrupt Pulse

6.11 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero through full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

ADVANCE INFORMATION

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, $N = \frac{(SINAD - 1.76)}{6.02}$ it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

7 Mechanicals

The mechanical package diagram(s) that follow the tables reflect the most current released mechanical data available for the designated device(s).

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Additions, Deletions and Modifications

LOCATION	DESCRIPTION
Section 1.1	Added enhanced control peripherals to features list
Table 2-2	Modified the descriptions of the X1, X2, and $\overline{\text{XRS}}$ pins
Section 3.2	Modified the memory maps
Section 3.3.4	Modified the Real-time JTAG and Analysis section
Section 3.3.19	Modified the Control Peripherals section
Table 3-7	Modified the peripheral frame 2 registers table
Figure 3-6	Moved and modified the VREG + POR + BOR + Reset Signal Connectivity figure
Figure 3-7	Modified the clock and reset domains figure
Table 3-9	Modified the device emulation registers table
Figure 3-4	Modified the external and PIE interrupt sources figure
Figure 3-8	Modified the clock tree figure
Table 3-14	Modified the PLLCR bit descriptions table and changed the title to PLL Settings
Section 3.7.2	Modified the section on POR and BOR circuit
Section 3.8.4	Modified the Loss of Input Clock section and added to the title
Figure 3-11	Changed the title of the Clock Fail figure to NMI-watchdog
Section 3.9	Modified the Low-power Modes Block section
Table 4-1	Added a column to show EALLOW protection to register tables
Table 3-7	Modified the peripheral frame 2 registers table
Section 4.8	Modified the GPIO MUX section
Section 6.1	Modified the Absolute Maximum Ratings table
Section 6.4	Added the Current Consumption section and all the sections following it

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TMX320F28023DAA	ACTIVE	TSSOP	DA	38	1	TBD	Call TI	Call TI
TMX320F28027PTA	ACTIVE	LQFP	PT	48	1	TBD	Call TI	Call TI

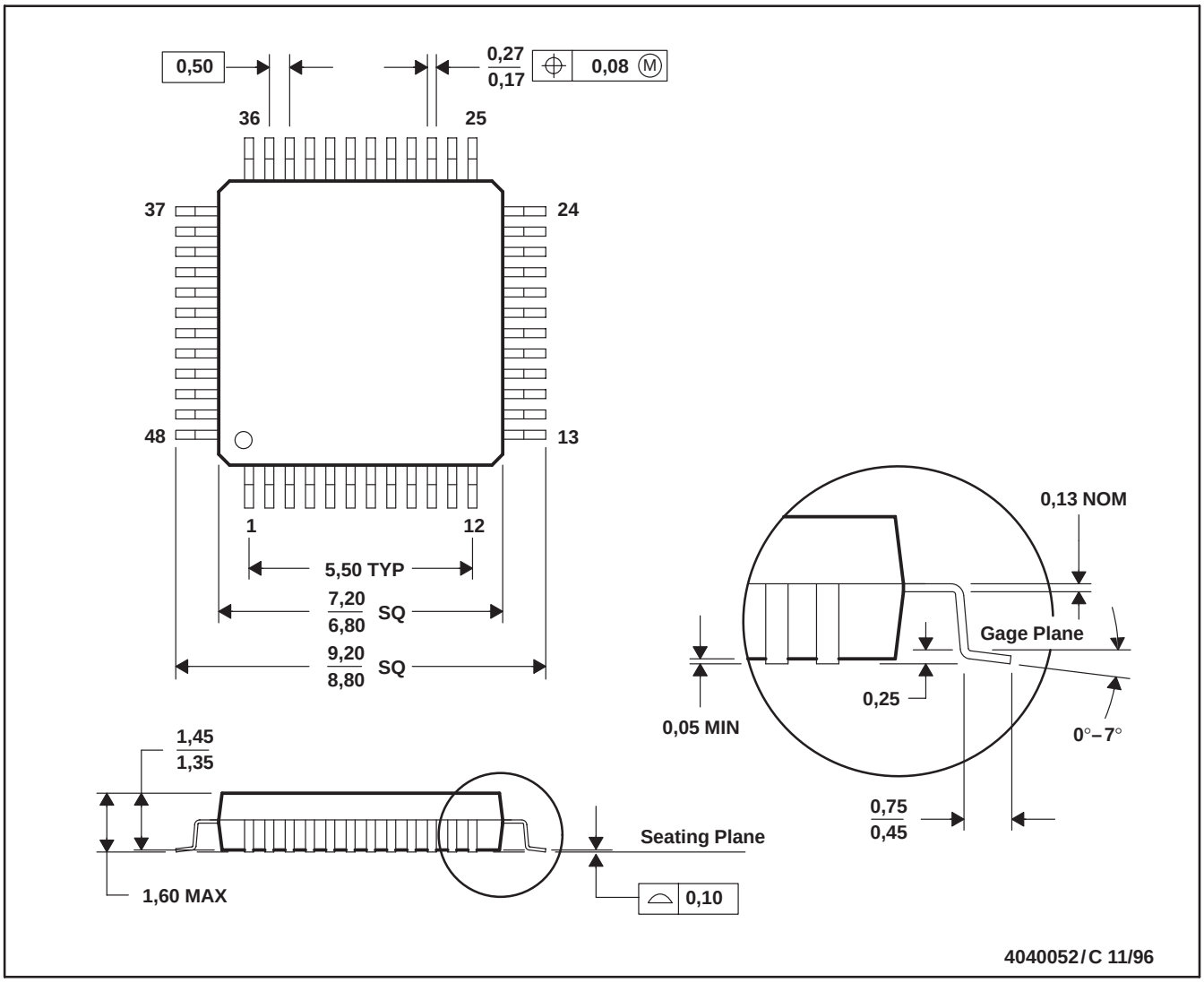
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

MTQF003A – OCTOBER 1994 – REVISED DECEMBER 1996

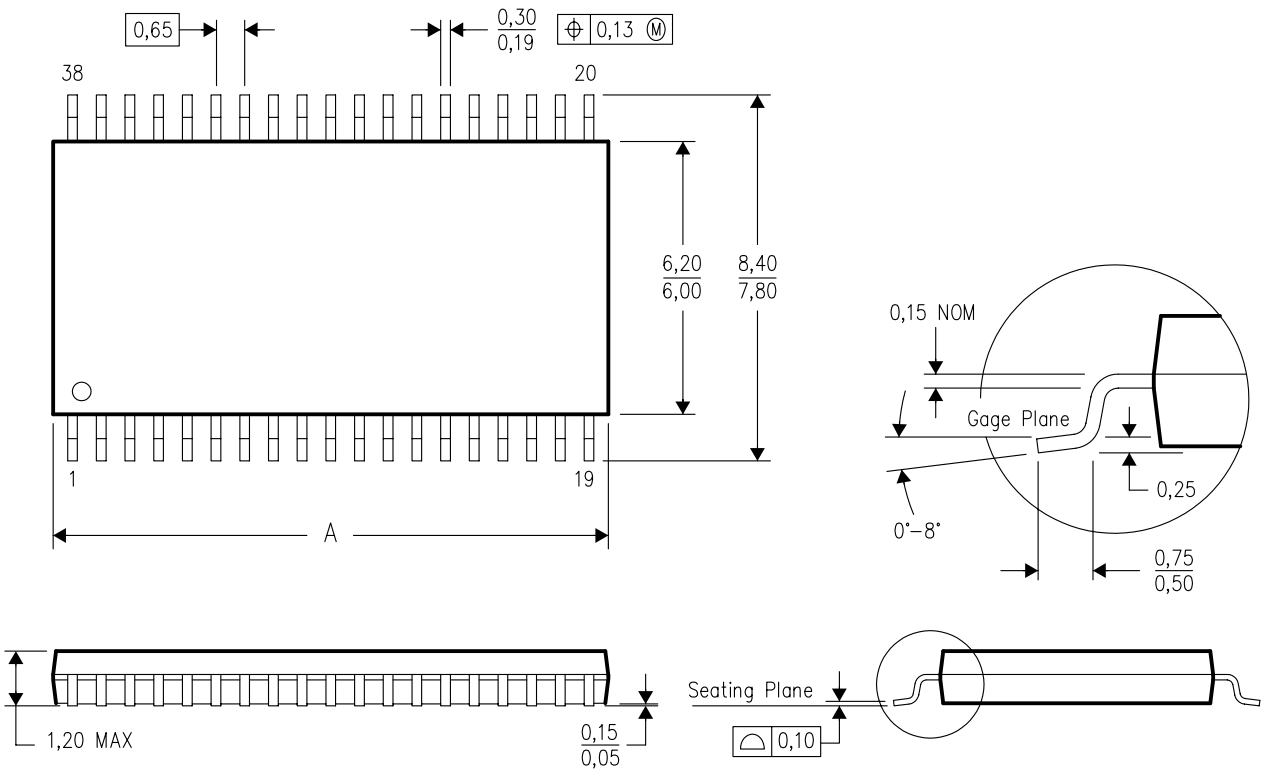
PT (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026
D. This may also be a thermally enhanced plastic package with leads conected to the die pads.

DA (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

38 PIN SHOWN



DIM \ PINS **	30	32	38
A MAX	11,10	11,10	12,60
A MIN	10,90	10,90	12,40

4040066/E 11/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–153

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