High Power/High Efficiency PoE Interface and DC/DC Controller

FEATURES

- **Powers up to 30 W (input) PDs**
- **DC/DC Control Optimized for Isolated Converters**
- **Supports High-efficiency Topologies**
- **Complete PoE Interface**
- **Enhanced Classification per IEEE 802.3at (Draft) with Status Flag**
- **Adapter ORing Support**
- **Programmable Frequency with Synchronization**
- **Robust 100 V, 0.5 Ω Hotswap MOSFET**
- **–40°C to 125°C Junction Temperature Range**
- **Industry Standard PowerPAD™ TSSOP-20**

APPLICATIONS

- **IEEE 802.3at (Draft) Compliant Devices**
- **Video and VoIP Telephones**
- **RFID Readers**
- **Multiband Access Points**
- **Security Cameras**

DESCRIPTION

The TPS23754/6 is a combined Power over Ethernet (PoE) powered device (PD) interface and current-mode dc/dc controller optimized specifically for isolated converters. The PoE interface supports the IEEE 802.3at (draft) standard.

The TPS23754/6 supports a number of input voltage ORing options including highest voltage, external adapter preference, and PoE preference. These features allow the designer to determine which power source will carry the load under all conditions.

The PoE interface features the new extended hardware classification necessary for compatibility with high-power midspan power sourcing equipment (PSE) per IEEE 802.3at (draft). The detection signature pin can also be used to force power from the PoE source off. Classification can be programmed to any of the defined types with a single resistor.

The dc/dc controller features two complementary gate drivers with programmable dead time. This simplifies design of active-clamp forward converters or optimized gate drive for highly-efficient flyback topologies. The second gate driver may be disabled if desired for single MOSFET topologies. The controller also features internal softstart, bootstrap startup source, current-mode compensation, 78% maximum duty cycle. A programmable and synchronizable oscillator allows design optimization for efficiency and eases use of the controller to upgrade existing power supply designs. Accurate programmable blanking, with a default period, simplifies the usual current-sense filter design trade-offs.

The TPS23754 has a 15 V converter startup while the TPS23756 has a 9 V converter startup. The TPS23754-1 replaces the PPD pin with a no-connect for increased pin spacing.

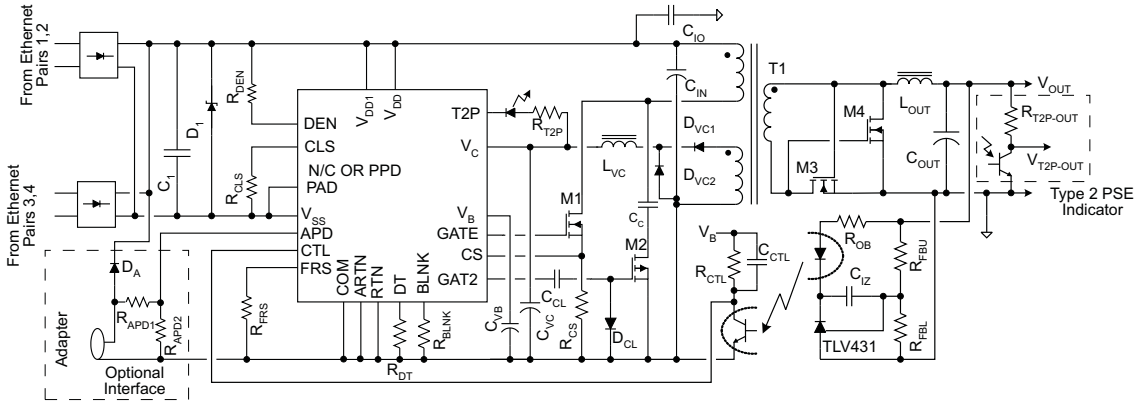

Figure 1. High Efficiency Converter Using TPS23754

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PowerPAD is a trademark of Texas Instruments.

This device contains circuits to protect its inputs and outputs against damage due to high static voltages or electrostatic fields. These circuits have been qualified to protect this device against electrostatic discharges (ESD) of up to 2 kV according to MIL-STD-883C, Method 3015; however, it is advised that precautions be taken to avoid application of any voltage higher than maximum-rated voltages to these high-impedance circuits. During storage or handling the device leads should be shorted together or the device should be placed in conductive foam. In a circuit, unused inputs should always be connected to an appropriate voltage level, preferably either the proper supply or ground. Specific guidelines for handling devices of this type are contained in the publication Guidelines for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices and Assemblies available from Texas Instruments.

PRODUCT INFORMATION(1)

	STATUS	DUTY CYCLE	POE UVLO ON / HYST.	CONVERTER UVLO ON / HYST.	FEATURE	PACKAGE	MARKING
TPS23754PWP	Active	0–78%	35/4.5	15 / 6.5	PPD	TSSOP-20 PowerPAD™	TPS23754
TPS23754PWP-1	Active	0–78%	35/4.5	15 / 6.5	–	TSSOP-20 PowerPAD™	23754-1
TPS23756PWP	Active	0–78%	35/4.5	9 / 3.5	PPD	TSSOP-20 PowerPAD™	TPS23756

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1) (2)

Voltage with respect to V_{SS} unless otherwise noted.

	VALUE	UNIT
Input voltage range, ARTN(2), COM(2), DEN, PPD, RTN(3), V_{DD}, V_{DD1}	–0.3 to 100	V
Input voltage range CLS(4)	-0.3 to 6.5	V
Input voltage range [APD, BLNK(4), CTL, DT(4), FRS(4), VB(4)] to [ARTN, COM]	–0.3 to 6.5	V
Input voltage range CS to [ARTN,COM]	–0.3 to V_B	V
Input voltage range [ARTN, COM] to RTN	–2 to 2	V
Voltage range V_C, T2P, to [ARTN, COM]	–0.3 to 19	V
Voltage range GATE(4), GAT2(4) to [ARTN, COM]	–0.3 to V_C+0.3	V
Sinking current RTN	Internally limited	mA
Sourcing current V_B	Internally limited	mA
Average Sourcing or sinking current, GATE, GAT2	25	mArms
ESD rating, HBM	2	kV
ESD rating, CDM	500	V
ESD – system level (contact/air) at RJ-45(5)	8 / 15	kV
Operating junction temperature range, T_J	–40 to Internally limited	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ARTN and COM must be tied to RTN.
(3) I_{RTN} = 0 for V_{RTN} > 80V.
(4) Do not apply voltage to these pins
(5) ESD per EN61000-4-2. A power supply containing the TPS23754 was subjected to the highest test levels in the standard. See the ESD section.

RECOMMENDED OPERATING CONDITIONS(1)

Voltage with respect to V_{SS} (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input voltage range ARTN, COM, PPD, RTN, V_{DD}, V_{DD1}	0		57	V
Input voltage range T2P, V_C to [ARTN, COM]	0		18	V
Input voltage range APD, CTL, DT to [ARTN, COM]	0		V_B	V
Input voltage range CS to [ARTN, COM]	0		2	V
Continuous RTN current ($T_J \le 125°C$)(2)			825	mA
Sourcing current, V_B	0	2.5	5	mA
V_B capacitance	0.08			µF
R_{BLNK}	0		350	kΩ
Synchronization pulse width input (when used)	25			ns
Operating junction temperature range, T_J	–40		125	°C

(1) ARTN and COM tied to RTN.
(2) This is the minimum current-limit value. Viable systems will be designed for maximum currents below this value with reasonable margin. IEEE 802.3at (draft) permits 600mA continuous loading

DISSIPATION RATINGS

PACKAGE	Ψ_{JT} °C/W(1)	θ_{JP} °C/W	θ_{JA} °C/W(2)	θ_{JA} °C/W(3)	MAXIMUM POWER RATING (W)(4)
PWP (TSSOP-20)	0.607	1.4	32.6	73.8	1.2

(1) Thermal resistance junction to case top.
(2) See TI document SLMA002C (or latest version) for recommended layout. This is a best case, natural convection number.
(3) JEDEC method with high-k board (2 signal – 2 plane layers) and power pad not soldered (worst case).
(4) Based on TI recommended layout and 85°C.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: CS=COM=APD=CTL=RTN=ARTN, GATE & GAT2 float, R_{FRS}=68.1 kΩ, R_{BLNK}=249 kΩ, DT=V_B, PPD=V_{SS}, T2P open, C_{VB}=C_{VC}=0.1 µF, R_{DEN}=24.9 kΩ, R_{CLS} open, 0 V ≤ (V_{DD}, V_{DD1}) ≤ 57 V, 0 V ≤ V_C ≤ 18 V, –40°C ≤ T_J ≤ 125°C. Typical specifications are at 25°C.

CONTROLLER SECTION ONLY

[V_{SS} = RTN and V_{DD}=V_{DD1}] or [V_{SS}=RTN=V_{DD}], all voltages referred to [ARTN, COM].

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_C						
V_{CUV}	UVLO	V_C rising '754	14.3	15	15.7	V
		V_C rising '756	8.7	9	9.3	
V_{CUVH}		Hysteresis '754 (1)	6.2	6.5	6.8	
		Hysteresis '756 (1)	3.3	3.5	3.7	
	Operating current	V_C = 12 V, CTL = V_B, R_{DT} = 68.1 kΩ	0.7	0.92	1.2	mA
t_{ST}	Bootstrap startup time, C_{VC} = 22 µF	'756, V_{DD1} = 10.2 V, V_C(0) = 0 V	50	85	175	ms
		'756, V_{DD1} = 35 V, V_C(0) = 0 V	27	45	92	
		'754, V_{DD1} = 19.2 V, V_C(0) = 0 V	49	81	166	
		'754, V_{DD1} = 35 V, V_C(0) = 0 V	44	75	158	
	Startup current source - I_{VC}	'754, V_{DD1} = 19.2 V, V_C = 13.9 V	1.7	3.4	5.5	mA
		'756, V_{DD1} = 10.2 V, V_C = 8.6 V	0.44	1.06	1.80	
		'754, '756, V_{DD1} = 48 V, V_C = 0 V	2.7	4.8	6.8	
V_B						
	Voltage	6.5 V ≤ V_C ≤ 18 V, 0 ≤ I_{VB} ≤ 5 mA	4.8	5.10	5.25	V

(1) The hysteresis tolerance tracks the rising threshold for a given device.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FRS						
	Switching frequency	CTL = V_B, measure GATE				kHz
		R_{FRS} = 68.1 kΩ	227	253	278	
D_{MAX}	Duty cycle	CTL= V_B, measure GATE	76	78	80	%
V_{SYNC}	Synchronization	Input threshold	2	2.2	2.4	V
CTL						
V_{ZDC}	0% duty cycle threshold	V_{CTL} ↓ until GATE stops	1.3	1.5	1.7	V
	Softstart period	Interval from switching start to V_{CSMAX}	1.9	3.9	6.2	ms
	Input resistance		70	100	145	kΩ
BLNK						
	Blanking delay (In addition to t_1)	BLNK = RTN	35	55	78	ns
		R_{BLNK} = 49.9 kΩ	38	55	70	
DT						
		CTL = V_B, C_{GATE} = 1 nF, C_{GAT2} = 1 nF, measure GATE, GAT2				ns
t_{DT1}	Dead time See Figure 2 for t_{DTx} definition	R_{DT} = 24.9 kΩ, GAT2 ↑ to GATE ↑	40	50	62.5	
t_{DT2}		R_{DT} = 24.9 kΩ, GATE ↓ to GAT2 ↓	40	50	62.5	
t_{DT1}		R_{DT} = 75 kΩ, GAT2 ↑ to GATE ↑	120	150	188	
t_{DT2}		R_{DT} = 75 kΩ, GATE ↓ to GAT2 ↓	120	150	188	
CS						
V_{CSMAX}	Maximum threshold voltage	V_{CTL} = V_B, V_{CS} rising until GATE duty cycle drops	0.5	0.55	0.6	V
t_1	Turnoff delay	V_{CS} = 0.65 V	24	40	70	ns
V_{SLOPE}	Internal slope compensation voltage	Peak voltage at maximum duty cycle, referenced to CS	120	155	185	mV
I_{SL_EX}	Peak slope compensation current	V_{CTL} = V_B, I_{CS} at maximum duty cycle	30	42	54	µA
	Bias current (sourcing)	DC component of I_{CS}	1	2.5	4.3	µA
GATE						
	Source current	V_{CTL} = V_B, V_C = 12 V, GATE high, pulsed measurement	0.37	0.6	0.95	A
	Sink current	V_{CTL} = V_B, V_C = 12 V, GATE low, pulsed measurement	0.7	1.0	1.4	A
GAT2						
	Source current	V_{CTL} = V_B, V_C = 12 V, GAT2 high, R_{DT} = 24.9 kΩ, pulsed measurement	0.37	0.6	0.95	A
	Sink current	V_{CTL} = V_B, V_C = 12 V, GAT2 low, R_{DT} = 24.9 kΩ, pulsed measurement	0.7	1.0	1.4	A
APD / PPD						
V_{APDEN}	APD threshold voltage	V_{APD} rising	1.43	1.5	1.57	V
V_{APDH}		Hysteresis (2)	0.29	0.31	0.33	
V_{PPDEN}	PPD threshold voltage	V_{PPD}- V_{VSS} rising, UVLO disable	1.45	1.55	1.65	V
V_{PPDH}		Hysteresis (2)	0.29	0.31	0.33	
V_{PPD2}		V_{PPD}- V_{VSS} rising, Class enable	7.4	8.3	9.2	V
V_{PPD2H}		Hysteresis (2)	0.5	0.6	0.7	
	APD leakage current (source or sink)	V_C = 12 V, V_{APD} = V_B			1	µA
I_{PPD}	PPD sink current	$V_{PPD-VSS}$ = 1.5 V	2.5	5	7.5	µA
THERMAL SHUTDOWN						
	Turnoff temperature	T_J rising	135	145	155	°C
	Hysteresis (3)			20		°C

(2) The hysteresis tolerance tracks the rising threshold for a given device.
(3) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

ELECTRICAL CHARACTERISTICS – PoE AND CONTROL

[V_{DD}=V_{DD1}] or [V_{DD1}=RTN], V_C = RTN, COM=RTN=ARTN, all voltages referred to V_{SS} unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DETECTION (DEN)		(VDD = VDD1 = RTN = V_{SUPPLY} positive)				
	Detection current	Measure I_{SUPPLY}				
		V_{DD} = 1.6 V	62	64.3	66.5	µA
		V_{DD} = 10 V	399	406	414	
	Detection bias current	V_{DD} = 10 V, float DEN, measure I_{SUPPLY}, Note: Not during Mark state		5.6	10	µA
V_{PD_DIS}	Hotswap disable threshold		3	4	5	V
	DEN leakage current	V_{DEN} = V_{DD} = 57 V, float V_{DD1} and RTN, measure I_{DEN}		0.1	5	µA
CLASSIFICATION (CLS)		(V_{DD} = V_{DD1} = RTN = V_{SUPPLY} positive)				
I_{CLS}	Classification current, applies to both cycles	13 V ≤ V_{DD} ≤ 21 V, Measure I_{SUPPLY}				mA
		R_{CLS} = 1270 Ω	1.8	2.1	2.4	
		R_{CLS} = 243 Ω	9.9	10.4	10.9	
		R_{CLS} = 137 Ω	17.6	18.5	19.4	
		R_{CLS} = 90.9 Ω	26.5	27.7	29.3	
		R_{CLS} = 63.4 Ω	38.0	39.7	42	
	Classification mark resistance	5.6 V ≤ V_{DD} ≤ 9.4 V	7.5	9.7	12	kΩ
V_{CL_ON}	Classification regulator lower threshold	Regulator turns on, V_{DD} rising	11.2	11.9	12.6	V
V_{CL_H}		Hysteresis(1)	1.55	1.65	1.75	
V_{CU_OFF}	Classification regulator upper threshold	Regulator turns off, V_{DD} rising	21	22	23	V
V_{CU_H}		Hysteresis(1)	0.5	0.75	1.0	
V_{MSR}	Mark state reset	V_{DD} falling	3	4	5	V
	Leakage current	V_{DD} = 57 V, V_{CLS} = 0 V, DEN = V_{SS}, measure I_{CLS}			1	µA
PASS DEVICE (RTN)		(V_{DD1} = RTN)				
	On resistance		0.25	0.43	0.75	Ω
	Current limit	V_{RTN} = 1.5 V, V_{DD} = 48 V, pulsed measurement	850	970	1100	mA
	Inrush limit	V_{RTN} = 2 V, V_{DD}: 0 V → 48 V, pulsed measurement	100	140	180	mA
	Foldback voltage threshold	V_{DD} rising	11	12.3	13.6	V
UVLO						
V_{UVLO_R}	UVLO threshold	V_{DD} rising	33.9	35	36.1	V
V_{UVLO_H}		Hysteresis(1)	4.4	4.55	4.76	
T2P						
	ON characteristic	Perform classification algorithm, $V_{T2P-RTN}$ = 1 V, CTL = ARTN	2			mA
	Leakage current	V_{T2P} = 18 V, CTL = V_B			10	µA
t_{T2P}	Delay	From start of switching to T2P active	5	9	15	ms
THERMAL SHUTDOWN						
	Turnoff temperature	T_J rising	135	145	155	°C
	Hysteresis(2)			20		°C

(1) The hysteresis tolerance tracks the rising threshold for a given device.
(2) These parameters are provided for reference only, and do not constitute part of TI's published specifications for purposes of TI's product warranty.

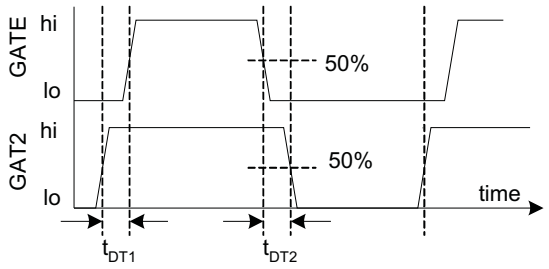
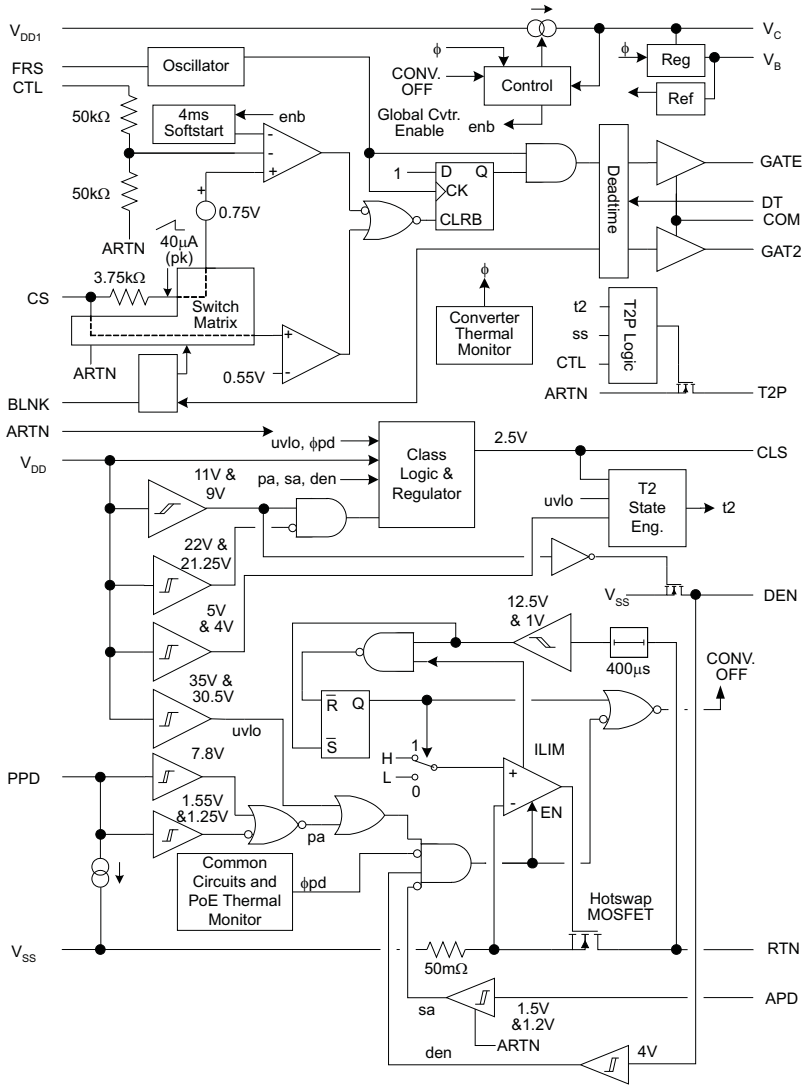


Figure 2. GATE and GAT2 Timing and Phasing

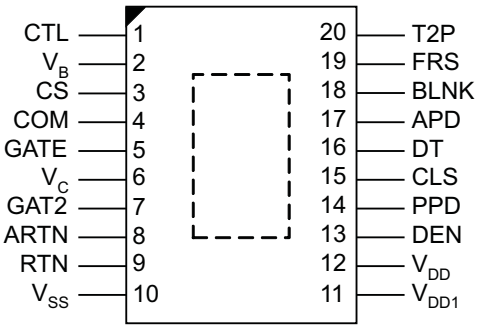
DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAM



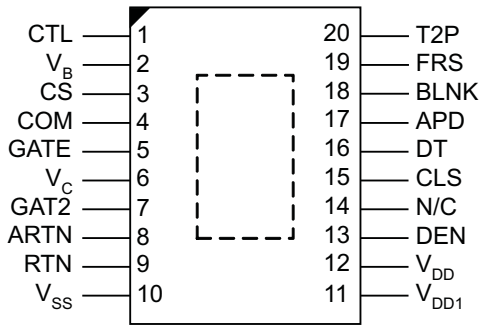
(TOP VIEW)

TPS23754/6



PAD = V_{SS}

TPS23754-1



PAD = V_{SS}

N/C = Leave Pin Unused

PIN FUNCTIONS

NAME	NO.		TYPE	DESCRIPTION
	'754/6	'754-1		
CTL	1	1	I	The control loop input to the PWM (pulse width modulator), typically driven by output regulation feedback (e.g. optocoupler). Use V_B as a pullup for CTL.
V_B	2	2	O	5.1 V bias rail for dc/dc control circuits and the feedback optocoupler. Typically bypass with a 0.1 µF to ARTN.
CS	3	3	I/O	DC/DC converter switching MOSFET current sense input. See R_{CS} in Figure 1.
COM	4	4		Gate driver return, connect to ARTN and RTN.
GATE	5	5	O	Gate drive output for the main dc/dc converter switching MOSFET.
V_C	6	6	I/O	DC/DC converter bias voltage. Connect a 0.47 µF (minimum) ceramic capacitor to ARTN at the pin, and a larger capacitor to power startup.
GAT2	7	7	O	Gate drive output for a second dc/dc converter switching MOSFET (see Figure 1).
ARTN	8	8		ARTN is the dc/dc converter analog return. Tie to RTN and COM on the circuit board.
RTN	9	9		RTN is the output of the PoE hotswap MOSFET.
V_{SS}	10	10		Connect to the negative power rail derived from the PoE source.
V_{DD1}	11	11	I	Source of dc/dc converter startup current. Connect to V_{DD} for many applications.
V_{DD}	12	12	I	Connect to the positive PoE input power rail. V_{DD} powers the PoE interface circuits. Bypass with a 0.1 µF capacitor and protect with a TVS.
DEN	13	13	I/O	Connect a 24.9 kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. Pulling this pin to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off.
NC	–	14		Float this no-connect pin.
PPD	14	–	I	Raising $V_{PPD-VSS}$ above 1.55 V enables the hotswap MOSFET and activates T2P. Connecting PPD to V_{DD} enables classification when APD is active. Tie PPD to V_{SS} or float when not used.
CLS	15	15	I	Connect a resistor from CLS to V_{SS} to program classification current. 2.5 V is applied to the program resistor during classification to set class current.
DT	16	16	I	Connect a resistor from DT to ARTN to set the GATE to GAT2 dead time. Tie DT to V_B to disable GAT2 operation.
APD	17	17	I	Raising V_{APD}-V_{ARTN} above 1.5 V disables the internal hotswap switch, turns class off, and forces T2P active. This forces power to come from a external $V_{DD1-RTN}$ adapter. Tie APD to ARTN when not used.
BLNK	18	18	I	Connect to ARTN to utilize the internally set current-sense blanking period, or connect a resistor from BLNK to ARTN to program a more accurate period.
FRS	19	19	I	Connect a resistor from FRS to ARTN to program the converter switching frequency. FRS may be used to synchronize the converter to an external timing source.
T2P	20	20	O	Active low output that indicates a PSE has performed the IEEE 802.3at type 2 hardware classification, PPD is active, or APD is active.
Pad	–	–		Connect to V_{SS}.

PIN DESCRIPTION

Refer to Figure 1 for component reference designators (R_{CS} for example), and the Electrical Characteristics table for values denoted by reference (V_{CSMAX} for example). Electrical Characteristic values take precedence over any numerical values used in the following sections.

APD

APD forces power to come from an external adapter connected from V_{DD1} to RTN by opening the hotswap switch, disabling the CLS output (see PPD pin description), and enabling the T2P output. A resistor divider is recommended on APD when it is connected to an external adapter. The divider provides ESD protection, leakage discharge for the adapter ORing diode, and input voltage qualification. Voltage qualification assures the adapter output voltage is high enough that it can support the PD before the PoE current is cut off.

Select the APD divider resistors per Equation 1 where $V_{ADPTR-ON}$ is the desired adapter voltage that enables the APD function as adapter voltage rises.

$$R_{APD1} = R_{APD2} \times \left(V_{ADPTR\_ON} - V_{APDEN}\right) / V_{APDEN}$$

$$V_{ADPTR\_OFF} = \frac{R_{APD1} + R_{APD2}}{R_{APD2}} \times \left(V_{APDEN} - V_{APDH}\right) \quad (1)$$

Place the APD pull-down resistor adjacent to the APD pin.

APD should be tied to ARTN when not used.

BLNK

Blanking provides an interval between GATE going high and the current-control comparators on CS actively monitoring the input. This delay allows the normal turn-on current transient (spike) to subside before the comparators are active, preventing undesired short duty cycles and premature current limiting.

Connect BLNK to ARTN to obtain the internally set blanking period. Connect a resistor from BLNK to ARTN for a more accurate, programmable blanking period. The relationship between the desired blanking period and the programming resistor is defined by Equation 2.

$$R_{BLNK}\left(k\Omega\right) = t_{BLNK}\left(ns\right) \quad (2)$$

Place the resistor adjacent to the BLNK pin when it is used.

CLS

A resistor from CLS to V_{SS} programs the classification current per the IEEE standard. The PD power ranges and corresponding resistor values are listed in Table 1. The power assigned should correspond to the maximum average power drawn by the PD during operation.

High-power PSEs may perform two classification cycles if Class 4 is presented on the first cycle. The TPS23754 presents the same (resistor programmed) class each cycle per the standard.

Table 1. Class Resistor Selection

CLASS	POWER AT PD		RESISTOR (Ω)	NOTES
	MINIMUM (W)	MAXIMUM (W)		
0	0.44	12.95	1270	Minimum may be reduced by pulsed loading. Serves as a catch-all default class.
1	0.44	3.84	243	
2	3.84	6.49	137	
3	6.49	12.95	90.9	
4	12.95	25.5	63.4	Not allowed for IEEE 802.3-2005. Use to indicate a Type 2 PD (high power) per IEEE 802.3at.

CS

The CS (current sense) input for the dc/dc converter should be connected to the high side of the switching MOSFET's current sense resistor (R_{CS}). The current-limit threshold, V_{CSMAX}, defines the voltage on CS above which the GATE ON time will be terminated regardless of the voltage on CTL.

The TPS23754 provides internal slope compensation (150 mV, V_{SLOPE}), an output current for additional slope compensation, a peak current limiter, and an off-time pull-down to this pin.

Routing between the current-sense resistor and the CS pin should be short to minimize cross-talk from noisy traces such as the gate drive signal.

CTL

CTL (control) is the voltage-control loop input to the PWM (pulse width modulator). Pulling V_{CTL} below V_{ZDC} causes GATE to stop switching. Increasing V_{CTL} above V_{ZDC} (zero duty cycle voltage) raises the switching MOSFET programmed peak current. The maximum (peak) current is requested at approximately V_{ZDC} + (2 × V_{CSMAX}). The ac gain from CTL to the PWM comparator is 0.5. The internal divider from CTL to ARTN is approximately 100 kΩ.

Use V_B as a pull up source for CTL.

DEN

DEN (detection and enable) is a multifunction pin for PoE detection and inhibiting operation from PoE power. Connect a 24.9 kΩ resistor from DEN to V_{DD} to provide the PoE detection signature. DEN goes to a high-impedance state when $V_{VDD-VSS}$ is outside of the detection range. Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET and class regulator to turn off, while the reduced detection resistance prevents the PD from properly re-detecting.

DT

Dead-time programming sets the delay between GATE and GAT2 to prevent overlap of MOSFET ON times as shown in Figure 2. GAT2 turns the second MOSFET off when it transitions high. Both MOSFETs should be off between GAT2 going high to GATE going high, and GATE going low to GAT2 going low. The maximum GATE ON time is reduced by the programmed dead-time period. The dead time period is specified with 1 nF of capacitance on GATE and GAT2. Different loading on these pins will change the effective dead time.

A resistor connected from DT to ARTN sets the delay between GATE and GAT2 per Equation 3.

$$R_{DT}\left(k\Omega\right) = \frac{t_{DT}\left(ns\right)}{2} \tag{3}$$

Connect DT to V_B to set the dead time to 0 and turn GAT2 off.

FRS

Connect a resistor from FRS (frequency and synchronization) to ARTN to program the converter switching frequency. Select the resistor per the following relationship.

$$R_{FRS}(k\Omega) = \frac{17250}{f_{SW}(kHz)} \tag{4}$$

The converter may be synchronized to a frequency above its maximum free-running frequency by applying short ac-coupled pulses into the FRS pin per Figure 30.

The FRS pin is high impedance. Keep the connections short and apart from potential noise sources. Special care should be taken to avoid crosstalk when synchronizing circuits are used.

GATE

Gate drive output for the dc/dc converter's main switching MOSFET. GATE's phase turns the main switch on when it transitions high, and off when it transitions low. GATE is held low when the converter is disabled.

GAT2

GAT2 is the second gate drive output for the dc/dc converter. GAT2's phase turns the second switch off when it transitions high, and on when it transitions low. This drives active-clamp PMOS devices per Figure 1, and driven flyback synchronous rectifiers per Figure 28. See the DT Pin Description for GATE to GAT2 timing. Connecting DT to V_B disables GAT2 in a high-impedance condition. GAT2 is low when the converter is disabled.

PPD

PPD is a multifunction pin that has two voltage thresholds, PPD1 and PPD2.

PPD1 permits power to come from an external low voltage adapter, e.g., 24 V, connected from V_{DD} to V_{SS} by over-riding the normal hotswap UVLO. Voltage on PPD above 1.55 V (V_{PPDEN}) enables the hotswap MOSFET, inhibits class current, and enables T2P. A resistor divider per Figure 35 provides ESD protection, leakage discharge for the adapter ORing diode, reverse adapter protection, and input voltage qualification. Voltage qualification assures the adapter output voltage is high enough that it can support the PD before it begins to draw current.

$$R_{PPD1} = \left(\frac{V_{ADPTR\_ON} - V_{PPDEN}}{\frac{V_{PPDEN}}{R_{PPD2}} - I_{PPD}} \right)$$

$$V_{ADPTR\_OFF} = \left(V_{PPDEN} - V_{PPDH}\right) + \left[R_{PPD1} \times \left(\frac{\left(V_{PPDEN} - V_{PPDH}\right)}{R_{PPD2}} - I_{PPD} \right) \right] \quad (5)$$

PPD2 enables normal class regulator operation when V_{PPD} is above 8.3 V to permit type 2 classification when APD is used in conjunction with diode D_{VDD} (see Figure 34). Tie PPD to V_{DD} when PPD2 operation is desired.

The PPD pin has a 5 µA internal pull-down current.

Locate the PPD pull-down resistor adjacent to the pin when used.

PPD may be tied to V_{SS} or left open when not used.

RTN, ARTN, COM

RTN is internally connected to the drain of the PoE hotswap MOSFET, while ARTN is the quiet analog reference for the dc/dc controller return. COM serves as the return path for the gate drivers and should be tied to ARTN on the circuit board. The ARTN / COM / RTN net should be treated as a local reference plane (ground plane) for the dc/dc control and converter primary. RTN and (ARTN/COM) may be separated by several volts for special applications.

T2P

T2P is an active low output that indicates [(V_{APD} > 1.5 V) OR (1.55 V ≤ V_{PPD} ≤ 8.3 V) OR (type 2 hardware classification observed)]. T2P is valid after both a delay of t_{T2P} from the start of converter switching, and [V_{CTL} ≤ (V_B – 1 V)]. Once T2P is valid, V_{CTL} will not effect it. T2P will become invalid if the converter goes back into softstart, over-temperature, or is held off by the PD during C_{IN} recharge (inrush). T2P is referenced to ARTN and is intended to drive the diode side of an optocoupler. T2P should be left open or tied to ARTN if not used.

V_B

V_B is an internal 5.1V regulated dc/dc controller supply rail that is typically bypassed by a 0.1 µF capacitor to ARTN. V_B should be used to bias the feedback optocoupler.

V_C

V_C is the bias supply for the dc/dc controller. The MOSFET gate drivers run directly from V_C. V_B is regulated down from V_C, and is the bias voltage for the rest of the converter control. A startup current source from V_{DD1} to V_C is controlled by a comparator with hysteresis to implement the converter bootstrap startup. V_C must be connected to a bias source, such as a converter auxiliary output, during normal operation.

A minimum 0.47 µF capacitor, located adjacent to the V_C pin, should be connected from V_C to COM to bypass the gate driver. A larger total capacitance is required for startup to provide control power between the time the converter starts switching and the availability of the converter auxiliary output voltage.

V_{DD}

V_{DD} is the positive input power rail that is derived from the PoE source (PSE). V_{DD} should be bypassed to V_{SS} with a 0.1 µF capacitor as required by the IEEE standard. A transient suppressor diode (TVS), a special type of Zener diode, such as SMAJ58A should be connected from V_{DD} to V_{SS} to protect against over-voltage transients.

V_{DD1}

V_{DD1} is the dc/dc converter startup supply. Connect to V_{DD} for many applications. V_{DD1} may be isolated by a diode from V_{DD} to support PoE priority operation.

V_{SS}

V_{SS} is the PoE input-power return side. It is the reference for the PoE interface circuits, and has a current-limited hotswap switch that connects it to RTN. V_{SS} is clamped to a diode drop above RTN by the hotswap switch.

A local V_{SS} reference plane should be used to connect the input bypass capacitor, TVS, R_{CLS}, and the PowerPad. This plane becomes the main heatsink for the TPS23754.

V_{SS} is internally connected to the PowerPAD.

PowerPAD

The Powerpad is internally connected to V_{SS}. It should be tied to a large V_{SS} copper area on the PCB to provide a low resistance thermal path to the circuit board. It is recommended that a clearance of 0.025” be maintained between V_{SS}, RTN, and various control signals to high-voltage signals such as V_{DD} and V_{DD1}.

TYPICAL CHARACTERISTICS

DETECTION BIAS CURRENT vs VOLTAGE

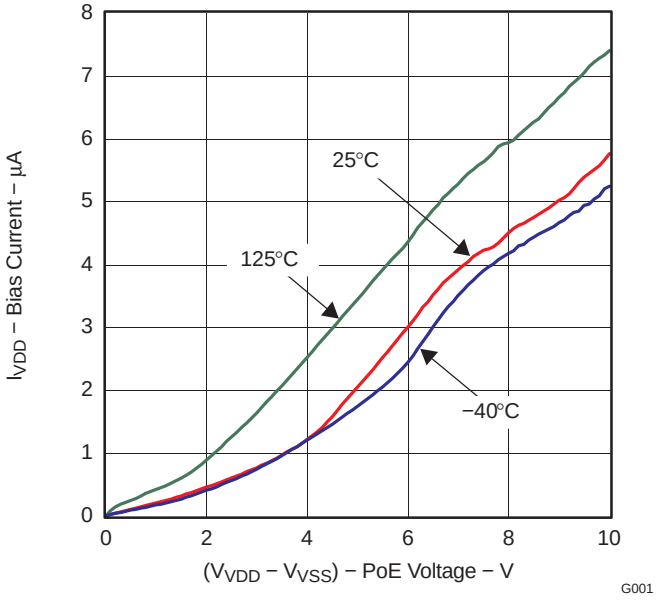


Figure 3.

PoE CURRENT LIMIT vs TEMPERATURE

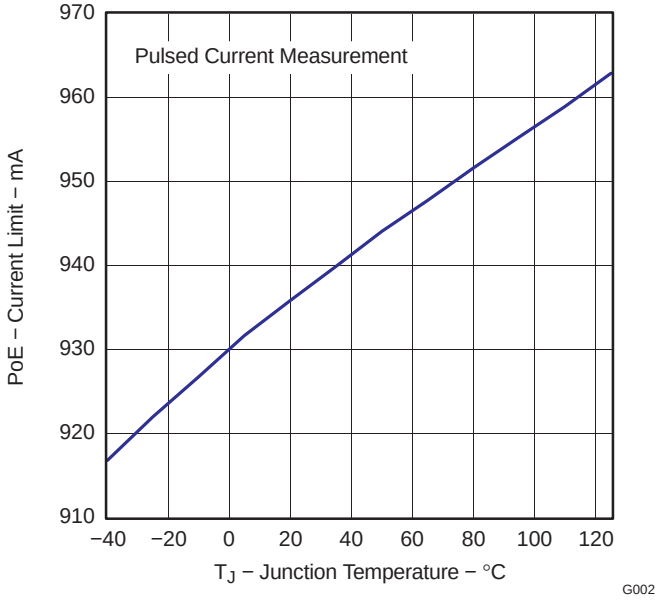


Figure 4.

TYPICAL CHARACTERISTICS (continued)

'754 CONVERTER START TIME vs TEMPERATURE

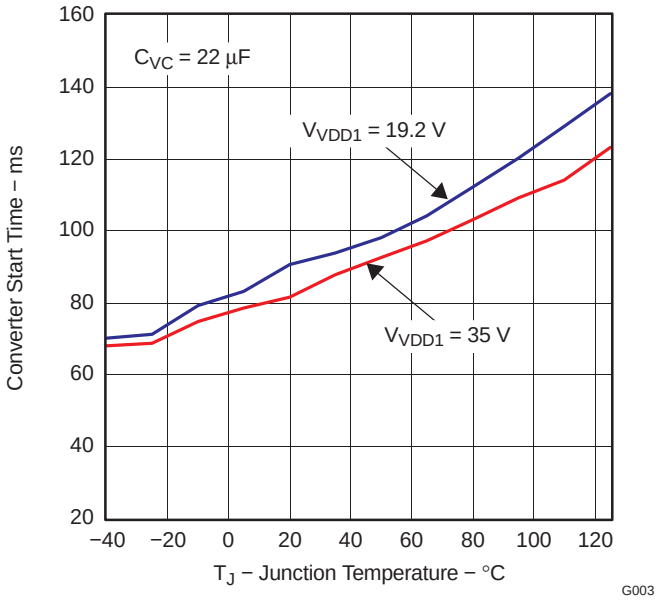


Figure 5.

'756 CONVERTER START TIME vs TEMPERATURE

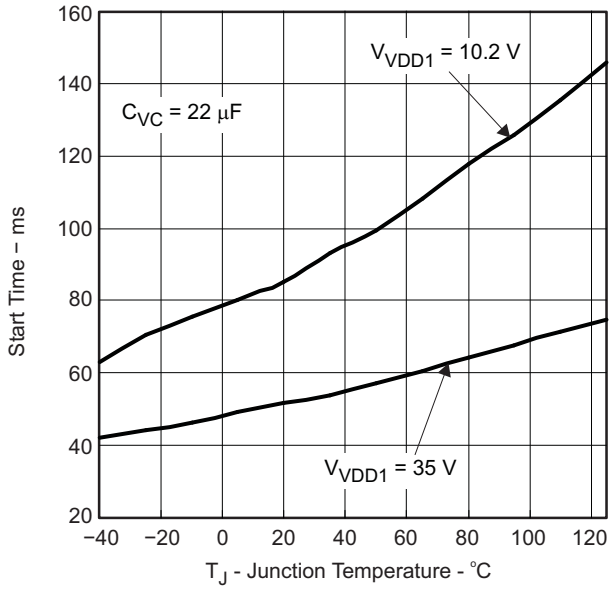


Figure 6.

'754 CONVERTER STARTUP CURRENT vs V_{VDD1}

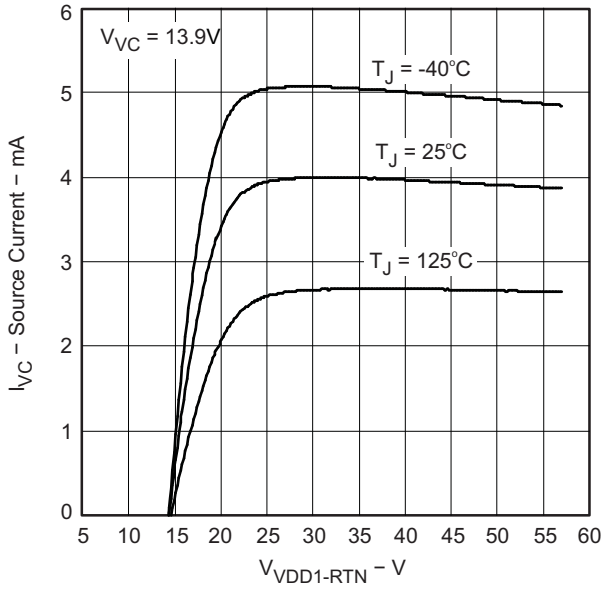


Figure 7.

'756 CONVERTER STARTUP CURRENT vs V_{VDD1}

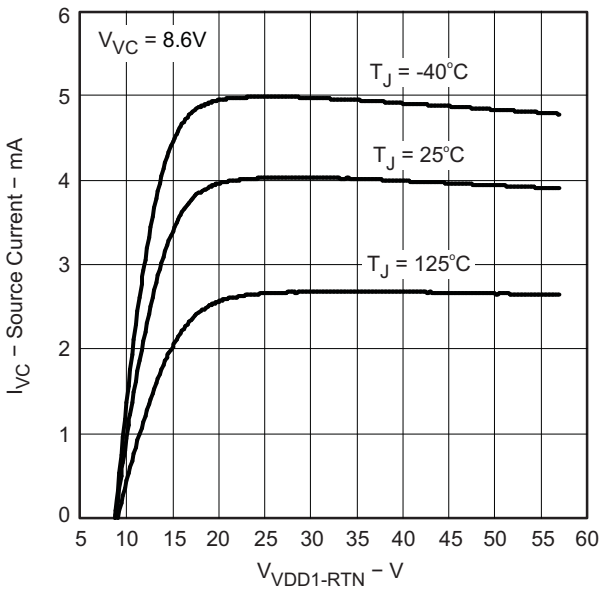


Figure 8.

TYPICAL CHARACTERISTICS (continued)

CONTROLLER BIAS CURRENT vs TEMPERATURE

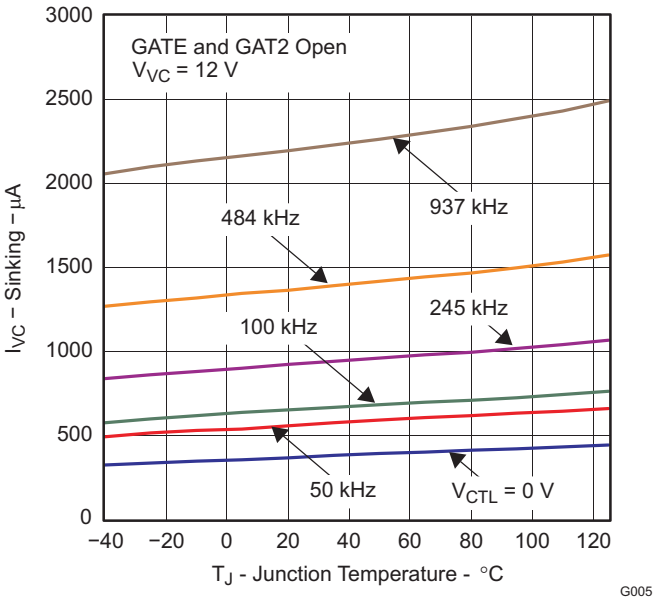


Figure 9.

'754 CONTROLLER BIAS CURRENT vs VOLTAGE

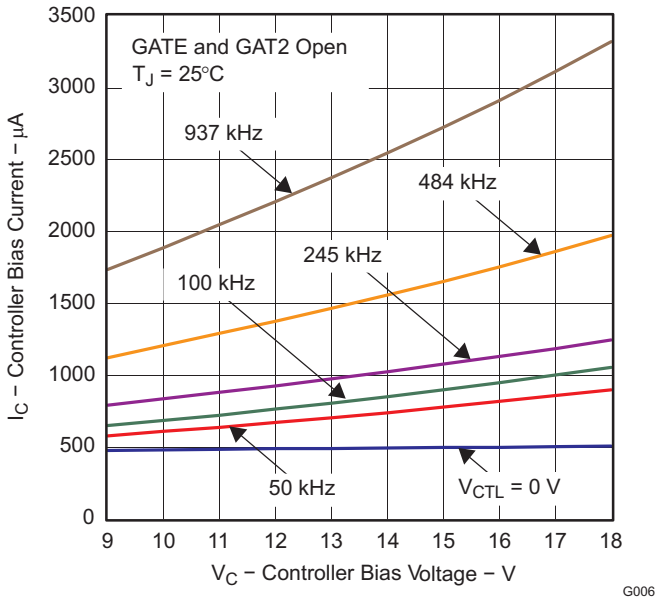


Figure 10.

'756 CONTROLLER BIAS CURRENT vs VOLTAGE

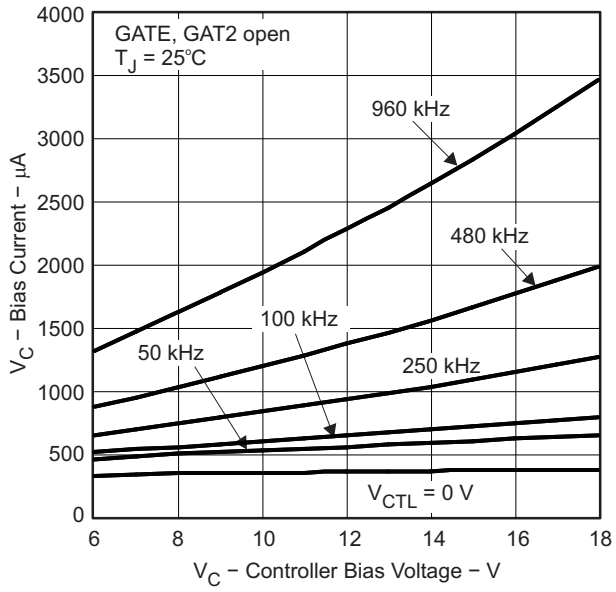


Figure 11.

SWITCHING FREQUENCY vs TEMPERATURE

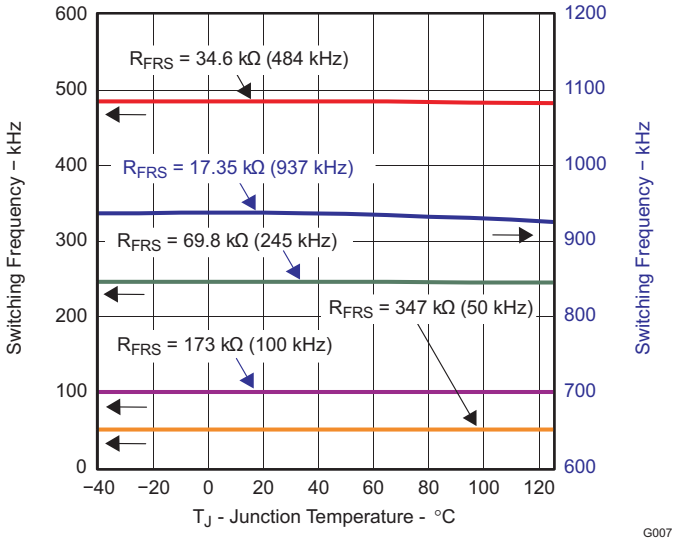


Figure 12.

TYPICAL CHARACTERISTICS (continued)

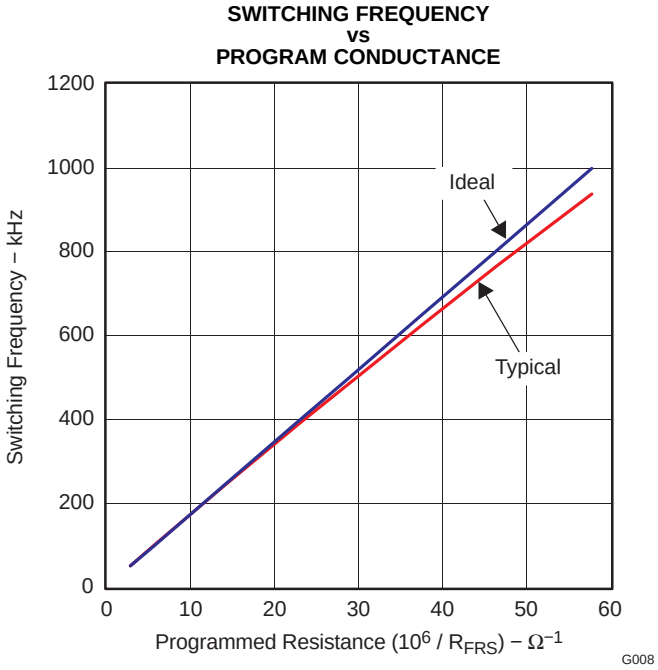


Figure 13.

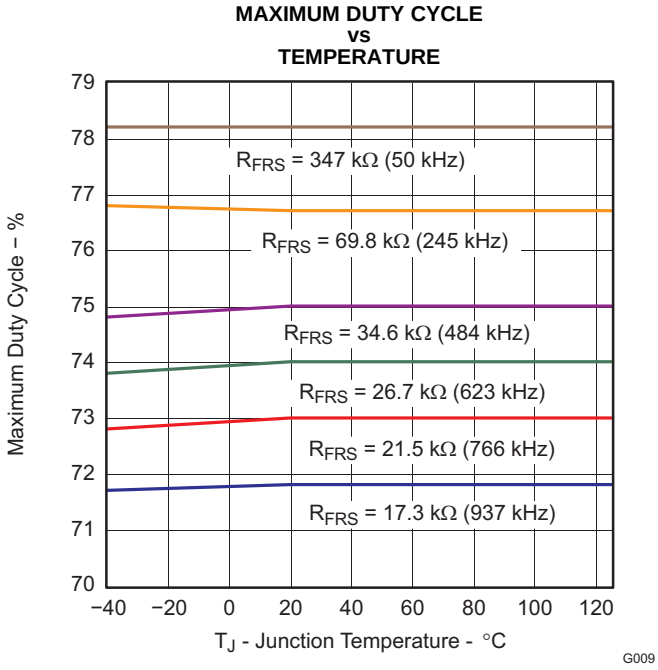


Figure 14.

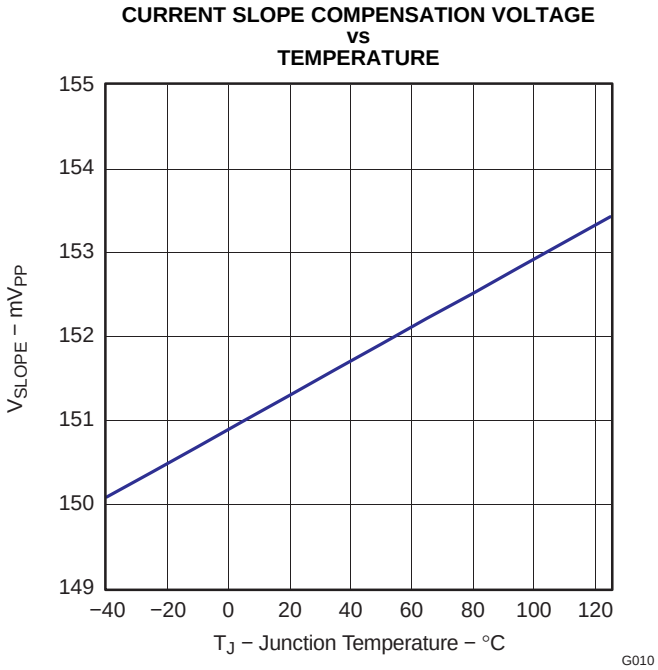


Figure 15.

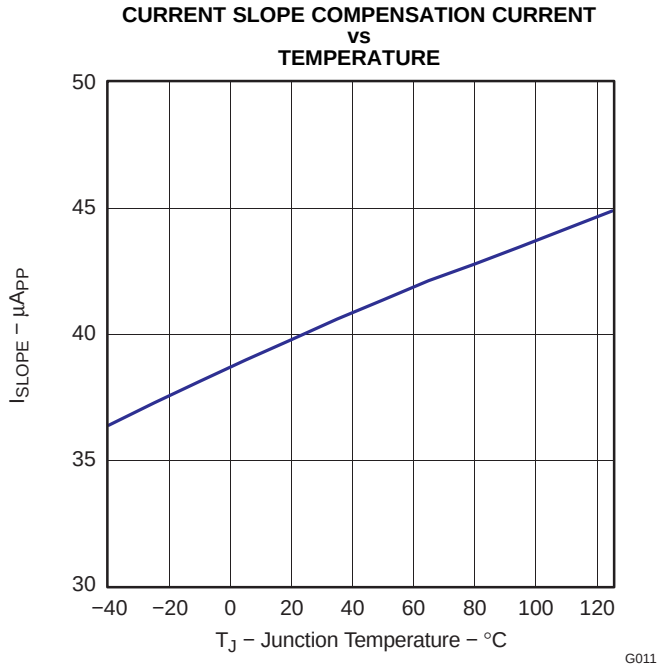


Figure 16.

TYPICAL CHARACTERISTICS (continued)

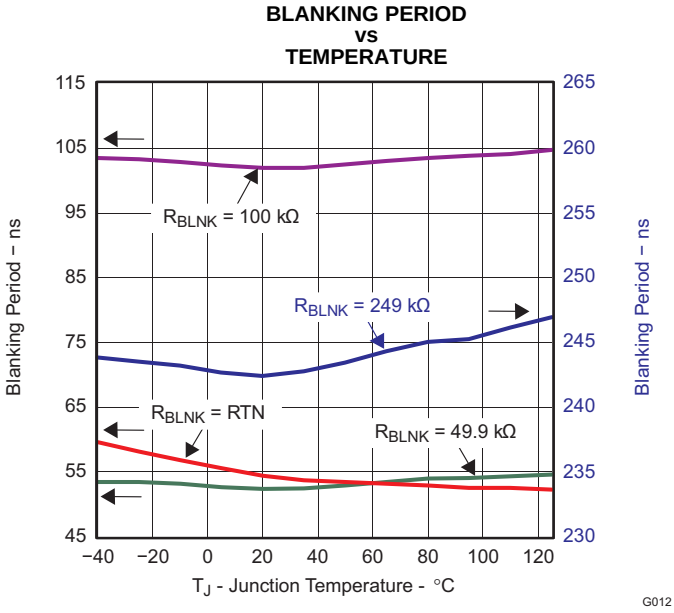


Figure 17.

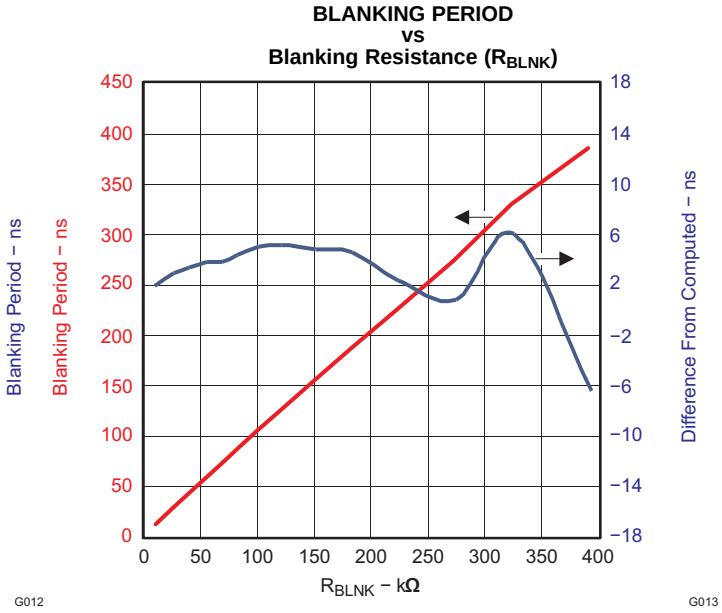


Figure 18.

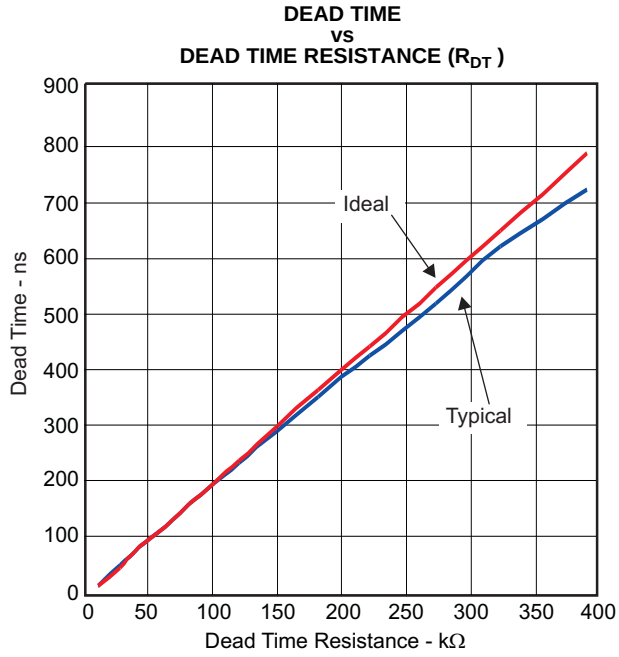


Figure 19.

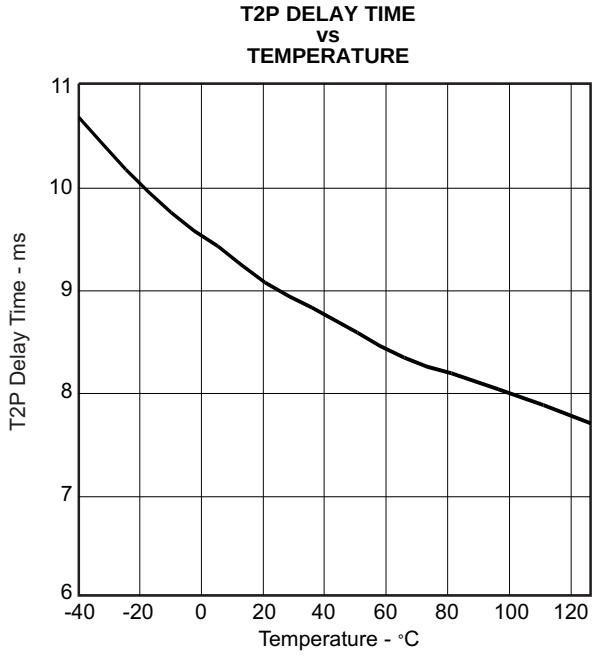


Figure 20.

DETAILED DESCRIPTION

PoE OVERVIEW

The following text is intended as an aid in understanding the operation of the TPS23754 but not as a substitute for the actual IEEE 802.3-2005 or IEEE 802.3at standard. The pending IEEE 802.3at standard is an update to IEEE 802.3-2005 clause 33 (PoE), adding high-power options and enhanced classification. Generally speaking, a device compliant to IEEE 802.3-2005 will be referred to as a type 1 device, and devices with high power and enhanced classification will be referred to as type 2 devices. Standards change and should always be referenced when making design decisions.

The IEEE 802.3-2005 (802.3at) standard defines a method of safely powering a PD (powered device) over a cable by power sourcing equipment (PSE), and then removing power if a PD is disconnected. The process proceeds through an idle state and three operational states of detection, classification, and operation. The PSE leaves the cable unpowered (idle state) while it periodically looks to see if something has been plugged in; this is referred to as detection. The low power levels used during detection are unlikely to damage devices not designed for PoE. If a valid PD signature is present, the PSE my inquire how much power the PD requires; this is referred to as classification. The PSE may then power the PD if it has adequate capacity.

Type 2 PSEs are required to do type 1 hardware classification plus a (new) data-layer classification, or an enhanced type 2 hardware classification. Type 1 PSEs are not required to do hardware or data link layer (DLL) classification. A type 2 PD must do type 2 hardware classification as well as DLL classification. The PD may return the default 12.95W (often referred to as 13W) current-encoded class, or one of four other choices. DLL classification occurs after power-on and the ethernet data link has been established.

Once started, the PD must present the maintain power signature (MPS) to assure the PSE that it is still present. The PSE monitors its output for a valid MPS, and turns the port off if it loses the MPS. Loss of the MPS returns the PSE to the idle state. Figure 21 shows the operational states as a function of PD input voltage. The upper half is for IEEE 802.3-2005, and the lower half shows specific differences for IEEE 802.3at. The dashed lines in the lower half indicate these are the same (e.g., Detect and Class) for both.

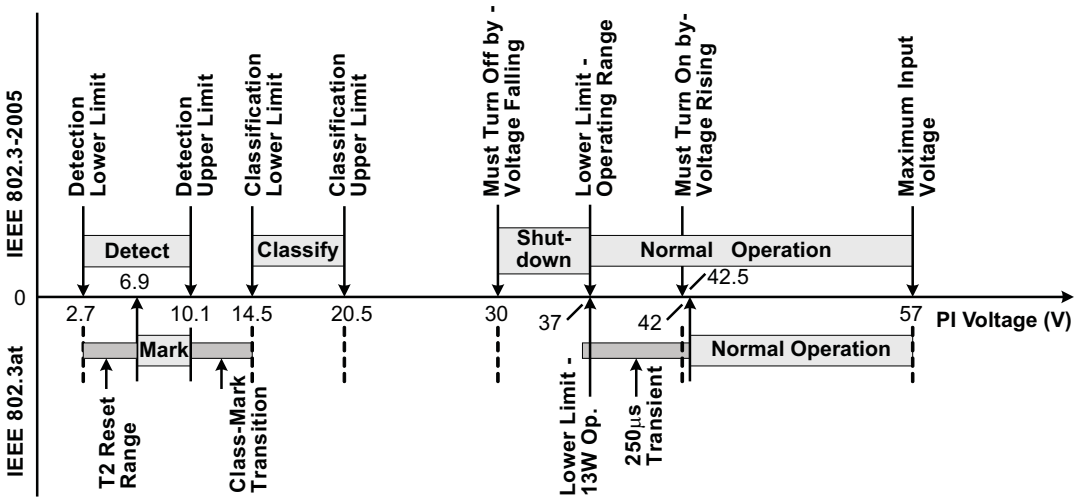


Figure 21. Operational States for PD

The PD input, typically an RJ-45 eight-lead connector, is referred to as the power interface (PI). PD input requirements differ from PSE output requirements to account for voltage drops and operating margin. The standard allots the maximum loss to the cable regardless of the actual installation to simplify implementation. IEEE 802.3-2005 was designed to run over infrastructure including ISO/IEC 11801 class C (CAT3 per TIA/EIA-568) that may have had AWG 26 conductors. IEEE 802.3at cabling power loss allotments and voltage drops have been adjusted for 12.5 Ω power loops per ISO/IEC11801 class D (CAT5 or higher per TIA/EIA-568, typically AWG #24 conductors). Table 2 shows key operational limits broken out for the two revisions of the standard.

Table 2. Comparison of Operational Limits

STANDARD	POWER LOOP RESISTANCE (max)	PSE OUTPUT POWER (min)	PSE STATIC OUTPUT VOLTAGE (min)	PD INPUT POWER (max)	STATIC PD INPUT VOLTAGE	
					POWER ≤ 12.95 W	POWER > 12.95 W
'2005	20 Ω	15.4 W	44 V	12.95 W	37 V–57 V	N/A
802.3at	12.5 Ω	36 W	50 V	25.5 W	37 V–57 V	42.5 V–57 V

The PSE can apply voltage either between the RX and TX pairs (pins 1 - 2 and 3 - 6 for 10baseT or 100baseT), or between the two spare pairs (4 - 5 and 7 - 8). Power application to the same pin combinations in 1000baseT systems is recognized in 802.3at. 1000baseT systems can handle data on all pairs, eliminating the spare pair terminology. The PSE may only apply voltage to one set of pairs at a time. The PD uses input diode bridges to accept power from any of the possible PSE configurations. The voltage drops associated with the input bridges create a difference between the standard limits at the PI and the TPS23754 specifications.

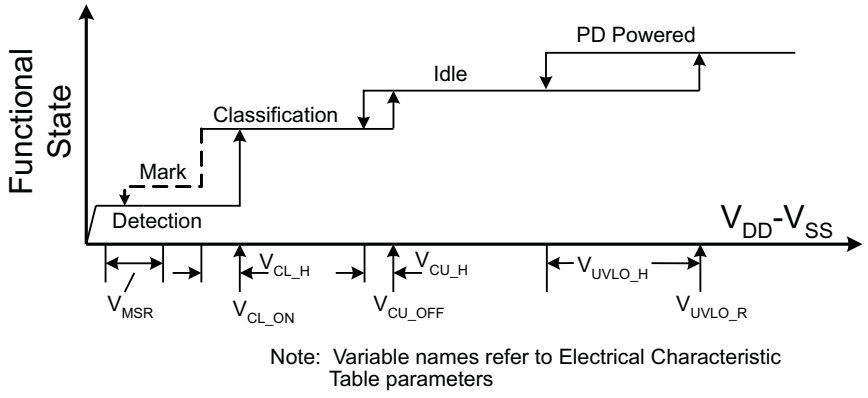
A compliant type 2 PD has power management requirements not present with a type 1 PD. These requirements include the following:

1. Must interpret type 2 hardware classification
2. Must present hardware class 4
3. Must implement DLL negotiation
4. Must behave like a type 1 PD during inrush and startup
5. Must not draw more than 13W for 80ms after PSE applies operating voltage (power-up)
6. Must not draw more than 13W if it has not received a type 2 hardware classification or received permission through DLL
7. Must meet various operating and transient templates
8. Optionally monitor for the presence or absence of an adapter (assume high power).

As a result of these requirements, the PD must be able to dynamically control its loading, and monitor T2P for changes. In cases where the design needs to know specifically if an adapter is plugged in and operational, the adapter should be individually monitored, typically with an optocoupler.

Threshold Voltages

The TPS23754 has a number of internal comparators with hysteresis for stable switching between the various states. Figure 22 relates the parameters in the Electrical Characteristics section to the PoE states. The mode labeled idle between classification and operation implies that the DEN, CLS, and RTN pins are all high impedance. The state labeled Mark, which is drawn in dashed lines, is part of the new type 2 hardware class state machine.



Note: Variable names refer to Electrical Characteristic Table parameters

Figure 22. Threshold Voltages

PoE Startup Sequence

The waveforms of Figure 23 demonstrate detection, classification, and startup from a PSE with type 2 hardware classification. The key waveforms shown are V_{VDD}-V_{VSS}, V_{RTN}-V_{VSS}, and I_{PI}. IEEE 802.3at requires a minimum of two detection levels, two class and mark cycles, and startup from the second mark event. V_{RTN} to V_{SS} falls as the TPS23754 charges C_{IN} following application of full voltage. Subsequently, the converter starts up, drawing current as seen in the I_{PI} waveform.

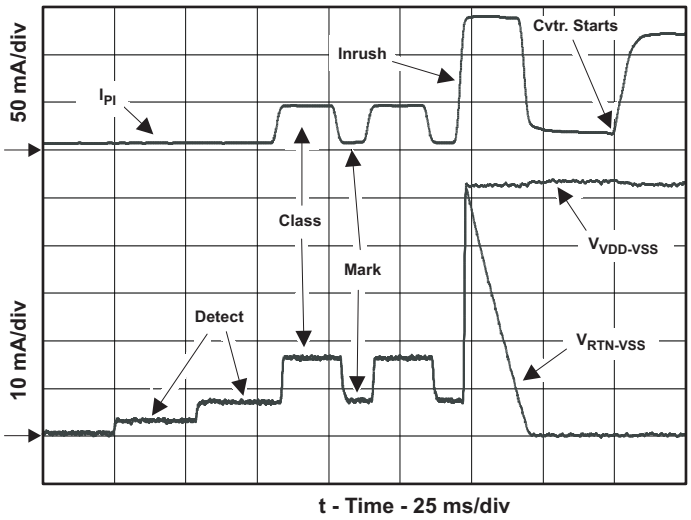


Figure 23. Startup

Detection

The TPS23754 drives DEN to V_{SS} whenever V_{VDD}-V_{VSS} is below the lower classification threshold. When the input voltage rises above V_{CL-ON}, the DEN pin goes to an open-drain condition to conserve power. While in detection, RTN is high impedance, and almost all the internal circuits are disabled. An R_{DEN} of 24.9 kΩ (1%), presents the correct signature. It may be a small, low-power resistor since it only sees a stress of about 5 mW. A valid PD detection signature is an incremental resistance (ΔV / ΔI) between 23.75 kΩ and 26.25 kΩ at the PI.

The detection resistance seen by the PSE at the PI is the result of the input bridge resistance in series with the parallel combination of R_{DEN} and internal V_{DD} loading. The input diode bridge's incremental resistance may be hundreds of ohms at the very low currents drawn when 2.7 V is applied to the PI. The input bridge resistance is partially cancelled by the TPS23754's effective resistance during detection.

The type 2 hardware classification protocol of IEEE 802.3at specifies that a type 2 PSE drops its output voltage into the detection range during the classification sequence. The PD is required to have an incorrect detection signature in this condition, which is referred to as the mark event (see Figure 23). After the first mark event, the TPS23754 will present a signature less than 12 kΩ until it has experienced a V_{VDD}-V_{VSS} voltage below the mark reset (V_{MSR}). This is explained more fully under Hardware Classification.

Hardware Classification

Hardware classification allows a PSE to determine a PD's power requirements before powering, and helps with power management once power is applied. Type 2 hardware classification permits high power PSEs and PDs to determine whether the connected device can support high-power operation. A type 2 PD presents class 4 in hardware to indicate it is a high-power device. A type 1 PSE will treat a class 4 device like a class 0 device, allotting 12.95 W if it chooses to power the PD. A PD that receives a 2 event class understands that it is powered from a high-power PSE and it may draw up to 25.5 W immediately after the 80 ms startup period completes. A type 2 PD that does not receive a 2-event hardware classification may choose to not start, or must start in a 13 W condition and request more power through the DLL after startup. The standard requires a type 2 PD to indicate that it is underpowered if this occurs. Startup of a high-power PD under 13 W implicitly requires some form of powering down sections of the application circuits.

The maximum power entries in Table 1 determine the class the PD must advertise. The PSE may disconnect a PD if it draws more than its stated Class power, which may be the hardware class or a lower DLL-derived power level. The standard permits the PD to draw limited current peaks that increase the instantaneous power above the Table 1 limit, however the average power requirement always applies.

The TPS23754 implements two-event classification. Selecting an R_{CLS} of 63.4 Ω provides a valid type 2 signature. TPS23754 may be used as a compatible type 1 device simply by programming class 0–3 per Table 1. DLL communication is implemented by the ethernet communication system in the PD and is not implemented by the TPS23754.

The TPS23754 disables classification above V_{CU_OFF} to avoid excessive power dissipation. CLS voltage is turned off during PD thermal limit or when APD or DEN are active. The CLS output is inherently current limited, but should not be shorted to V_{SS} for long periods of time.

Figure 24 shows how classification works for the TPS23754. Transition from state-to-state occurs when comparator thresholds are crossed (see Figure 21 and Figure 22). These comparators have hysteresis, which adds inherent memory to the machine. Operation begins at idle (unpowered by PSE) and proceeds with increasing voltage from left to right. A 2-event classification follows the (heavy lined) path towards the bottom, ending up with a latched type 2 decode along the lower branch that is highlighted. This state results in a low T2P during normal operation. Once the valid path to type 2 PSE detection is broken, the input voltage must transition below the mark reset threshold to start anew.

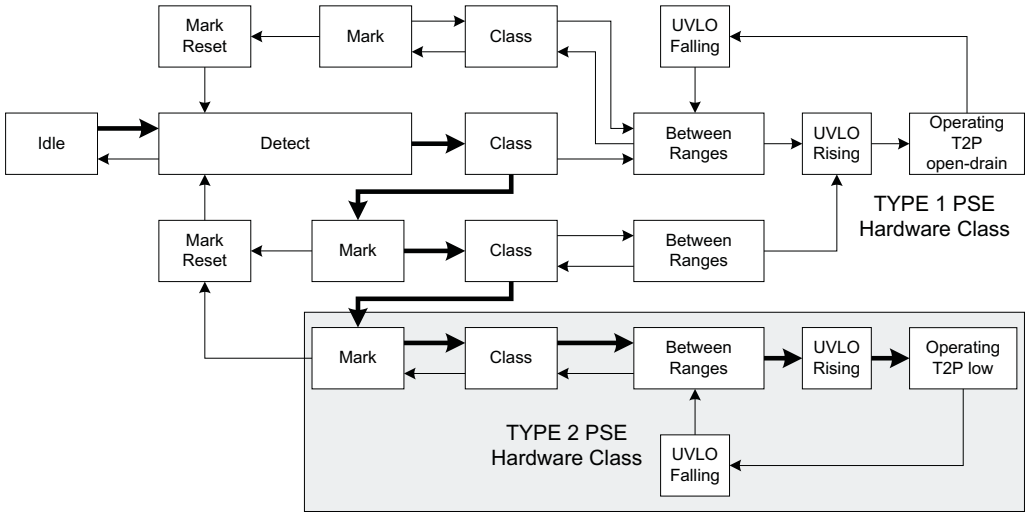


Figure 24. Two-Event Class Internal States

Inrush and Startup

802.3at has a startup current and time limitation, providing type 2 PSE compatibility for type 1 PDs. A type 2 PSE limits output current to between 400 mA and 450 mA for up to 75 ms after power-up (applying “48 V” to the PI) in order to mirror type 1 PSE functionality. The type 2 PSE will support higher output current after 75 ms. The TPS23754 implements a 140 mA inrush current, which is compatible with all PSE types. A high-power PD must control its converter startup peak and operational currents drawn to below 400 mA for 80 ms. The TPS23754’s internal softstart permits control of the converter startup, however the application circuits must assure that their power draw does not cause the PD to exceed the current/time limitation. This requirement implicitly requires some form of powering down sections of the application circuits. T2P becomes valid within t_{T2P} after switching starts, or if an adapter is plugged in while the PD is operating from a PSE.

Maintain Power Signature

The MPS is an electrical signature presented by the PD to assure the PSE that it is still present after operating voltage is applied. A valid MPS consists of a minimum dc current of 10 mA (or a 10 mA pulsed current for at least 75 ms every 225 ms) and an ac impedance lower than 26.25 kΩ in parallel with 0.05 µF. The ac impedance is usually accomplished by the minimum operating C_{IN} requirement of 5 µF. When either APD or DEN is used to force the hotswap switch off, the dc MPS will not be met. A PSE that monitors the dc MPS will remove power from the PD when this occurs. A PSE that monitors only the ac MPS may remove power from the PD.

Startup and Converter Operation

The internal PoE UVLO (Under Voltage Lock Out) circuit holds the hotswap switch off before the PSE provides full voltage to the PD. This prevents the converter circuits from loading the PoE input during detection and classification. The converter circuits will discharge C_{IN}, C_{VC}, and C_{VB} while the PD is unpowered. Thus V_{VDD}-V_{RTN} will be a small voltage just after full voltage is applied to the PD, as seen in Figure 23. The PSE drives the PI voltage to the operating range once it has decided to power up the PD. When V_{VDD} rises above the UVLO turn-on threshold (V_{UVLO-R}, ~35 V) with RTN high, the TPS23754 enables the hotswap MOSFET with a ~140 mA (inrush) current limit as seen in Figure 25. Converter switching is disabled while C_{IN} charges and V_{RTN} falls from V_{VDD} to nearly V_{VSS}, however the converter startup circuit is allowed to charge C_{VC} (the bootstrap startup capacitor). Converter switching is allowed if the PD is not in inrush, OTSD is not active, and the V_C UVLO permits it. Once the inrush current falls about 10% below the inrush current limit, the PD current limit switches to the operational level (~970 mA). Continuing the startup sequence shown in Figure 25, V_{VC} continues to rise until the startup threshold (V_{CUV}, ~15 V or ~9 V) is exceeded, turning the startup source off and enabling switching. The V_B regulator is always active, powering the internal converter circuits as V_{VC} rises. There is a slight delay between the removal of charge current and the start of switching as the softstart ramp sweeps above the V_{ZDC} threshold. V_{VC} falls as it powers both the internal circuits and the switching MOSFET gates. If the converter control bias output rises to support V_{VC} before it falls to $V_{CUV} – V_{CUVH}$ (~8.5 V or ~5.5 V), a successful startup occurs. T2P in Figure 23 (Figure 1, $V_{T2P-OUT}$) becomes active within t_{T2P} from the start of switching, indicating that a type 2 PSE or an adapter is plugged in.

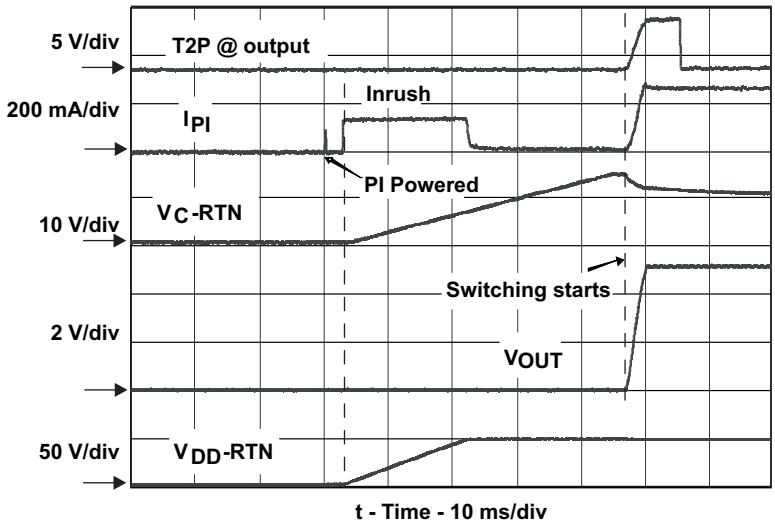


Figure 25. Power Up and Start

If V_{VDD}- V_{VSS} drops below the lower PoE UVLO (V_{UVLO-R} - V_{UVLO-H}, ~30.5 V), the hotswap MOSFET is turned off, but the converter will still run. The converter will stop if V_{VC} falls below the converter UVLO ($V_{CUV} – V_{CUVH}$, ~8.5 V or ~5.5 V), the hotswap is in inrush current limit, 0% duty cycle is demanded by V_{CTL} ($V_{CTL} < V_{ZDC}$, ~1.5 V), or the converter is in thermal shutdown.

PD Hotswap Operation

IEEE 802.3at has taken a new approach to PSE output limiting. A type 2 PSE must meet an output current vs. time template with specified minimum and maximum sourcing boundaries. The peak output current may be as high as 50 A for 10 µs or 1.75 A for 75 ms. This makes robust protection of the PD device even more important than it was in IEEE 802.3-2005.

The internal hotswap MOSFET is protected against output faults and input voltage steps with a current limit and deglitched (time-delay filtered) foldback. An overload on the pass MOSFET engages the current limit, with V_{RTN}-V_{VSS} rising as a result. If V_{RTN} rises above ~12 V for longer than ~400 µs, the current limit reverts to the inrush value, and turns the converter off. The 400 µs deglitch feature prevents momentary transients from

causing a PD reset, provided that recovery lies within the bounds of the hotswap and PSE protection. Figure 26 shows an example of recovery from a 16 V PSE rising voltage step. The hotswap MOSFET goes into current limit, overshooting to a relatively low current, recovers to ~950 mA full current limit, and charges the input capacitor while the converter continues to run. The MOSFET did not go into foldback because V_{RTN}-V_{VSS} was below 12 V after the 400 µs deglitch.

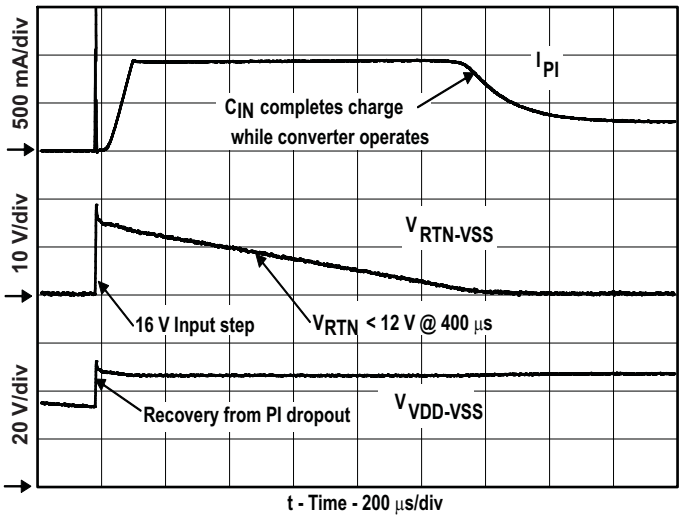


Figure 26. Response to PSE Step Voltage

The PD control has a thermal sensor that protects the internal hotswap MOSFET. Conditions like startup or operation into a V_{DD} to RTN short cause high power dissipation in the MOSFET. An over-temperature shutdown (OTSD) turns off the hotswap MOSFET and class regulator, which are restarted after the device cools. The hotswap MOSFET will be re-enabled with the inrush current limit when exiting from an over-temperature event.

Pulling DEN to V_{SS} during powered operation causes the internal hotswap MOSFET to turn off. This feature allows a PD with Option three ORing per Figure 27 to achieve adapter priority. Care must be taken with synchronous converter topologies that can deliver power in both directions.

The hotswap switch will be forced off under the following conditions:

1. V_{APD} above V_{APDEN} (~1.5 V)
2. $V_{DEN} < V_{PD-DIS}$ when $V_{VDD} – V_{VSS}$ is in the operational range
3. PD over-temperature
4. $(V_{VDD} – V_{VSS}) <$ PoE UVLO (~30.5 V).

Converter Controller Features

The TPS23754 dc/dc controller implements a typical current-mode control as shown in the Functional Block Diagram. Features include oscillator, over-current and PWM comparators, current-sense blanker, dead-time control, softstart, and gate driver. In addition, an internal slope-compensation ramp generator, frequency synchronization logic, thermal shutdown, and startup current source with control are provided.

The TPS23754 is optimized for isolated converters, and does not provide an internal error amplifier. Instead, the optocoupler feedback is directly fed to the CTL pin which serves as a current-demand control for the PWM. There is an offset of V_{ZDC} (~1.5 V) and 2:1 resistor divider between the CTL pin and the PWM. A V_{CTL} below V_{ZDC} will stop converter switching, while voltages above $(V_{ZDC} + (2 \times V_{CSMAX}))$ will not increase the requested peak current in the switching MOSFET. Optocoupler biasing design is eased by this limited control range.

Bootstrap Topology

The internal startup current source and control logic implement a bootstrap-type startup as discussed in "Startup and Converter Operation." The startup current source charges C_{VC} from V_{DD1} when the converter is disabled (either by the PD control or the V_C control) to store enough energy to start the converter. Steady-state operating power must come from a converter (bias winding) output or other source. Loading on V_C and V_B must be minimal while C_{VC} charges, otherwise the converter may never start. The optocoupler will not load V_B when the converter is off for most situations, however care should be taken in ORing topologies where the output is powered when PoE is off.

The converter will shut off when V_C falls below its lower UVLO. This can happen when power is removed from the PD, or during a fault on a converter output rail. When one output is shorted, all the output voltages fall including the one that powers V_C. The control circuit discharges V_C until it hits the lower UVLO and turns off. A restart will initiate as described in *Startup and Converter Operation* if the converter turns off and there is sufficient V_{DD1} voltage. This type of operation is sometimes referred to as *hiccup mode* which provides robust output short protection by providing time-average heating reduction of the output rectifier.

The bootstrap control logic disables most of the converter controller circuits except the V_B regulator and internal reference. Both GATE and GAT2 (assuming GAT2 is enabled) will be low when the converter is disabled. FRS, BLNK, and DT will be at ARTN while the V_C UVLO disables the converter. While the converter runs, FRS, BLNK, and DT will be about 1.25 V.

The startup current source transitions to a resistance as ($V_{VDD1} – V_{VC}$) falls below 7 V, but will start the converter from adapters within t_{ST}. The lower test voltage for t_{ST} was chosen based on an assumed adapter tolerance, but is not meant to imply a hard cutoff exists. Startup takes longer and eventually will not occur as V_{DD1} decreases below the test voltage. The bootstrap source provides reliable startup from widely varying input voltages, and eliminates the continual power loss of external resistors. The startup current source will not charge above the maximum recommended V_{VC} if the converter is disabled and there is sufficient V_{DD1} to charge higher.

Current Slope Compensation and Current Limit

Current-mode control requires addition of a compensation ramp to the sensed inductive (transformer or inductor) current for stability at duty cycles near and over 50%. The TPS23754 has a maximum duty cycle limit of 78%, permitting the design of wide input-range flyback and active clamp converters with a lower voltage stress on the output rectifiers. While the maximum duty cycle is 78%, converters may be designed that run at duty cycles well below this for a narrower, 36 V to 57 V PI range. The TPS23754 provides a fixed internal compensation ramp that suffices for most applications.

The TPS23754 provides internal, frequency independent, slope compensation (150 mV, V_{SLOPE}) to the PWM comparator input for current-mode control-loop stability. This voltage is not applied to the current-limit comparator whose threshold is 0.55 V (V_{CSMAX}). If the provided slope is not sufficient, the effective slope may be increased by addition of R_S per Figure 31. The additional slope voltage is provided by ($I_{SL-EX} \times R_S$). There is also a small dc offset caused by the ~2.5 µA pin current. The peak current limit does not have duty cycle dependency unless R_S is used. This makes it easier to design the current limit to a fixed value. See *Current Slope Compensation* for more information.

The internal comparators monitoring CS are isolated from the IC pin by the blanking circuits while GATE is low, and for a short time (blanking period) just after GATE switches high. A 440 Ω (max) equivalent pull down on CS is applied while GATE is low.

Blanking - R_{BLNK}

The TPS23754 provides a choice between internal fixed and programmable blanking periods. The blanking period is specified as an increase in the minimum GATE on time over the inherent gate driver and comparator delays. The default period (see the Electrical Characteristics table) is selected by connecting BLNK to RTN, and the programmable period is set with R_{BLNK}.

The TPS23754 blanker timing is precise enough that the traditional R-C filters on CS can be eliminated. This avoids current-sense waveform distortion, which tends to get worse at light output loads. There may be some situations or designers that prefer an R-C approach. The TPS23754 provides a pull-down on CS during the GATE off time to improve sensing when an R-C filter must be used. The CS input signal should be protected from nearby noisy signals like GATE drive and the switching MOSFET drain.

Dead Time

The TPS23754 features two switching MOSFET gate drivers to ease implementation of high-efficiency topologies. Specifically, these include active (primary) clamp topologies and those with synchronous drivers that are hard-driven by the control circuit. In all cases, there is a need to assure that both driven MOSFETs are not on at the same time. The DT pin programs a fixed time period delay between the turn-off of one gate driver until the turn-on of the next. This feature is an improvement over the repeatability and accuracy of discrete solutions while eliminating a number of discrete parts on the board. Converter efficiency is easily tuned with this one repeatable adjustment. The programmed dead time is the same for both GATE-to-GAT2 and GAT2-to-GATE transitions. The dead time is triggered from internal signals that are several stages back in the driver to eliminate the effects of gate loading on the period, however the observed and actual dead-time will be somewhat dependent on the gate loading. The turnoff of GAT2 coincides with the start of the internal clock period.

DT may be used to disable GAT2, which goes to a high-impedance state.

GATE's phase turns the main switch on when it transitions high, and off when it transitions low. GAT2's phase turns the second switch off when it transitions high, and on when it transitions low. Both switches should be off when GAT2 is high and GATE is low. The signal phasing is shown in Figure 2. Many topologies that use secondary-side synchronous rectifiers also use N-Channel MOSFETs driven through a gate-drive transformer. The proper signal phase for these rectifiers may be achieved by inverting the phasing of the secondary winding (swapping the leads). Use of the two gate drives is shown in Figure 1 and Figure 28.

FRS and Synchronization

The FRS pin programs the (free-running) oscillator frequency, and may also be used to synchronize the TPS23754 converter to a higher frequency. The internal oscillator sets the maximum duty cycle at 78% and controls the slope-compensation ramp circuit. Synchronization may be accomplished by applying a short pulse (T_{SYNC}) of magnitude V_{SYNC} to FRS as shown in Figure 30. The synchronization pulse terminates the potential on-time period, and the off-time period does not begin until the pulse terminates.

T2P, Startup and Power Management

T2P (type 2 PSE) is an active-low multifunction pin that indicates if

$$[(\text{PSE} = \text{Type\_2}) + (1.5\ \text{V} < V_{APD}) + (1.55\ \text{V} < V_{PPD} < 8.3\ \text{V})] \times (V_{CTL} < 4\ \text{V}) \times (\text{pd current limit} \neq \text{Inrush}).$$

The term with V_{CTL} prevents an optocoupler connected to the secondary-side from loading V_C before the converter is started. The APD and PPD terms allow the PD to operate from an adapter at high-power if a type 2 PSE is not present, assuming the adapter has sufficient capacity. Applications must monitor the state of T2P to detect power source transitions. Transitions could occur when a local power supply is added or dropped or when a PSE is enabled on the far end. The PD may be required to adjust the load appropriately. The usage of T2P is demonstrated in Figure 1.

In order for a type 2 PD to operate at less than 13 W the first 80 ms after power application, the various delays must be estimated and used by the application controller to meet the requirement. The bootup time of many applications processors may be long enough to eliminate the need to do any timing.

Thermal Shutdown

The dc/dc controller has an OTSD that can be triggered by heat sources including the V_B regulator, GATE driver, bootstrap current source, and bias currents. The controller OTSD turns off V_B, the GATE driver, and forces the V_C control into an under-voltage state.

Adapter ORing

Many PoE-capable devices are designed to operate from either a wall adapter or PoE power. A local power solution adds cost and complexity, but allows a product to be used if PoE is not available in a particular installation. While most applications only require that the PD operate when both sources are present, the TPS23754 supports forced operation from either of the power sources. Figure 27 illustrates three options for diode ORing external power into a PD. Only one option would be used in any particular design. Option 1 applies power to the TPS23754 PoE input, option 2 applies power between the TPS23754 PoE section and the power circuit, and option 3 applies power to the output side of the converter. Each of these options has advantages and disadvantages. Many of the basic ORing configurations and discussion contained in application note *Advanced Adapter ORing Solutions using the TPS23753* (literature number SLVA306A), apply to the TPS23754.

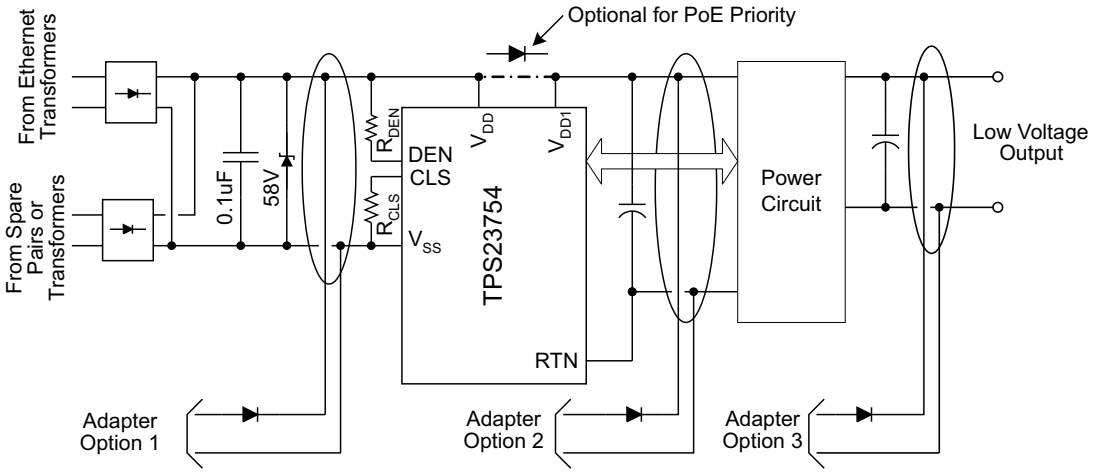


Figure 27. ORing Configurations

The IEEE standards require that the Ethernet cable be isolated from ground and all other system potentials. The adapter must meet a minimum 1500 Vac dielectric withstand test between the output and all other connections for ORing options 1 and 2. The adapter only needs this isolation for option 3 if it is not provided by the converter.

Adapter ORing diodes are shown for all the options to protect against a reverse voltage adapter, a short on the adapter input pins, and damage to a low-voltage adapter. ORing is sometimes accomplished with a MOSFET in option 3.

PPD ORing Features

The TPS23754 provides several additional features to ease ORing based on the multifunction PPD pin (not available on TPS23754-1). These include T2P signaling of an option 1 adapter, use of a 24 V adapter (reduced output power) for option 1, and use of PoE as a power backup in conjunction with option 2. See the *Advanced ORing Techniques* section.

ORing Challenges

Preference of one power source presents a number of challenges. Combinations of adapter output voltage (nominal and tolerance), power insertion point, and which source is preferred determine solution complexity. Several factors adding to the complexity are the natural high-voltage selection of diode ORing (the simplest method of combining sources), the current limit implicit in the PSE, and PD inrush and protection circuits (necessary for operation and reliability). Creating simple and seamless solutions is difficult if not impossible for many of the combinations. However the TPS23754 offers several built-in features that simplify some combinations.

Several examples will demonstrate the limitations inherent in ORing solutions. Diode ORing a 48 V adapter with PoE (option 1) presents the problem that either source might be higher. A blocking switch would be required to assure which source was active. A second example is combining a 12 V adapter with PoE using option 2. The converter will draw approximately four times the current at 12 V from the adapter than it does from PoE at 48 V. Transition from adapter power to PoE may demand more current than can be supplied by the PSE. The converter must be turned off while C_{IN} capacitance charges, with a subsequent converter restart at the higher voltage and lower input current. A third example is use of a 12 V adapter with ORing option 1. The PD hotswap would have to handle four times the current, and have 1/16 the resistance (be 16 times larger) to dissipate equal power. A fourth example is that MPS is lost when running from the adapter, causing the PSE to remove power from the PD. If ac power is then lost, the PD will stop operating until the PSE detects and powers the PD.

APPLICATION INFORMATION

The TPS23754 will support many power supply topologies that require a single PWM gate drive or two complementary gate drives and will operate with current-mode control. Figure 1 provides an example of an active clamp forward converter that uses the second gate driver to control M2, the active element in the clamp. GAT2 may also be used to drive a synchronous rectifier as demonstrated in Figure 28. The TPS23754 may be used in topologies that do not require GAT2, which may be disabled to reduce its idling loss.

Selecting a converter topology along with a design procedure is beyond the scope of this applications section. Examples to help in programming the TPS23754 are shown below. Additional special topics are included to explain the ORing capabilities, frequency dithering, and other design considerations.

For more specific converter design examples refer to the following application notes:

- Designing with the TPS23753 Powered Device and Power Supply Controller, SLVA305
- Designing for High Efficiency with the Active Clamp UCC2891 PWM Controller, SLUA303
- Advanced Adapter ORing Solutions using the TPS23753, SLVA306A
- TPS23754EVM-420 EVM: Evaluation Module for TPS23754, SLVU301
- TPS23754EVM-383 EVM: Evaluation Module for TPS23754, SLVU304

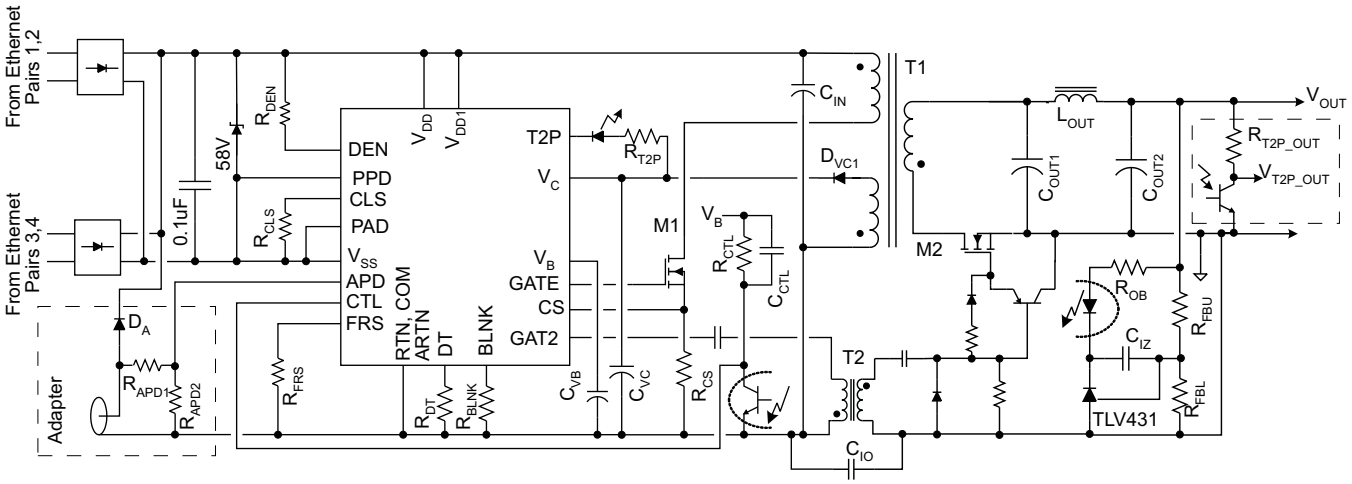


Figure 28. Driven Synchronous Flyback

Input Bridges and Schottky Diodes

Using Schottky diodes instead of PN junction diodes for the PoE input bridges and D_{VDD} will reduce the loss of this function by about 30%. There are however some things to consider when using them.

The IEEE standard specifies a maximum backfeed voltage of 2.8 V. A 100 kΩ resistor is placed between the unpowered pairs and the voltage is measured across the resistor. Schottky diodes often have a higher reverse leakage current than PN diodes, making this a harder requirement to meet. Use conservative design for diode operating temperature, select lower-leakage devices where possible, and match leakage and temperatures by using packaged bridges to help with this.

Schottky diode leakage current and lower dynamic resistance can impact the detection signature. Setting reasonable expectations for the temperature range over which the detection signature is accurate is the simplest solution. Increasing R_{DEN} slightly may also help meet the requirement.

Schottky diodes have proven less robust to the stresses of ESD transients, failing as a short or becoming leaky. Care must be taken to provide adequate protection in line with the exposure levels. This protection may be as simple as ferrite beads and capacitors.

A general recommendation for the input rectifiers are 1 A or 2 A, 100 V rated discrete or bridge diodes.

Protection, D1

A TVS, D_1, across the rectified PoE voltage per Figure 29 must be used. An SMAJ58A, or a part with equal to or better performance, is recommended for general indoor applications. If an adapter is connected from V_{DD1} to RTN, as in ORing option 2 above, voltage transients caused by the input cable inductance ringing with the internal PD capacitance can occur. Adequate capacitive filtering or a TVS must limit this voltage to be within the absolute maximum ratings. Outdoor transient levels or special applications require additional protection.

Use of diode D_{VDD} for PoE priority may dictate the use of additional protection around the TPS23754. ESD events between the PD power inputs, or the inputs and converter output, cause large stresses in the hotswap MOSFET if D_{VDD} becomes reverse biased and transient current around the TPS23754 is blocked. The use of C_{VDD} and D_{RTN} in Figure 29 provides additional protection should over-stress of the TPS23754 be an issue. An SMAJ58A would be a good initial selection for D_{RTN}. Individual designs may have to tune the value of C_{VDD}.

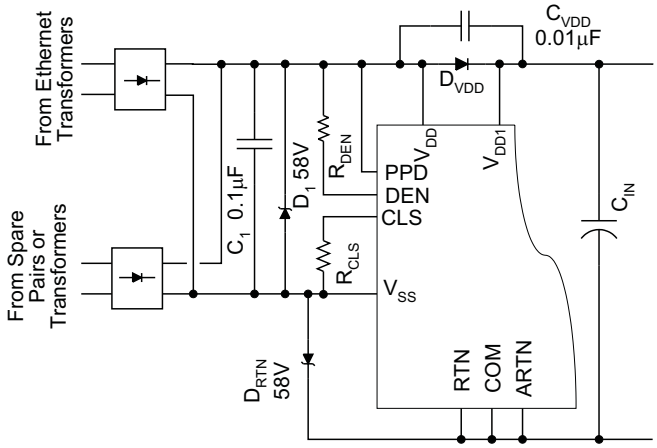


Figure 29. Example of Added ESD Protection for PoE Priority

Capacitor, C_1

The IEEE 802.3-2005 standard specifies an input bypass capacitor (from V_{DD} to V_{SS}) of 0.05 µF to 0.12 µF. Typically a 0.1 µF, 100 V, 10% ceramic capacitor is used.

Detection Resistor, R_{DEN}

The IEEE 802.3-2005 standard specifies a detection signature resistance, R_{DEN} between 23.75 kΩ and 26.25 kΩ, or 25 kΩ ± 5%. Choose an R_{DEN} of 24.9 kΩ.

Classification Resistor, R_{CLS}

Connect a resistor from CLS to V_{SS} to program the classification current according to the IEEE 802.3-2005 standard. The class power assigned should correspond to the maximum average power drawn by the PD during operation. Select R_{CLS} according to Table 1.

For a high power design, choose class 4 and R_{CLS} = 63.4 Ω.

APD Pin Divider Network, R_{APD1}, R_{APD2}

The APD pin can be used to disable the TPS23754 internal hotswap MOSFET giving the adapter source priority over the PoE source. An example calculation is provided, see literature number SLVA306A.

PPD Pin Divider Network, R_{PPD1}, R_{PPD2}

The PPD pin can be used to override the internal hotswap MOSFET UVLO (V_{UVLO_R} and V_{UVLO_H}) when using low voltage adapters connected between V_{DD} and V_{SS}. The PPD pin has an internal 5 µA pulldown current source. As an example, consider the choice of R_{PPD1} and R_{PPD2}, for a 24 V adapter.

1. Select the startup voltage, $V_{ADPTR-ON}$ approximately 75% of nominal for a 24 V adapter. Assuming that the adapter output is 24 V ± 10%, this provides 15% margin below the minimum adapter operating voltage.

2. Choose $V_{ADPTR-ON}$ = 24 V × 0.75 = 18 V
3. Choose R_{PPD2} = 3.01 kΩ
4. Calculate R_{PPD1}

a. $$R_{PPD1} = \left(\frac{V_{ADPTR\_ON} - V_{PPDEN}}{\frac{V_{PPDEN}}{R_{PPD2}} - I_{PPD}} \right) = \left(\frac{18\ V - 1.55\ V}{\frac{1.55\ V}{3.01\ k\Omega} - 5\ \mu A} \right) = 32.26\ k\Omega$$

b. Choose R_{PPD1} = 32.4 kΩ

5. Check PPD turn on and PPD turn off voltages

a. $$V_{ADPTR\_ON} = V_{PPDEN} + \left[R_{PPD1} \times \left(\frac{V_{PPDEN}}{R_{PPD2}} - I_{PPD} \right) \right] = 18.07\ V$$

b. $$V_{ADPTR\_OFF} = (V_{PPDEN} - V_{PPDH}) + \left[R_{PPD1} \times \left(\frac{(V_{PPDEN} - V_{PPDH})}{R_{PPD2}} - I_{PPD} \right) \right] = 14.54\ V$$

c. Voltages look acceptable.

6. Check PPD resistor power consumption.

a. $$P_{RPPD} = \frac{(V_{DD} - V_{SS})^2}{R_{PPD1} + R_{PPD2}} = \frac{(24\ V \times 1.1)^2}{3.01\ k\Omega + 32.4\ k\Omega} = 19.6\ mW$$

b. Power is acceptable, but resistor values could be increased to reduce the power loss.

Setting Frequency (R_{FRS}) and Synchronization

The converter switching frequency is set by connecting R_{FRS} from the FRS pin to ARTN. The frequency may be set as high as 1 MHz with some loss in programming accuracy as well as converter efficiency. Synchronization at high duty cycles may become more difficult above 500 kHz due to the internal oscillator delays reducing the available on-time. As an example:

1. Assume a desired switching frequency (f_{SW}) of 250 kHz.
2. Compute R_{FRS}:

a. $$R_{FRS}(k\Omega) = \frac{17250}{f_{SW}(kHz)} = \frac{17250}{250} = 69$$

b. Select 69.8 kΩ.

The TPS23754 may be synchronized to an external clock to eliminate beat frequencies from a sampled system, or to place emission spectrum away from an RF input frequency. Synchronization may be accomplished by applying a short pulse (T_{SYNC}) of magnitude V_{SYNC} to FRS as shown in Figure 30. R_{FRS} should be chosen so that the maximum free-running frequency is just below the desired synchronization frequency. The synchronization pulse terminates the potential on-time period, and the off-time period does not begin until the pulse terminates. The pulse at the FRS pin should reach between 2.5 V and V_B, with a minimum width of 22 ns (above 2.5 V) and rise/fall times less than 10 ns. The FRS node should be protected from noise because it is high-impedance. An R_T on the order of 100 Ω in the isolated example reduces noise sensitivity and jitter.

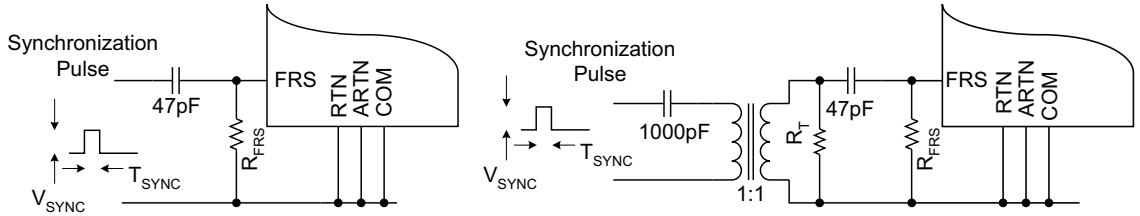


Figure 30. Synchronization

Current Slope Compensation

The TPS23754 provides a fixed internal compensation ramp that suffices for most applications. R_S (see Figure 31) may be used if the internally provided slope compensation is not enough.

Most current-mode control papers and application notes define the slope values in terms of V_{PP}/T_S (peak ramp voltage / switching period), however the electrical characteristics table specifies the slope peak (V_{SLOPE}) based on the maximum (78%) duty cycle. Assuming that the desired slope, $V_{SLOPE\text{-}D}$ (in mV/period), is based on the full period, compute R_S per the following equation where V_{SLOPE}, D_{MAX}, and $I_{SL\text{-}EX}$ are from the electrical characteristics table with voltages in mV, current in µA, and the duty cycle is unitless (e.g., D_{MAX} = 0.78).

$$R_S(\Omega) = \frac{\left[V_{SLOPE\_D}(mV) - \left(\frac{V_{SLOPE}(mV)}{D_{MAX}}\right)\right]}{I_{SL\_EX}(\mu A)} \times 1000$$

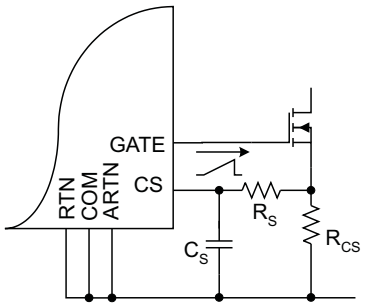


Figure 31. Additional Slope Compensation

C_S may be required if the presence of R_S causes increased noise, due to adjacent signals like the gate drive, to appear at the C_S pin.

Blanking Period, R_{BLNK}

Selection of the blanking period is often empirical because it is affected by parasitics and thermal effects of every device between the gate-driver and output capacitors. The minimum blanking period prevents the current limit and PWM comparators from being falsely triggered by the inherent current spike that occurs when the switching MOSFET turns on. The maximum blanking period is bounded by the output rectifier's ability to withstand the currents experienced during a converter output short.

If blanking beyond the internal default is desired choose R_{BLNK} using R_{BLNK} (kΩ) = t_{BLNK} (ns).

1. For a 100 ns blanking interval
   a. R_{BLNK} (kΩ) = 100
   b. Choose R_{BLNK} = 100 kΩ.

The blanking interval can also be chosen as a percentage of the switching period.

1. Compute R_{BLNK} as follows for 2% blanking interval in a switcher running at 250 kHz.
   a. $$R_{BLNK}(k\Omega) = \frac{Blanking\_Interval(\%)}{f_{SW}(kHz)} \times 10^4 = \frac{2}{250} \times 10^4 = 80$$
   b. Select R_{BLNK} = 80.6 kΩ.

Dead Time Resistor, R_{DT}

The required dead time period depends on the specific topology and parasitics. The easiest technique to obtain the optimum timing resistor is to build the supply and tune the dead time to achieve the best efficiency after considering all corners of operation (load, input voltage, and temperature). A good initial value is 100 ns. Program the dead time with a resistor connected from DT to ARTN per Equation 3.

1. Choose R_{DT} as follows assuming a t_{DT} of 100 ns:

a. $R_{DT}(k\Omega) = \frac{t_{DT}(ns)}{2} = \frac{100}{2} = 50$
b. Choose R_{DT} = 49.9 kΩ

Estimating Bias Supply Requirements and C_{VC}

The bias supply (V_C) power requirements determine the C_{VC} sizing and frequency of hiccup during a fault. The first step is to determine the power/current requirements of the power supply control, then use this to select C_{VC}. The control current draw will be assumed constant with voltage to simplify the estimate, resulting in an approximate value.

First determine the switching MOSFET gate drive power.

1. Let V_{QG} be the gate voltage swing that the MOSFET Q_G is rated to (often 10 V).
   a. $P_{GATE} = V_C \times f_{SW} \times \left(Q_{GATE} \times \frac{V_C}{V_{QG}}\right)$ $P_{GAT2} = V_C \times f_{SW} \times \left(Q_{GATE2} \times \frac{V_C}{V_{QG}}\right)$
   b. Compute gate drive power if V_C is 12 V, Q_{GATE} is 17 nC, and Q_{GAT2} is 8 nC.

      $P_{GATE} = 12\ V \times 250\ kHz \times 17\ nC \times \frac{12}{10} = 61.2\ mW$

   c. $P_{GAT2} = 12\ V \times 250\ kHz \times 8\ nC \times \frac{12}{10} = 28.8\ mW$

      $P_{DRIVE} = 61.2\ mW + 28.8\ mW = 90\ mW$
   d. This illustrates why MOSFET Q_G should be an important consideration in selecting the switching MOSFETs.
2. Estimate the required bias current at some intermediate voltage during the C_{VC} discharge. For the TPS23754, 12 V provides a reasonable estimate. Add the operating bias current to the gate drive current.
   a. $I_{DRIVE} = \frac{P_{DRIVE}}{V_C} = \frac{90\ mW}{12\ V} = 7.5\ mA$
   b. $I_{TOTAL} = I_{DRIVE} + I_{OPERATING} = 7.5\ mA + 0.92\ mA = 8.42\ mA$
3. Compute the required C_{VC} based on startup within the typical softstart period of 4 ms.
   a. $C_{VC1} + C_{VC2} = \frac{T_{STARTUP} \times I_{TOTAL}}{V_{CUVH}} = \frac{4\ ms \times 8.42\ mA}{6.5\ V} = 5.18\ \mu F$
   b. For this case, a standard 10 µF electrolytic plus a 0.47 µF should be sufficient.
4. Compute the initial time to start the converter when operating from PoE.
   a. Using a typical bootstrap current of 4 mA, compute the time to startup.
   b. $T_{ST} = \frac{C_{VC1} \times V_{CUV}}{I_{VC}} = \frac{10.47\ \mu F \times 15\ V}{4\ mA} = 39\ ms$
5. Compute the fault duty cycle and hiccup frequency
   a. $T_{RECHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{VC}} = \frac{(10\ \mu F + 0.47\ \mu F) \times 6.5\ V}{4\ mA} = 17\ ms$
   b. $T_{DISCHARGE} = \frac{(C_{VC1} + C_{VC2}) \times V_{CUVH}}{I_{TOTAL}} = \frac{(10\ \mu F + 0.47\ \mu F) \times 6.5V}{8.42\ mA} = 8.08\ ms$
      a. Note that the optocoupler current is 0 mA because the output is in current limit.
      b. Also, it is assumed I_{T2P} is 0 mA.
   c. Duty Cycle: $D = \frac{T_{DISCHARGE}}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{8.08\ ms}{8.08\ ms + 17\ ms} = 32\%$
   d. Hiccup Frequency: $F = \frac{1}{T_{DISCHARGE} + T_{RECHARGE}} = \frac{1}{8.08\ ms + 17\ ms} = 39.9\ Hz$
6. With the TPS23754, the voltage rating of C_{VC1} and C_{VC2} should be 25 V minimum while with the TPS23756 the rating can be 16 V.

Switching Transformer Considerations and R_{VC}

Care in design of the transformer and V_C bias circuit is required to obtain hiccup overload protection. Leading-edge voltage overshoot on the bias winding may cause V_C to peak-charge, preventing the expected tracking with output voltage. Some method of controlling this is usually required. This may be as simple as a series resistor, or an R-C filter in front of D_{VC1}. Good transformer bias-to-output-winding coupling results in reduced overshoot and better voltage tracking.

R_{VC} as shown in Figure 32 helps to reduce peak charging from the bias winding. This becomes especially important when tuning hiccup mode operation during output overload. Typical values for R_{VC} will be between 10 Ω and 100 Ω.

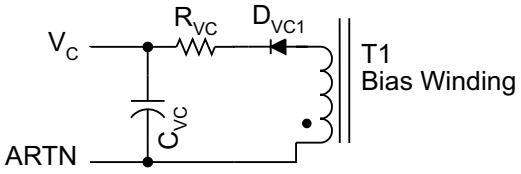


Figure 32. R_{VC} Usage

T2P Pin Interface

The T2P pin is an active low, open-drain output indicating a high power source is available. An optocoupler is typically used to interface with the T2P pin to signal equipment on the secondary side of the converter of T2P status. Optocoupler current-gain is referred to as CTR (current transfer ratio), which is the ratio of transistor collector current to LED current. To preserve efficiency, a high-gain optocoupler (250% ≤ CTR ≤ 500%, or 300% ≤ CTR ≤ 600%) along with a high-impedance (e.g., CMOS) receiver are recommended. Design of the T2P optocoupler interface can be accomplished as follows:

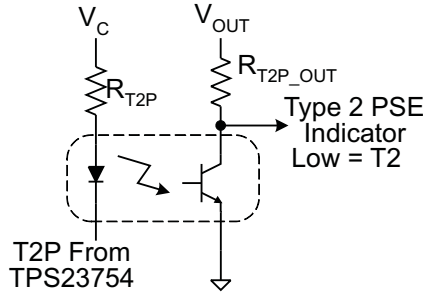


Figure 33. T2P Interface

1. T2P ON characteristic: I_{T2P} = 2 mA minimum, V_{T2P} = 1 V
2. Let V_C = 12 V, V_{OUT} = 5 V, $R_{T2P\text{-}OUT}$ = 10 kΩ, $V_{T2P\text{-}OUT}$ (low) = 400 mV max
   a. $$I_{RT2P\text{-}OUT} = \frac{V_{OUT} - V_{T2P\text{-}OUT}(low)}{R_{T2P\text{-}OUT}} = \frac{5 - 0.4}{10000} = 0.46\ mA$$
3. The optocoupler CTR will be needed to determine R_{T2P}. A device with a minimum CTR of 300% at 5 mA LED bias current is selected. CTR will also vary with temperature and LED bias current. The strong variation of CTR with diode current makes this a problem that requires some iteration using the CTR versus I_{DIODE} curve on the optocoupler data sheet.
   a. Using the (normalized) curves, a current of 0.4 mA to 0.5 mA is required to support the output current at the minimum CTR at 25°C.
      a. Pick an I_{DIODE}. For example one around the desired load current.
      b. Use the optocoupler datasheet curve to determine the effective CTR at this operating current. It is usually necessary to apply the normalized curve value to the minimum specified CTR. It might be necessary to ratio or offset the curve readings to obtain a value that is relative to the current that the CTR is specified at.
      c. If $I_{DIODE} \times CTR_{I\_DIODE}$ is substantially different from I_{RT2P_OUT}, choose another I_{DIODE} and repeat.
   b. This manufacturer's curves also indicate a –20% variation of CTR with temperature. The approximate

forward voltage of the optocoupler diode is 1.1 V from the data sheet.

$$I_{RT2P} \cong I_{MIN} \times \frac{100}{100 - \Delta CTR_{TEMP}} = 0.5\ mA \times \frac{100}{100 - 20} = 0.625\ mA$$

c. $V_{FLED} \approx 1.1\ V$

$$R_{T2P} = \frac{V_C - V_{T2P} - V_{FLED}}{I_{RT2P}} = \frac{12 - 1 - 1.1}{0.625\ mA} = 15.48\ k\Omega$$

d. Select a 15.4 kΩ resistor. Even though the minimum CTR and temperature variation were considered, the designer might choose a smaller resistor for a little more margin.

Advanced ORing Techniques

See *Advanced Adapter ORing Solutions using the TSP23753*, TI document number SLVA306A for ORing applications that also work with the TPS23754. The material in sections *Adapter ORing* and *Protection, D1* are important to consider as well. The following applications are unique to the TPS23754 with the introduction of PPD.

Option 2 ORing with PoE acting as a hot backup is eased by connecting PPD to V_{DD} per Figure 34. This PPD connection enables the class regulator even when APD is high. The R-Zener network (1.8 kΩ – 24 V) is the simplest circuit that will satisfy MPS requirements, keeping the PSE online. This network may be switched out when the APD is not powered with an optocoupler. This works best with a 48-V adapter and the APD-programmed threshold as high as possible. An example of an adapter priority application with smooth switchover between a 48 V adapter and PoE is shown on the right side of Figure 34. D_{APD} is used to reduce the effective APD hysteresis, allowing the PSE to power the load before V_{VDD1}-V_{RTN} falls too low and causes a hotswap foldback.

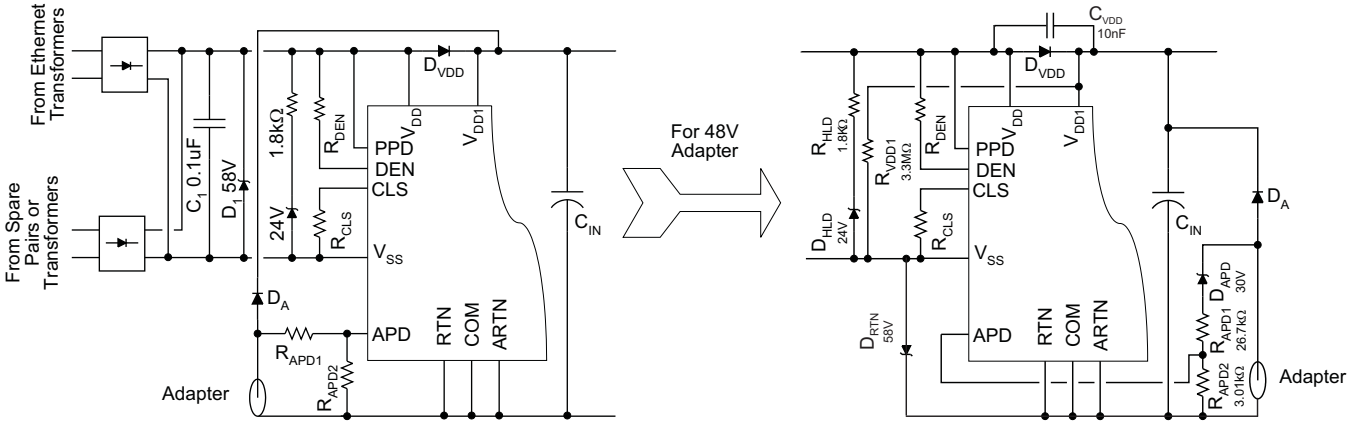


Figure 34. Option 2 PoE Backup ORing

Option 1 ORing of a low voltage adapter (e.g., 24 V) is possible by connecting a resistor divider to PPD as in Figure 35. When 1.55 V ≤ V_{PPD} ≤ 8.3 V, the hotswap MOSFET is enabled, T2P is activated, and the class feature is disabled. The hotswap current limit is unaffected, limiting the available power. For example, the maximum input power from a 24 V adapter would be 19.3 W [(24 V – 0.6 V) × 0.825 A].

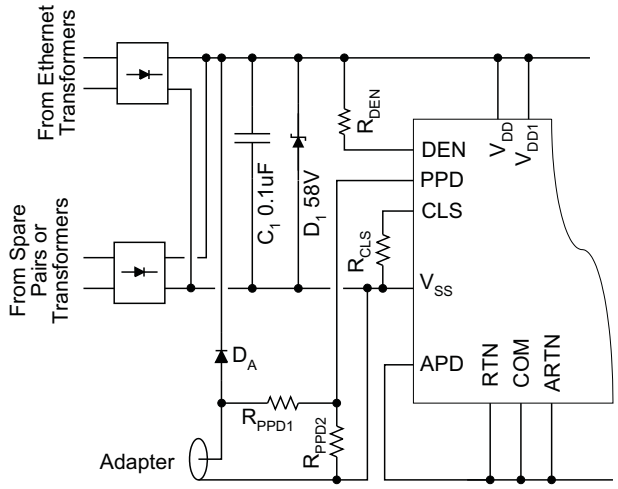


Figure 35. Low-Voltage Option 1 ORing

Softstart

Converters require a softstart on the voltage error amplifier to prevent output overshoot on startup. Figure 36 shows a common implementation of a secondary-side softstart that works with the typical TL431 error amplifier. The softstart components consist of D_{SS}, R_{SS}, and C_{SS}. They serve to control the output rate-of-rise by pulling V_{CTL} down as C_{SS} charges through R_{OB}, the optocoupler, and D_{SS}. This has the added advantage that the TL431 output and C_{IZ} are preset to the proper value as the output voltage reaches the regulated value, preventing voltage overshoot due to the error amplifier recovery. The secondary-side error amplifier will not become active until there is sufficient voltage on the secondary. The TPS23754 provides a primary-side softstart which persists long enough (~4 ms) for secondary side voltage-loop softstart to take over. The primary-side current-loop softstart controls the switching MOSFET peak current by applying a slowly rising ramp voltage to a second PWM control input. The PWM is controlled by the lower of the softstart ramp or the CTL-derived current demand. The actual output voltage rise time is usually much shorter than the internal softstart period. Initially the internal softstart ramp limits the maximum current demand as a function of time. Either the current limit, secondary-side softstart, or output regulation assume control of the PWM before the internal softstart period is over. Figure 25 shows a smooth handoff between the primary and secondary-side softstart with minimal output voltage overshoot.

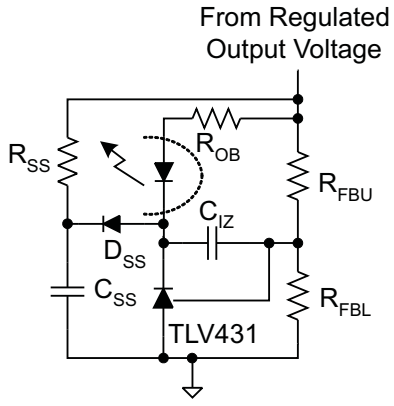


Figure 36. Error Amplifier Soft Start

Special Switching MOSFET Considerations

Special care must be used in selecting the converter switching MOSFET. The TPS23756 minimum switching MOSFET V_{GATE} is ~5.5 V, which is due to the V_C lower threshold. This will occur during an output overload, or towards the end of a (failed) bootstrap startup. The MOSFET must be able to carry the anticipated peak fault current at this gate voltage.

Thermal Considerations and OTSD

Sources of nearby local PCB heating should be considered during the thermal design. Typical calculations assume that the TPS23754 is the only heat source contributing to the PCB temperature rise. It is possible for a normally operating TPS23754 device to experience an OTSD event if it is excessively heated by a nearby device.

Frequency Dithering for Conducted Emissions Control

The international standard CISPR 22 (and adopted versions) is often used as a requirement for conducted emissions. Ethernet cables are covered as a telecommunication port under section 5.2 for conducted emissions. Meeting EMI requirements is often a challenge, with the lower limits of Class B being especially hard. Circuit board layout, filtering, and snubbing various nodes in the power circuit are the first layer of control techniques. A more detailed discussion of EMI control is presented in *Practical Guidelines to Designing an EMI Compliant PoE Powered Device With Isolated Flyback,* TI literature number SLUA469. Additionally, IEEE802.3-2005 sections 33.3 and 33.4 have requirements for noise injected onto the Ethernet cable based on compatibility with data transmission.

Occasionally, a technique referred to as frequency dithering is utilized to provide additional EMI measurement reduction. The switching frequency is modulated to spread the narrowband individual harmonics across a wider bandwidth, thus lowering peak measurements. The circuit of Figure 37 modulates the switching frequency by feeding a small ac signal into the FRS pin. These values may be adapted to suit individual needs.

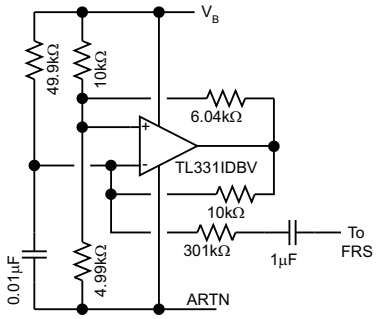


Figure 37. Frequency Dithering

ESD

The TPS23754 has been tested to EN61000-4-2 using a power supply based on Figure 1. The levels used were 8 kV contact discharge and 15 kV air discharge. Surges were applied between the PoE input and the dc output, between the adapter input and the dc output, between the adapter and the PoE inputs, and to the dc output with respect to earth. Tests were done both powered and unpowered. No TPS23754 failures were observed and operation was continuous. See Figure 29 for additional protection for some test configurations.

ESD requirements for a unit that incorporates the TPS23754 have a much broader scope and operational implications than are used in TI's testing. Unit-level requirements should not be confused with reference design testing that only validates the ruggedness of the TPS23754.

Layout

Printed circuit board layout recommendations are provided in the evaluation module (EVM) documentation available for these devices.

Changes from Revision A (April 2009) to Revision B **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS23754PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS23754PWP-1	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS23754PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS23754PWPR-1	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS23756PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS23756PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

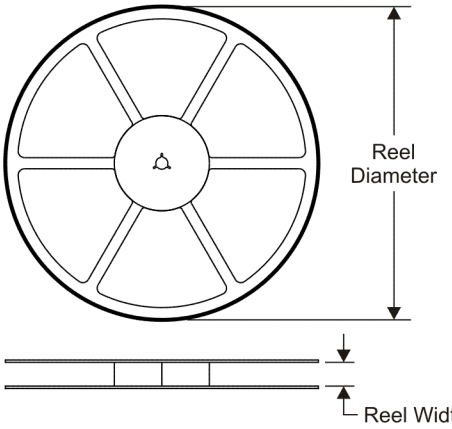
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

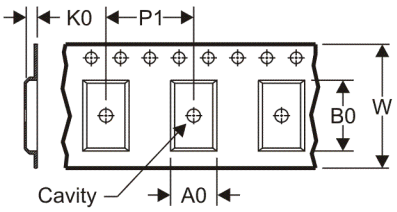
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

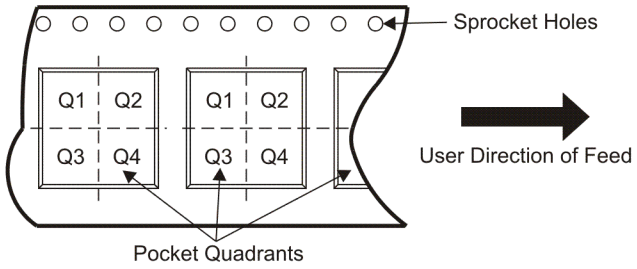


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

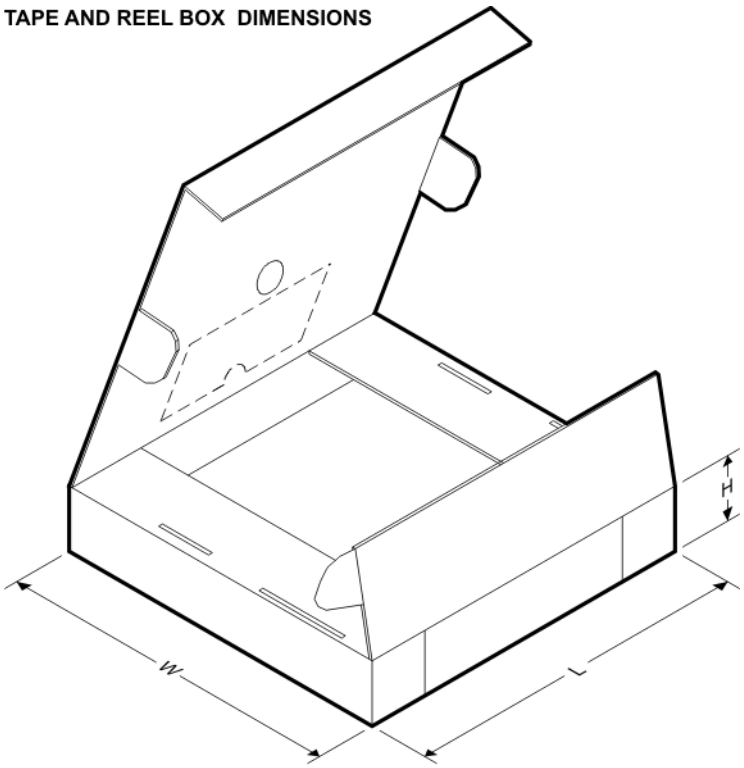
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23754PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS23754PWPR-1	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
TPS23756PWPR	HTSSOP	PWP	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

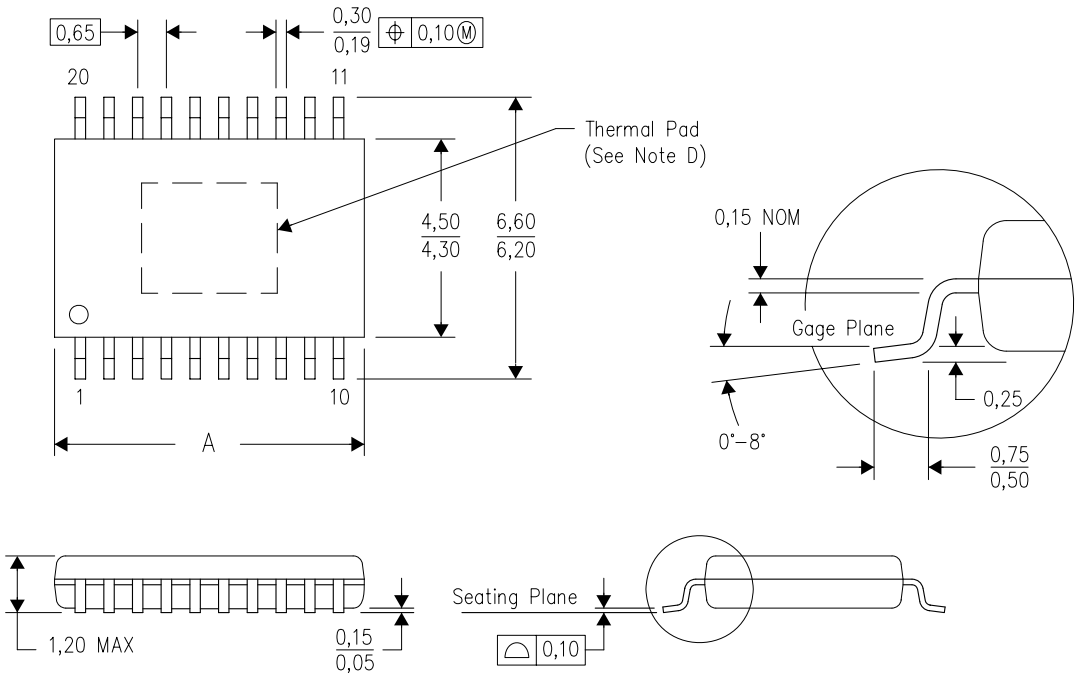


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23754PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS23754PWPR-1	HTSSOP	PWP	20	2000	346.0	346.0	33.0
TPS23756PWPR	HTSSOP	PWP	20	2000	346.0	346.0	33.0

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

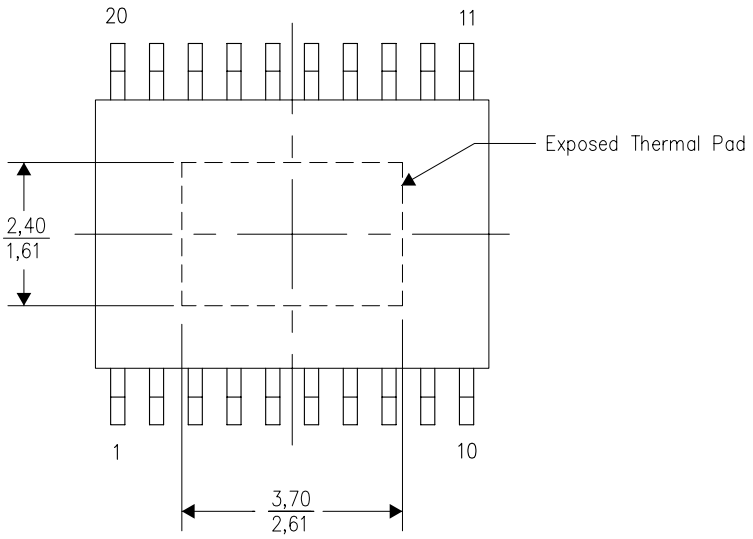
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

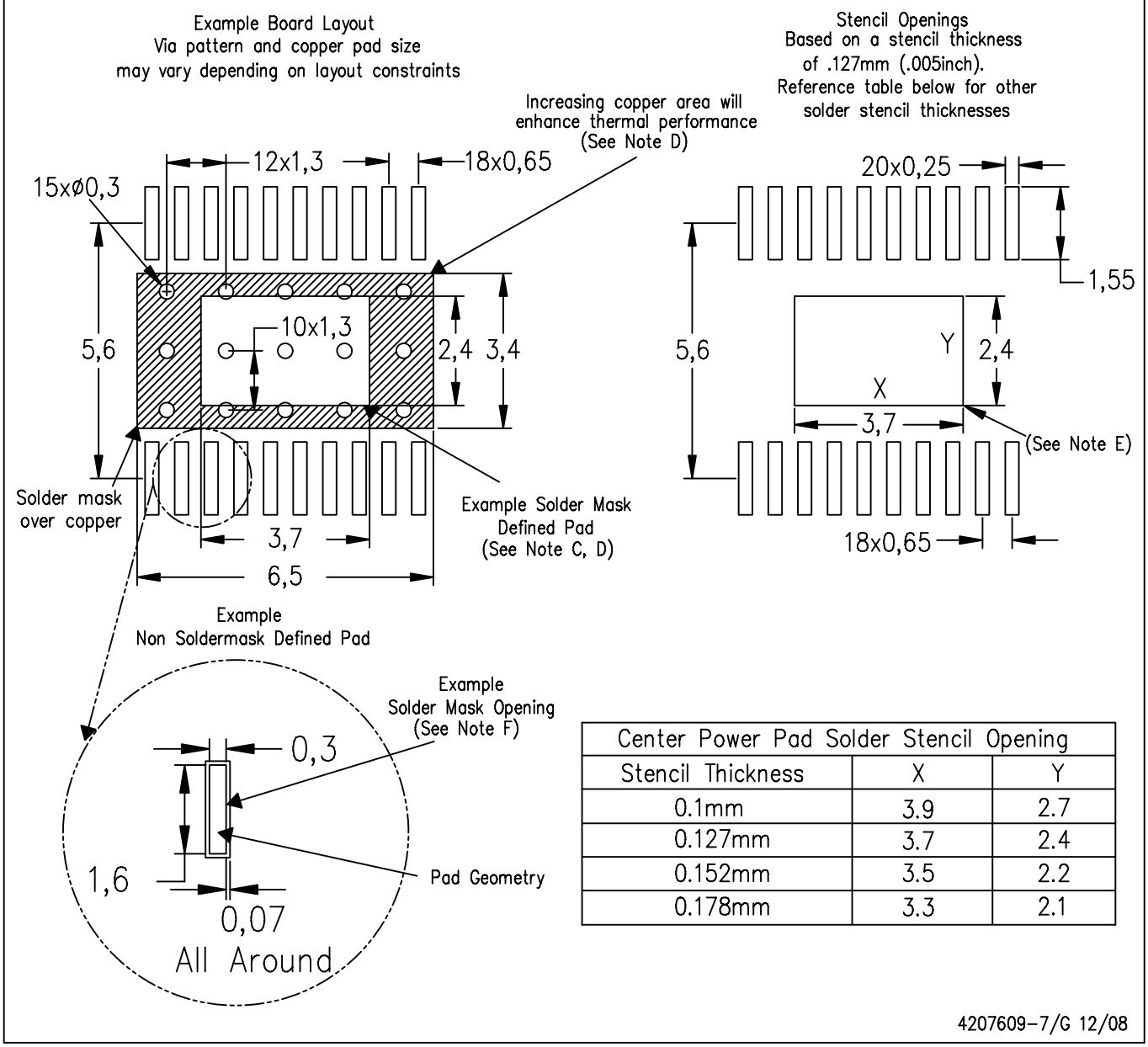


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G20) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.9	2.7
0.127mm	3.7	2.4
0.152mm	3.5	2.2
0.178mm	3.3	2.1

4207609–7/G 12/08

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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