

Dual N-channel Enhancement Mode Power MOSFET

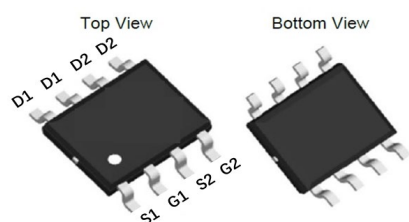
Features

- $V_{DS} = 20V$, $I_D = 6A$
 $R_{DS(ON)} < 21\text{ m}\Omega$ @ $V_{GS} = 10V$
 $R_{DS(ON)} < 25\text{ m}\Omega$ @ $V_{GS} = 4.5V$

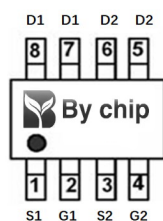
General Features

- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead Free and Green Available

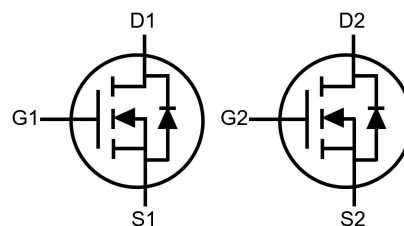
100% UIS TESTED!
100% ΔV_{ds} TESTED!



SOP-8 (Dual)



Pin Assignment



Schematic diagram

Absolute Maximum Ratings (@ $T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Units
V_{DS}	Drain-to-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D	Continuous Drain Current	$T_A = 25^\circ\text{C}$	A
		$T_A = 100^\circ\text{C}$	
I_{DM}	Pulsed Drain Current ⁽¹⁾	24	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	7.5	mJ
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	75	$^\circ\text{C/W}$
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Electrical Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0V	20	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 20V, V _{GS} = 0V	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	V _{DS} = 0V, V _{GS} = ±12V	-	-	±100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	0.5		1.5	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	V _{GS} = 4.5V, I _D = 6A	-		21	mΩ
		V _{GS} = 2.5V, I _D = 5A	-		25	mΩ
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 10V, f = 1MHz	-	455	-	pF
C _{oss}	Output Capacitance		-	64	-	pF
C _{rss}	Reverse Transfer Capacitance		-	55	-	pF
Q _g	Total Gate Charge	V _{GS} = 0 to 4.5V V _{DD} = 10V, I _D = 2A	-	6	-	nC
Q _{gs}	Gate Source Charge		-	1	-	nC
Q _{gd}	Gate Drain("Miller") Charge		-	1.5	-	nC
Switching Characteristics						
t _{d(on)}	Turn-On DelayTime	V _{GS} = 4.5V, V _{DD} = 10V I _D = 2A, R _{GEN} = 3Ω	-	4	-	ns
t _r	Turn-On Rise Time		-	13	-	ns
t _{d(off)}	Turn-Off DelayTime		-	65	-	ns
t _f	Turn-Off Fall Time		-	33	-	ns
Drain-Source Diode Characteristics and Max Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	24	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _S = 6A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I _F = 2A, di/dt = 60A/us	-	6	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	0.8	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. EAS condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 10\text{V}$, $V_G = 10\text{V}$, $R_G = 25\Omega$, $L = 0.5\text{mH}$, $I_{AS} = 5.5\text{A}$
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.

Typical Performance Characteristics

Figure 1: Output Characteristics

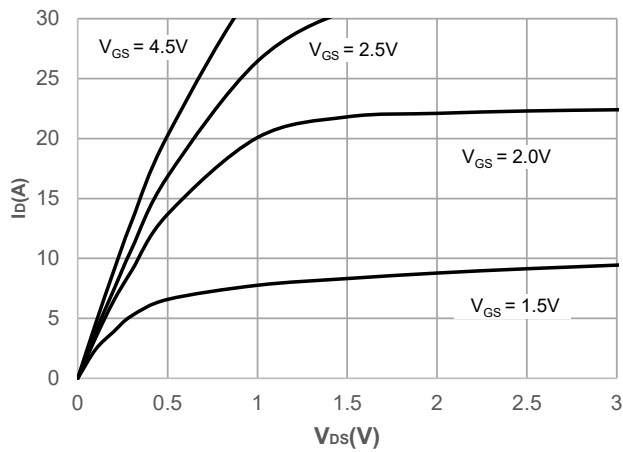


Figure 2: Typical Transfer Characteristics

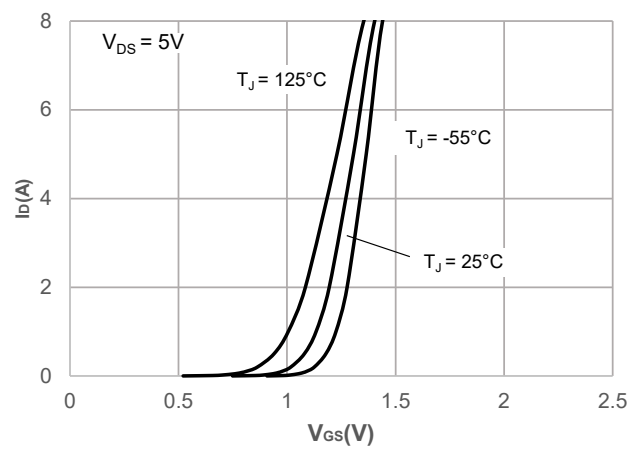


Figure 3: On-resistance vs. Drain Current

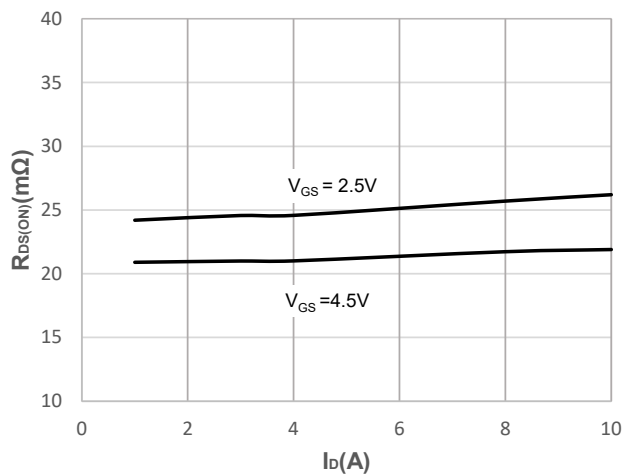


Figure 4: Body Diode Characteristics

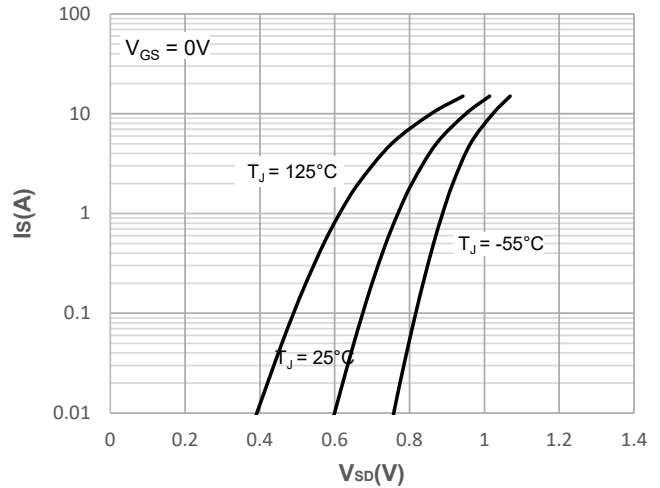


Figure 5: Gate Charge Characteristics

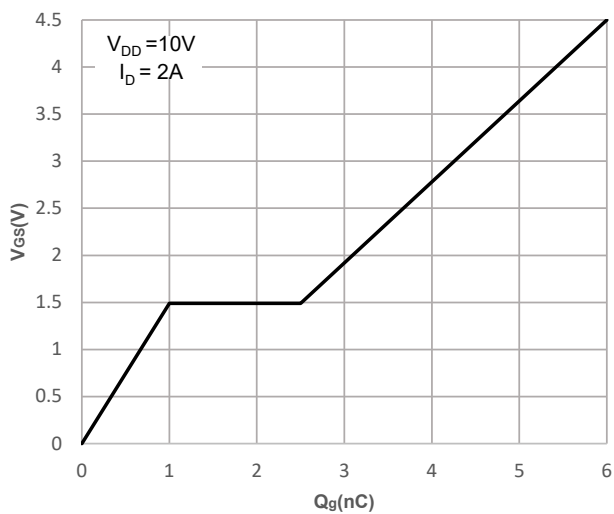
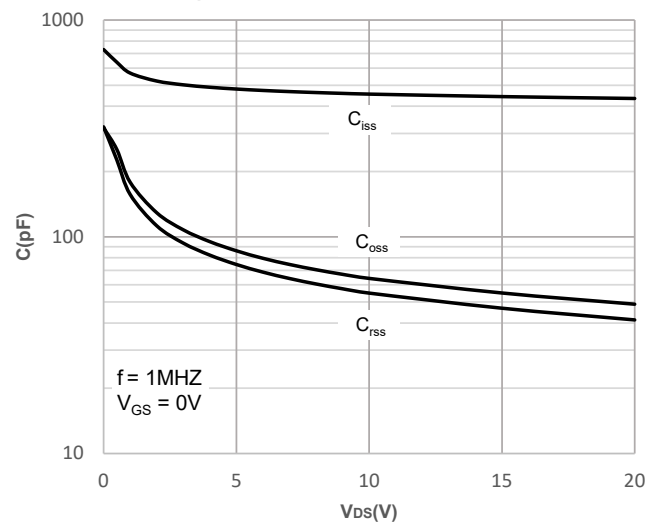


Figure 6: Capacitance Characteristics



Typical Performance Characteristics

Figure 7: Normalized Breakdown voltage vs. Junction Temperature

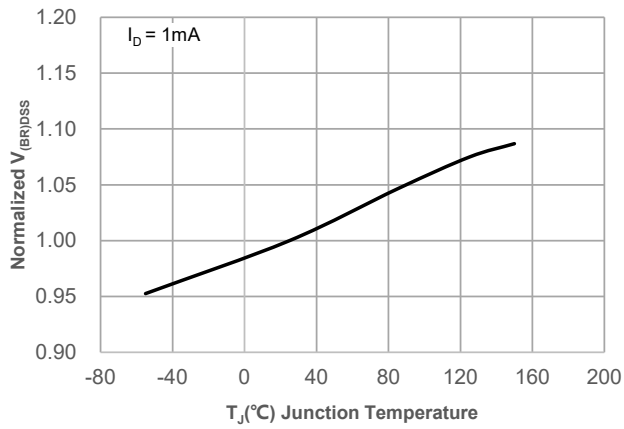


Figure 8: Normalized on Resistance vs. Junction Temperature

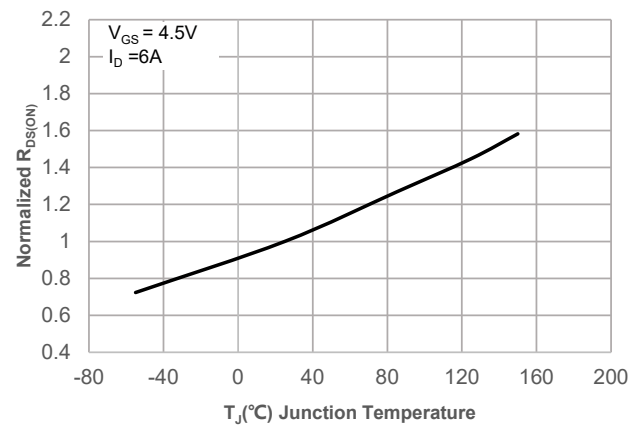


Figure 9: Maximum Safe Operating Area

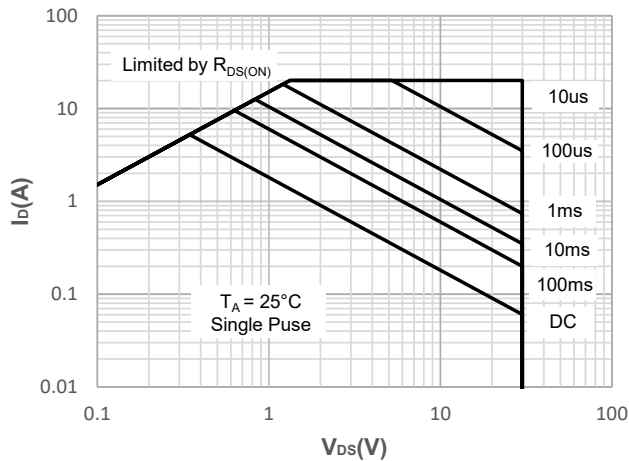


Figure 10: Maximum Continuous Drian Current vs. Ambient Temperature

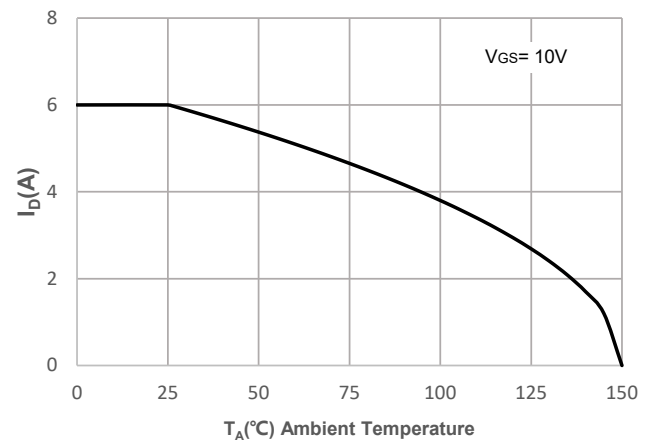


Figure 11: Normalized Maximum Transient Thermal Impedance

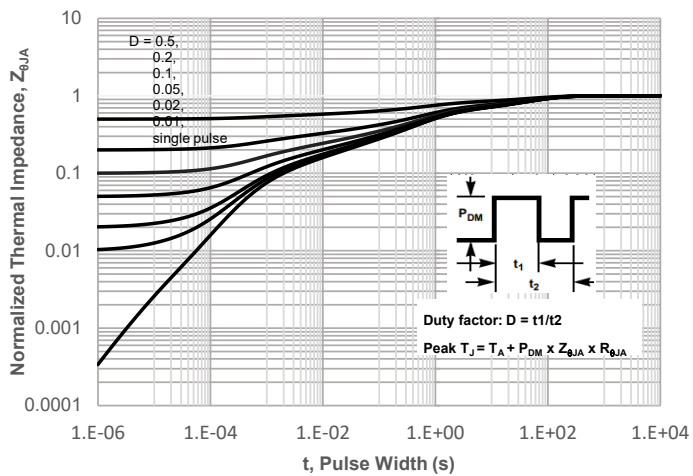
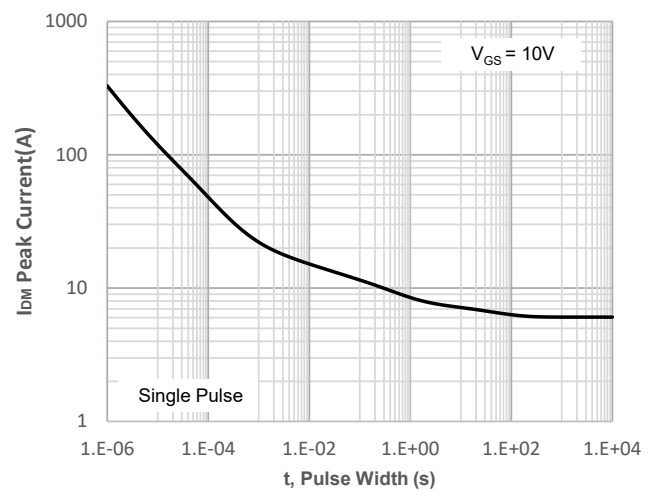


Figure 12: Peak Current Capacity



Test Circuit

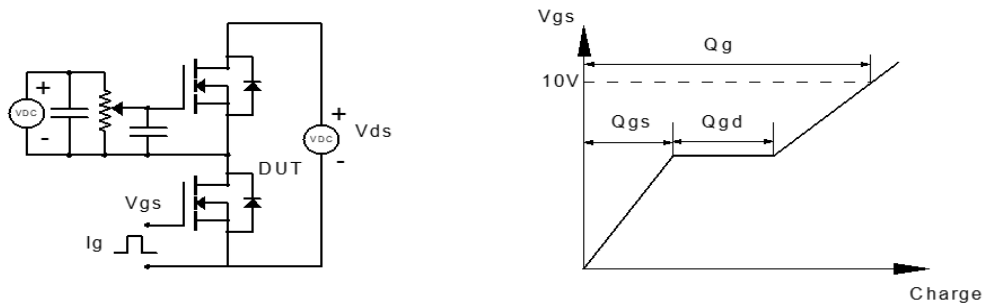


Figure 1: Gate Charge Test Circuit & Waveform

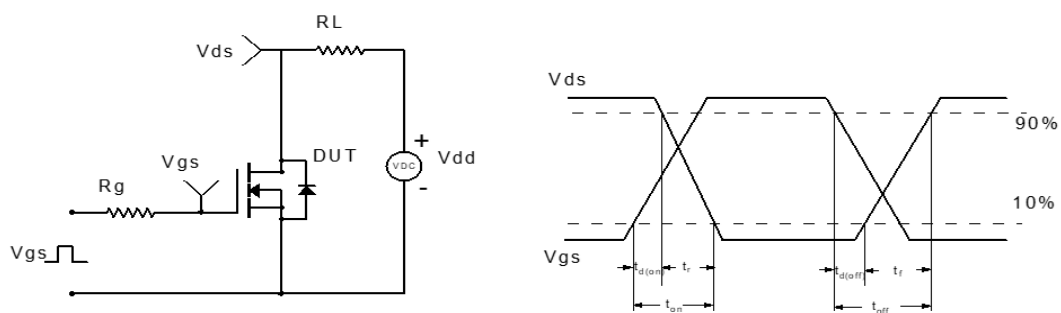


Figure 2: Resistive Switching Test Circuit & Waveform

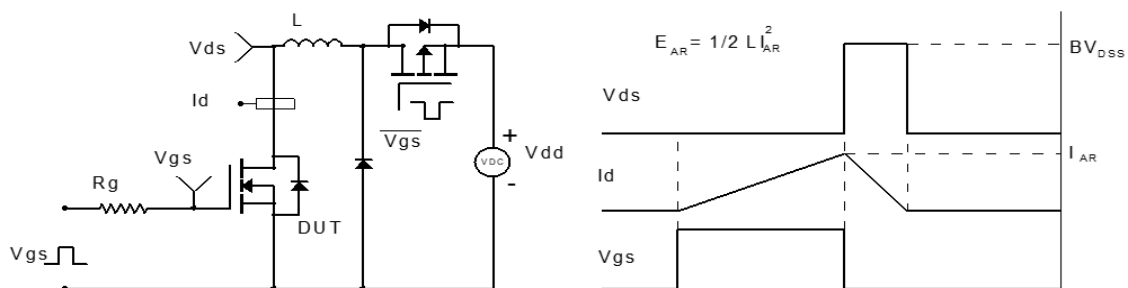


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

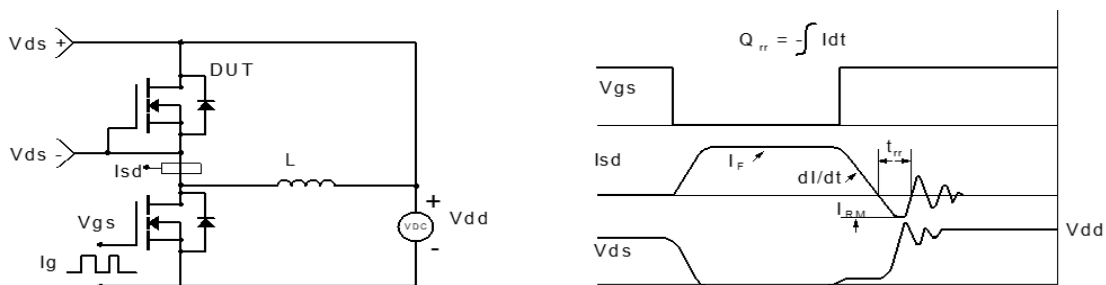


Figure 4: Diode Recovery Test Circuit & Waveform