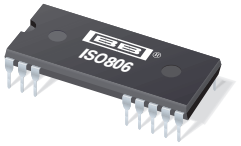
BURR - BROWN®



ISO806

Isolated 12-Bit Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- 1500Vrms ISOLATION CONTINUOUS
- 25μS CONVERSION TIME
- 12-BIT SERIAL OUTPUT
- SINGLE +5V SUPPLY
- 28-PIN 0.6" PLASTIC DIP

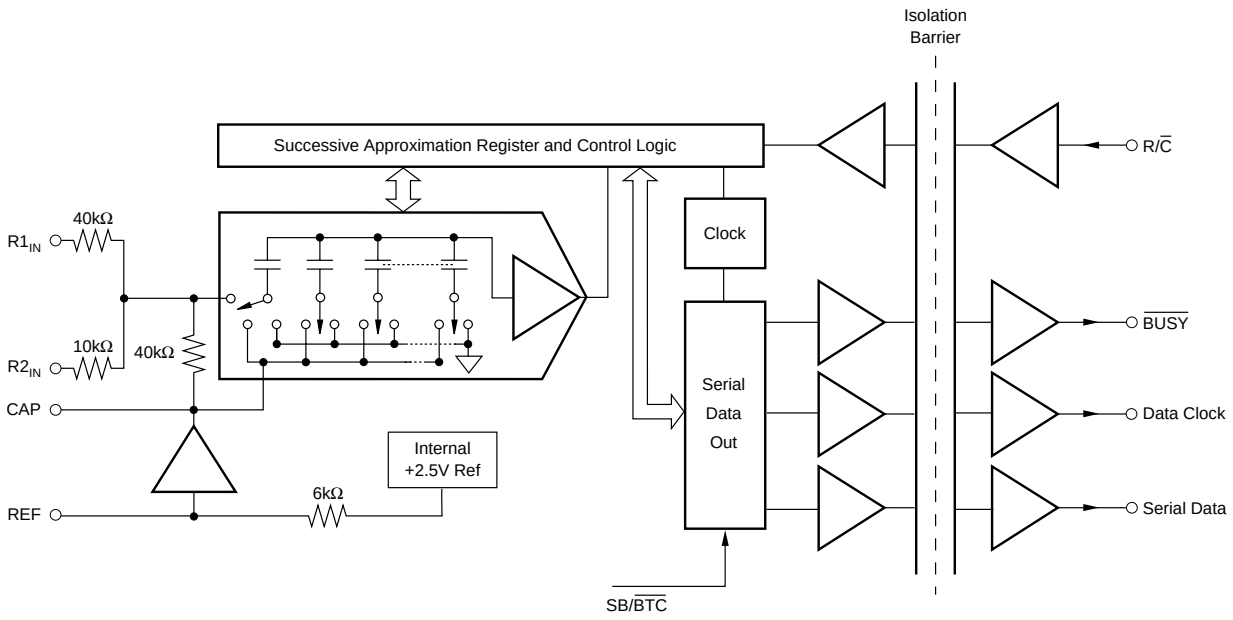
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- PC-BASED DATA ACQUISITION TEST EQUIPMENT

DESCRIPTION

The ISO806 is a low-power isolated sampling ADC using state-of-the-art CMOS structures and high voltage capacitors. The ISO806 contains a complete 12-bit capacitor based SAR, ADC with S/H, clock, reference, μP interface, serial out and galvanic isolation.

Laser-trimmed scaling resistors provide standard industrial input ranges including ±10V, ±5V, 0-5V, 0-4V. They are available in 28-pin 0.6" wide plastic DIP and are specified over the industrial temperature range of –40°C to +85°C.



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Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

Printed in U.S.A. August, 1997

SPECIFICATIONS

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

PARAMETER	CONDITIONS	ISO806P MIN	ISO806P TYP	ISO806P MAX	UNITS
ISOLATION PARAMETERS					
Rated Voltage, Continuous	50Hz	1500			Vrms
Partial Discharge, 100% Test[8]	1s, 5pC	2500			Vrms
Creepage Distance (External) DIP = "P" Package			16		mm
Internal Isolation Distance			0.10		mm
Barrier Impedance			$>10^{13}$ II 15		Ω II pF
Leakage Current[9]	240Vrms, 60Hz			1.7	μArms
	240Vrms, 50Hz			1.4	μArms
RESOLUTION				12	Bit
ANALOG INPUT					
Voltage Ranges			±10, 0 to +5, 0 to +4		V
Impedance			(See Table II)		
Capacitance			35		pF
THROUGHPUT SPEED					
Conversion Time				20	μs
Complete Cycle	Acquire and Convert			25	μs
Throughput Rate		40			kHz
DC ACCURACY					
Integral Linearity Error			±0.15	±0.9	LSB[1]
Differential Linearity Error			±0.15	±0.9	LSB
No Missing Codes			Guaranteed		Bits
Transition Noise[2]			0.1		LSB
Full Scale Error[3,4]				±0.5	%
Full Scale Error Drift			±7		ppm/°C
Full Scale Error Drift	Ext. 2.5000V Ref		±0.5		ppm/°C
Bipolar Zero Error[3]	±10V Range			±10	mV
Bipolar Zero Error Drift	±10V Range		±0.5		ppm/°C
Unipolar Zero Error[3]	0V to 5V, 0V to 4V Ranges			±3	mV
Unipolar Zero Error Drift	0V to 5V, 0V to 4V Ranges		±0.5		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_S)	+4.75V < V_S < +5.25V			±0.5	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 1kHz, ±10V		90		dB[5]
Total Harmonic Distortion	f_{IN} = 1kHz, ±10V		–90		dB
Signal-to-(Noise+Distortion)	f_{IN} = 1kHz, ±10V		73		dB
Signal-to-Noise	f_{IN} = 1kHz, ±10V		73		dB
Useable Bandwidth[6]			130		kHz
SAMPLING DYNAMICS					
Aperture Delay			40		ns
Aperture Jitter			20		ps
Overvoltage Recovery[7]			750		ns
REFERENCE					
Internal Reference Voltage	No Load	2.48	2.5	2.52	V
Internal Reference Source Current			1		μA
(Must use external buffer.)					
Internal Reference Drift			8		ppm/°C
External Reference Voltage Range		2.3	2.5	2.7	V
for Specified Linearity					
External Reference Current Drain	Ext. 2.5000V Ref			100	μA
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		1.0	V
V_{IH}		V_D –1.0		V_D +0.3V	V
I_{IL}	V_{IL} = 0V			±10	μA
I_{IH}	V_{IH} = 5V			±10	μA
DIGITAL OUTPUTS					
Data Coding			Binary Two's Complement or Straight Binary		
V_{OL}	I_{SINK} = 1.6mA			0.4	V
V_{OH}	I_{SOURCE} = 500μA	+4			V

SPECIFICATIONS (CONT)

ELECTRICAL

At T_A = –40°C to +85°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

PARAMETER	CONDITIONS	ISO806P MIN	ISO806P TYP	ISO806P MAX	UNITS
POWER SUPPLIES					
Specified Performance					
V_{DIG1}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	V
V_{DIG2}		+4.75		+5.25	V
I_{DIG1}			4.2		mA
I_{ANA}			5.0		mA
I_{DIG2}			10.8		mA
Power Dissipation	V_{ANA} = V_{DIG} = 5V, F_S = 40kHz		125		mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance, θ_{JA}					
Plastic DIP			75		°C/W

NOTES: (1) LSB means Least Significant Bit. One LSB for the ±10V input range is 4.88mV. (2) Typical rms noise at worst case transition. (3) As measured with fixed resistors shown in Figure 7b. Adjustable to zero with external potentiometer. (4) Full scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. (5) All specifications in dB are referred to a full-scale input. (6) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB. (7) Recovers to specified performance after 2 x FS input overvoltage. (8) All devices receive a 1s test. Failure criterion is ≥ 5 pulses of ≥ 5pC. (9) Tested at 2500Vrms, 50Hz limit 10µA.

ABSOLUTE MAXIMUM RATINGS

Analog Inputs: $R1_{IN}$	±25V
$R2_{IN}$	±25V
CAP	V_{ANA} +0.3V to AGND2 –0.3V
REF	Indefinite Short to AGND2, Momentary Short to V_{ANA}
Ground Voltage Differences: DGND and AGND1	±0.3V
DGND, AGND, and GND_{ISO}	1563Vrms
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to V_{DIG} +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

PACKAGE INFORMATION

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER(1)
ISO806P	Plastic DIP	215-1

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet published specifications.

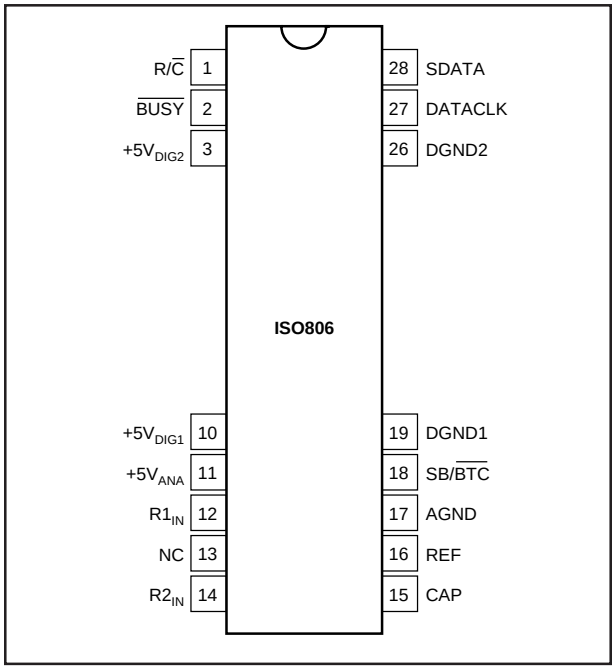
ORDERING INFORMATION

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	TYPICAL SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	SPECIFICATION TEMPERATURE RANGE	PACKAGE
ISO806P	±0.9	70	–40°C to +85°C	Plastic DIP

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	R/$\overline{C}$	I	Read/$\overline{\text{Convert}}$. With $\overline{\text{BUSY}}$ high, a falling edge on R/$\overline{C}$ initiates a new conversion.
2	$\overline{\text{BUSY}}$	O	At the start of conversion $\overline{\text{BUSY}}$ goes LOW and stays LOW until conversion is complete.
3	$+5V_{DIG2}$		Isolated Digital Supply Volts.
10	$+5V_{DIG1}$		Digital Supply Volts.
11	$+5V_{ANA}$		Analog Supply Volts.
12	$R1_{IN}$		Analog Input.
13	NC		No Connection. Leave unconnected.
14	$R2_{IN}$		Analog Input.
15	CAP		Reference Buffer Output. 2.2µF tantalum capacitor to ground.
16	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
17	AGND		Analog Ground.
18	SB/$\overline{\text{BTC}}$	I	Selects Straight Binary or Binary Two's Complement for Output Data Format.
19	DGND1		Digital Ground.
26	DGND2		Isolated Ground.
27	DATACLK	O	Data Clock Output.
28	SDATA	O	Serial Output Synchronized to DATACLK.

TABLE I. Pin Assignments.

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT $R1_{IN}$ VIA 200Ω TO	CONNECT $R2_{IN}$ VIA 100Ω TO	IMPEDANCE
±10V	V_{IN}	CAP	45.7kΩ
0V to 5V	AGND	V_{IN}	20.0kΩ
0V to 4V	V_{IN}	V_{IN}	21.4kΩ

TABLE II. Input Range Connections. See also Figure 3.

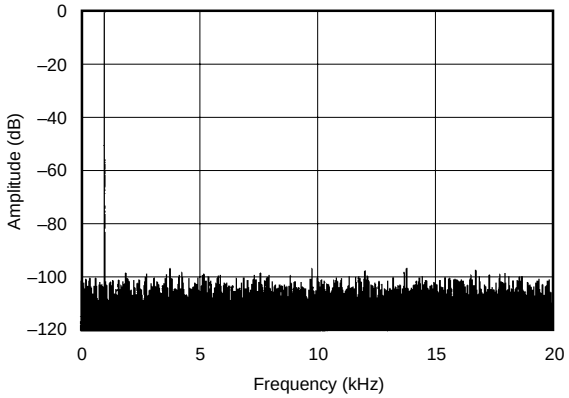
R/$\overline{C}$	$\overline{\text{BUSY}}$	DATACLK	OPERATION
↓	1	Output	Initiates conversion "n". Valid data from conversion "n-1" clocked out on SDATA.
0	↑	X	New conversion initiated without acquisition of a new signal. Data will be invalid. R/$\overline{C}$ must be HIGH when $\overline{\text{BUSY}}$ goes HIGH.
X	0	X	New convert commands ignored. Conversion "n" in progress.

TABLE III. Control Functions

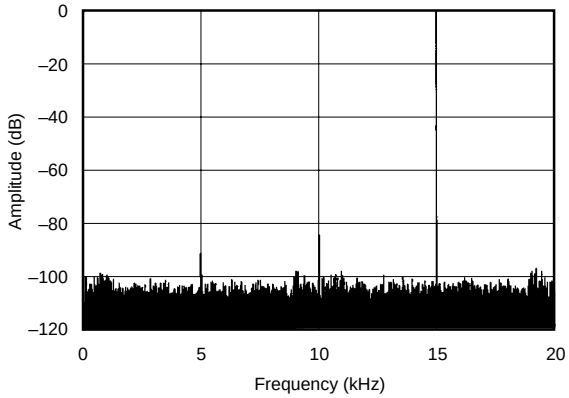
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

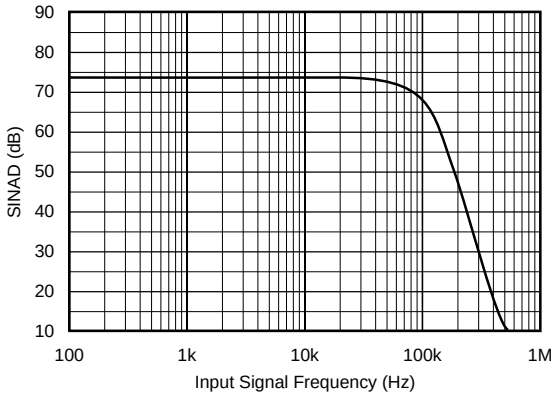
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 1kHz, 0dB)



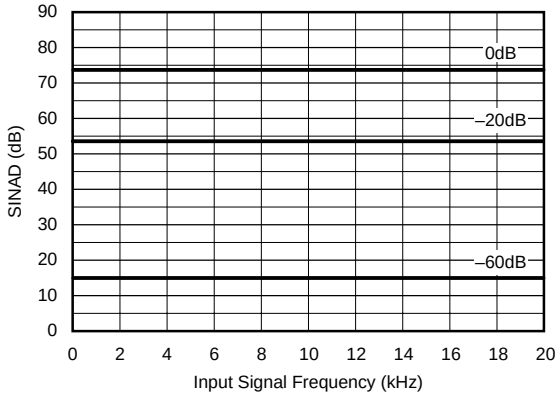
FREQUENCY SPECTRUM
(8192 Point FFT; f_{IN} = 15kHz, 0dB)



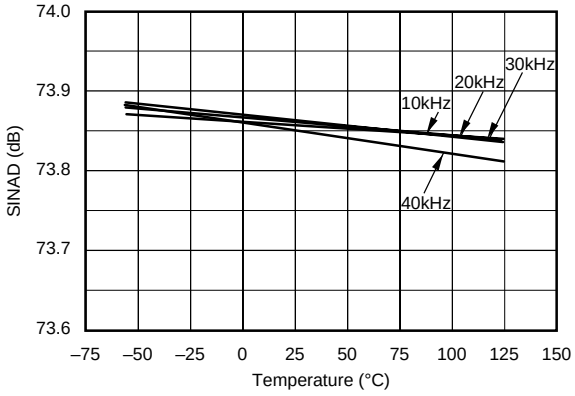
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = 0dB)



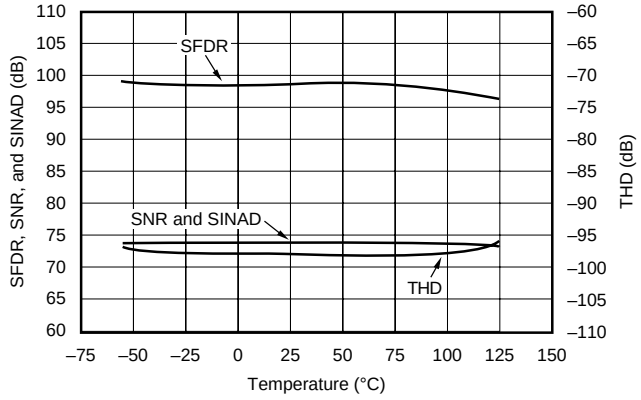
SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY AND INPUT AMPLITUDE



SIGNAL-TO-(NOISE + DISTORTION) vs TEMPERATURE
(f_{IN} = 1kHz, 0dB; f_S = 10kHz to 40kHz)

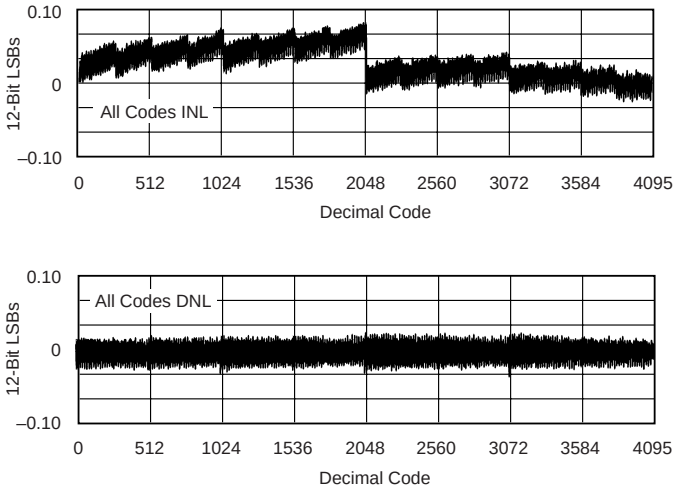


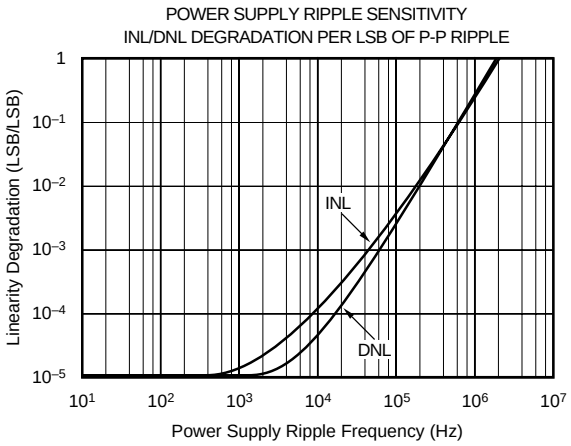
A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 1kHz, 0dB)

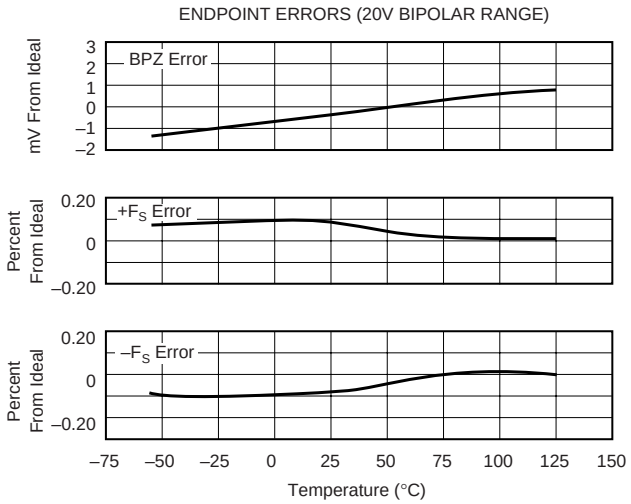


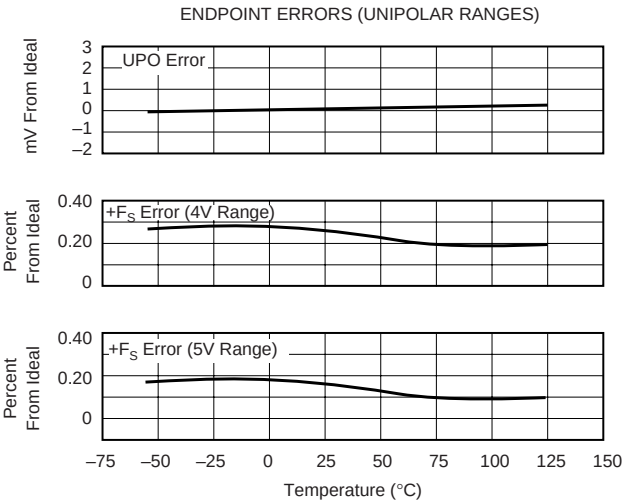
TYPICAL PERFORMANCE CURVES (CONT)

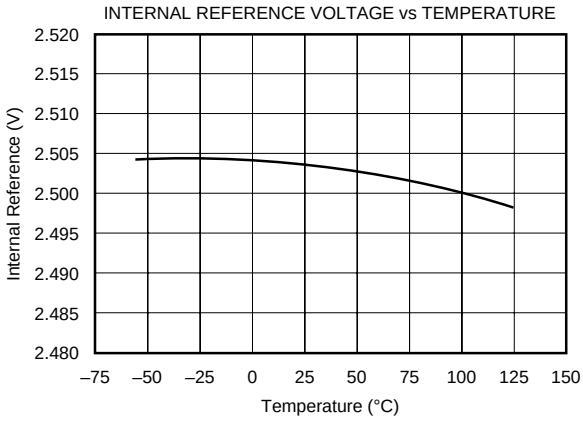
At T_A = +25°C, f_S = 40kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 3b, unless otherwise specified.

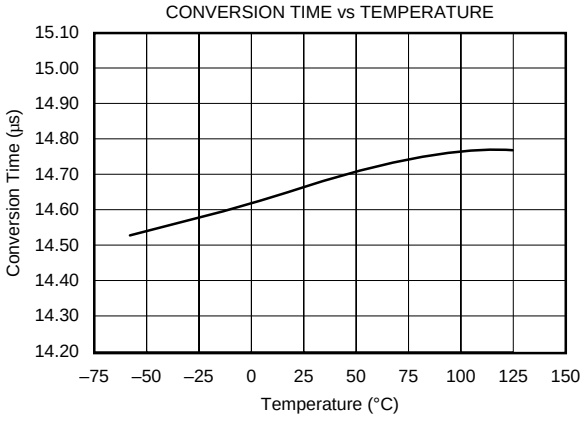












BASIC OPERATION

SERIAL OUTPUT

Figure 1 shows a basic circuit to operate the ISO806 with a ±10V input range and serial output. Taking R/$\overline{C}$ (pin 1) LOW for 40ns (12µs max) will initiate a conversion and output valid data from the previous conversion on SDATA (pin 28) synchronized to 12 clock pulses output on DATACLK (pin 27). $\overline{BUSY}$ (pin 2) will go LOW and stay LOW until the conversion is completed and the serial data has been transmitted. Data will be output in Binary Two's Complement format, MSB first, and will be valid on both the rising and falling edges of the data clock. $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ISO806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

STARTING A CONVERSION

The R/$\overline{C}$ (pin 1) LOW for a minimum of 40ns immediately puts the sample/hold of the ISO806 in the hold state and starts conversion 'n'. $\overline{BUSY}$ (pin 2) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored. R/$\overline{C}$ must go HIGH before $\overline{BUSY}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ISO806 will begin tracking the input signal at the end of the conversion. Allowing 25µs between convert commands assures accurate acquisition of a new signal. R/$\overline{C}$ is level triggered.

READING DATA

The ISO806 outputs serial data in Straight Binary or Binary Two's Complement data output format. If SB/$\overline{BTC}$ (pin 18) is HIGH, the output will be in SB format, and if LOW, the output will be in BTC format. Refer to Table IV for ideal output codes.

Reading the data through the serial port will shift the internal output registers one bit per data clock pulse.

DESCRIPTION	ANALOG INPUT			DIGITAL OUTPUT			
				BINARY TWO'S COMPLEMENT (SB/$\overline{BTC}$ LOW)		STRAIGHT BINARY (SB/$\overline{BTC}$ HIGH)	
Full-Scale Range	±10	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	4.88mV	1.22mV	976µV				
				BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
+Full Scale (FS – 1LSB)	9.99512V	4.99878V	3.999024V	0111 1111 1111	7FF	1111 1111 1111	FFF
Midscale	0V	2.5V	2V	0000 0000 0000	000	1000 0000 0000	800
One LSB Below Midscale	–4.88mV	2.49878V	1.999024V	1111 1111 1111	FFF	0111 1111 1111	7FF
–Full Scale	–10V	0V	0V	1000 0000 0000	800	0000 0000 0000	000

Table IV. Output Codes and Ideal Input Voltages.

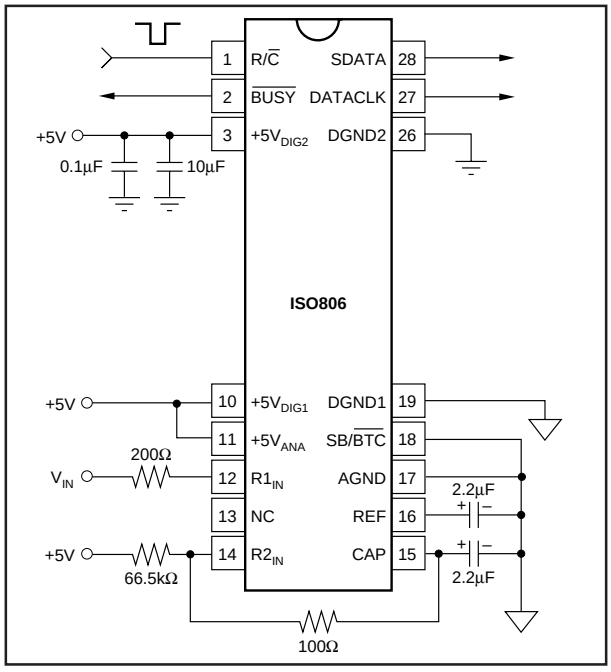


FIGURE 1. Basic ±10V Operation with Serial Output.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	0.04		12	µs
t_3	$\overline{BUSY}$ Delay from Start of Conversion		110		ns
t_4	$\overline{BUSY}$ LOW		14.7	20	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		90		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		14.7	20	µs
t_8	Acquisition Time		3		µs
t_{13}	Start of Conversion to DATACLK Delay		1.4		µs
t_{14}	DATACLK Period		1.1		µs
t_{15}	Data Valid to DATACLK HIGH Delay		75		ns
t_{16}	Data Valid after DATACLK LOW Delay		600		ns
$t_7 + t_8$	Throughput Time			25	µs

TABLE V. Conversion and Data Timing. T_A = –40°C to +85°C.

SERIAL OUTPUT

The serial output can not be tri-stated and is always active.

INTERNAL DATA CLOCK (During A Conversion)

The R/$\overline{C}$ (pin 1) LOW will initiate conversion 'n' and activate the internal data clock (typically 900kHz clock rate). The ISO806 will output 12 bits of valid data, MSB first, from conversion 'n-1' on SDATA (pin 28), synchronized to 12 clock pulses output on DATACLK (pin 27). The data will be valid on both the rising and falling edges of the internal data clock. The rising edge of $\overline{BUSY}$ (pin 2) can be used to latch the data. After the 12th clock pulse, DATACLK will remain LOW until the next conversion is initiated, SDATA will also go LOW.

INPUT RANGES

The ISO806 offers three input ranges: standard ±10V and 0-5V, and a 0-4V range for complete, single supply systems. Figures 3a and 3b show the necessary circuit connections for implementing each input range and optional offset and gain adjust circuitry. Offset and full scale error(1) specifications are tested and guaranteed with the fixed resistors shown in Figure 3b. Adjustments for offset and gain are described in the **Calibration** section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the **Calibration** section).

The input impedance, summarized in Table II, results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors used for each input range (see Figure 4). The input resistor divider network provides inherent overvoltage protection guaranteed to at least ±25V.

Analog inputs above or below the expected range will yield either positive full scale or negative full scale digital outputs respectively. There will be no wrapping or folding over for analog inputs outside the nominal range.

Note: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

HARDWARE CALIBRATION

To calibrate the offset and gain of the ISO806 in hardware, install the resistors shown in Figure 3a. Table VI lists the hardware trim ranges relative to the input for each input range.

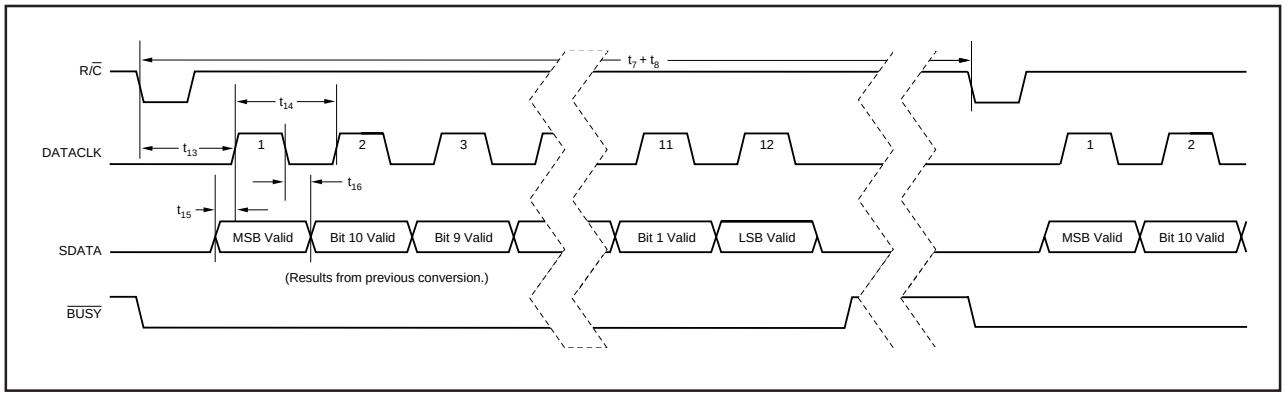


FIGURE 2. Serial Data Timing.

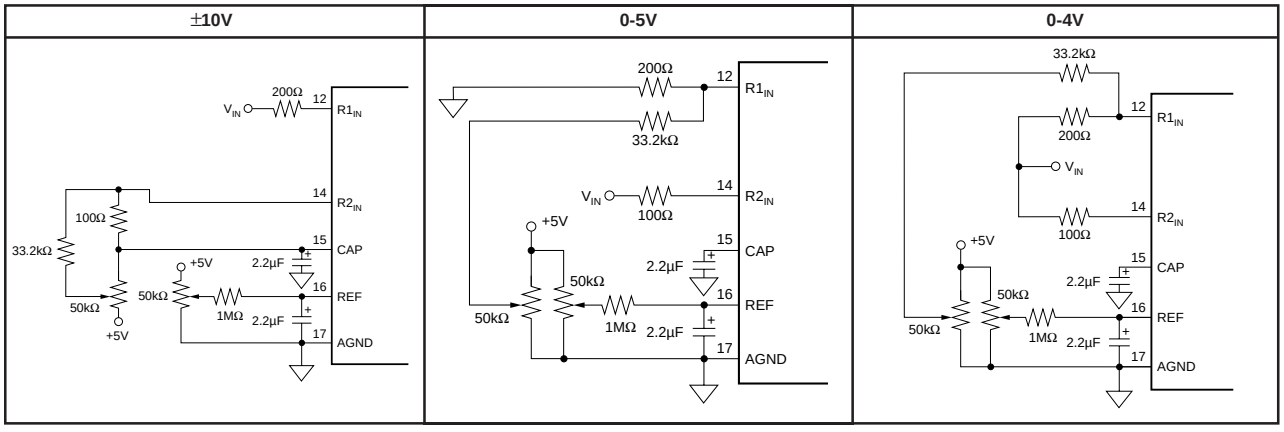


FIGURE 3a. Circuit Diagrams (With Hardware Trim).

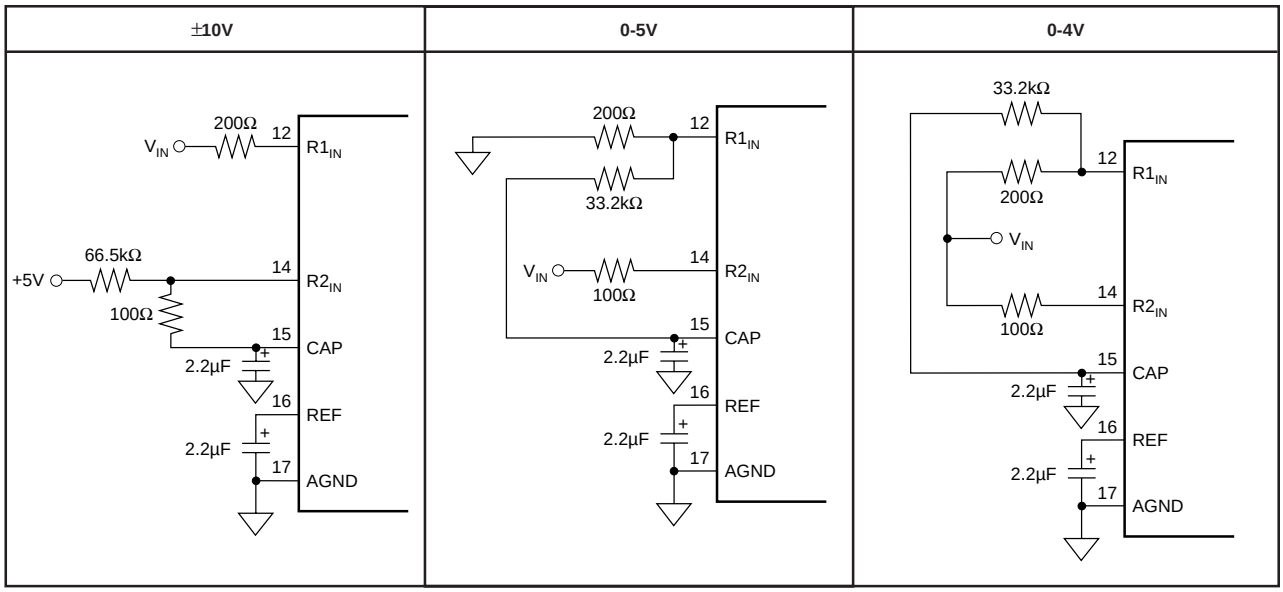


FIGURE 3b. Circuit Diagrams (Without Hardware Trim).

SOFTWARE CALIBRATION

To calibrate the offset and gain in software, no external resistors are required. However, to get the data sheet specifications for offset and gain, the resistors shown in Figure 3b are necessary. See the **No Calibration** section for more details on the external resistors. Refer to Table VII for the range of offset and gain errors with and without the external resistors.

NO CALIBRATION

See Figure 3b for circuit connections. Note that the actual voltage dropped across the external resistors is at least two orders of magnitude lower than the voltage dropped across the internal resistor divider network. This should be considered when choosing the accuracy and drift specifications of the external resistors. In most applications, 1% metal-film resistors will be sufficient.

The external resistors shown in Figure 3b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. Not using the external resistors will result in offset and gain errors in addition to those listed in the electrical specifications section. Offset refers to the equivalent voltage of the digital output when converting with the input grounded. A positive gain error occurs when the equivalent output voltage of the digital output is larger than the analog input. Refer to Table VII for nominal ranges of gain and offset errors with and without the external resistors. Refer to Figure 4 for typical shifts in the transfer functions which occur when the external resistors are removed.

To further analyze the effects of removing any combination of the external resistors, consider Figure 5. The combination of the external and the internal resistors form a voltage divider which reduces the input signal to a 0.3125V to 2.8125V input range at the CDAC. The internal resistors are laser trimmed to high relative accuracy to meet full specifications. The actual input impedance of the internal resistor network looking into pin 12 or pin 14 however, is only accurate to ±20% due to process variations. This should be taken into account when determining the effects of removing the external resistors.

REFERENCE

The ISO806 operates with its internal 2.5V reference. The internal reference has approximately an 8ppm/°C drift (typical) and accounts for approximately 20% of the full scale error (FSE = ±0.5%).

The ISO806 also has an internal buffer for the reference voltage. See Figure 6 for characteristic impedances at the input and output of the buffer with all combinations of power down and reference down.

REF

REF (pin 16) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF tantalum capacitor should be connected as close as possible to the REF pin from ground. This capacitor and the output resistance of REF create a low pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference, degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads. See Figure 6.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 15) is the output of the internal reference buffer. A 2.2µF tantalum capacitor should be placed as close as possible to the CAP pin from ground to provide optimum switching currents for the CDAC throughout the conversion cycle. This capacitor also provides compensation for the output of the buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little affect on improving performance. See Figure 6.

The output of the buffer is capable of driving up to 1mA of current to a DC load. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ISO806 uses 50% of its isolated power for the analog circuitry. The ISO806 front end should be considered as an analog component.

The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG1} (pin 10) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG1} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Two ground pins are present on the ISO806 input side. DGND1 is the digital supply ground. AGND is the analog supply ground. AGND is the ground to which all analog signals internal to the A/D are referenced. AGND is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

The ground pin of the A/D should be tied to an analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

INPUT RANGE	OFFSET ADJUST RANGE (mV)	GAIN ADJUST RANGE (mV)
±10V	±15	±60
0 to 5V	±4	±30
0 to 4V	±3	±30

TABLE VI. Offset and Gain Adjust Ranges for Hardware Calibration (see Figure 3a).

INPUT RANGE (V)	OFFSET ERROR			GAIN ERROR		
	W/ RESISTORS	W/OUT RESISTORS		W/ RESISTORS	W/OUT RESISTORS	
	RANGE (mV)	RANGE (mV)	TYP (mV)	RANGE (% FS)	RANGE (% FS)	TYP
±10	–10 ≤ BPZ ≤ 10	0 ≤ BPZ ≤ 35	+15	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–0.3 ≤ G ≤ 0.5 –0.1 ≤ G(1) ≤ 0.2	+0.05 +0.05
0 to 5	–3 ≤ UPO ≤ 3	–12 ≤ UPO ≤ –3	–7.5	–0.4 ≤ G ≤ 0.4 0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
0 to 4	–3 ≤ UPO ≤ 3	–10.5 ≤ UPO ≤ –1.5	–6	–0.4 ≤ G ≤ 0.4 –0.15 ≤ G(1) ≤ 0.15	–1.0 ≤ G ≤ 0.1 –0.55 ≤ G(1) ≤ –0.05	–0.2 –0.2
Note: (1) High Grade.						

TABLE VII. Range of Offset and Gain Errors with and without External Resistors

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The amount of charge injection due to the sampling FET switch on the ISO806 is approximately 5-10% of the amount on similar ADCs with the charge redistribution DAC (CDAC) architecture. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D. Any op amp sufficient for the signal in an application will be sufficient to drive the ISO806.

The resistive front end of the ISO806 also provides a guaranteed ±25V overvoltage protection. In most cases, this eliminates the need for external over voltage protection circuitry.

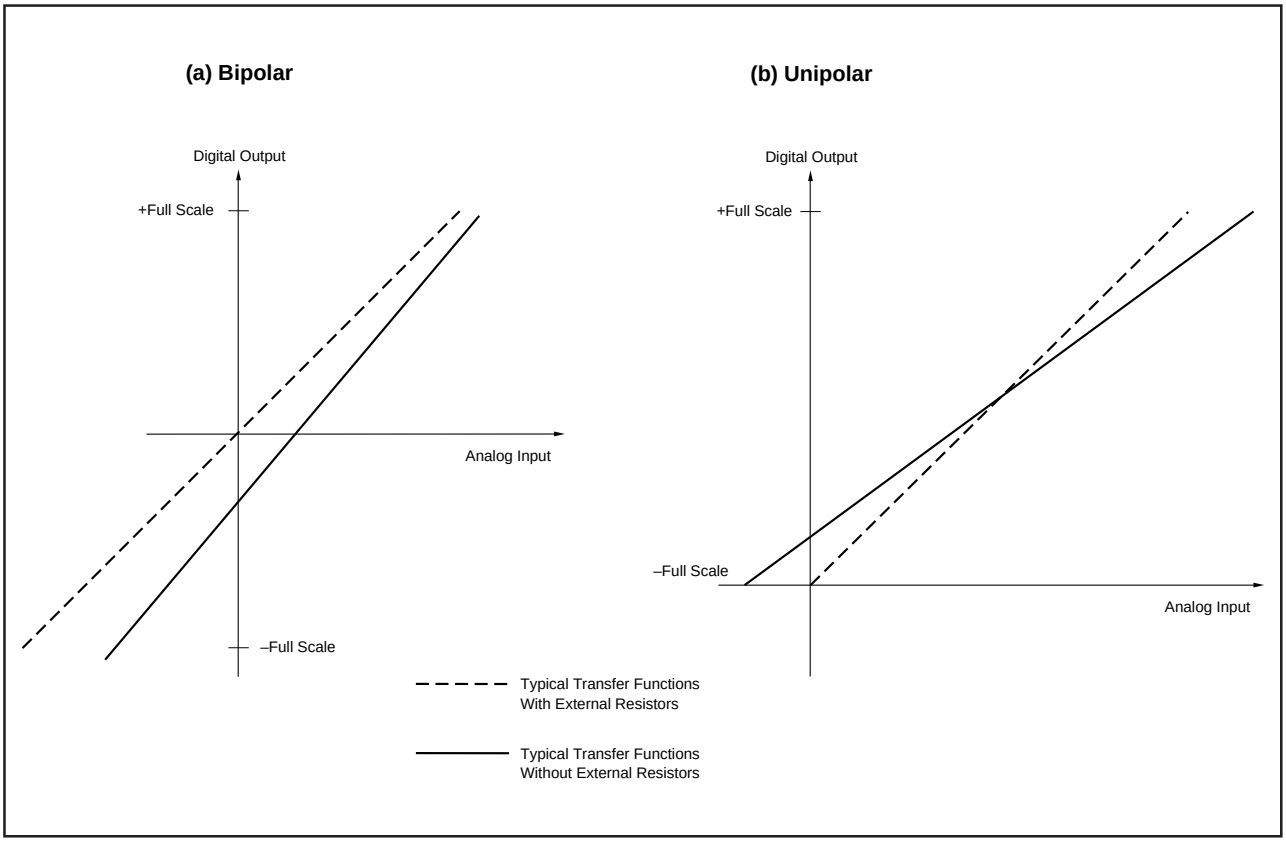


FIGURE 4. Typical Transfer Functions With and Without External Resistors.

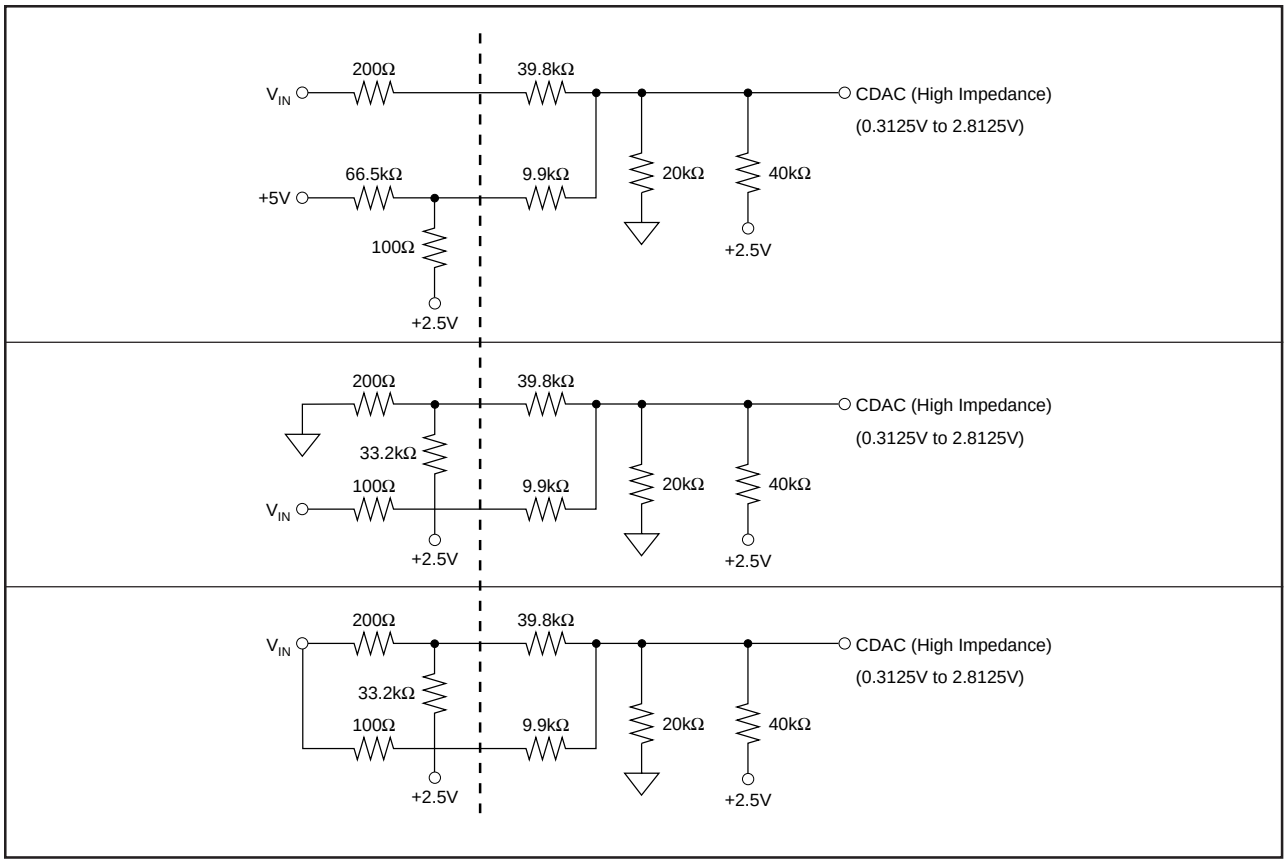
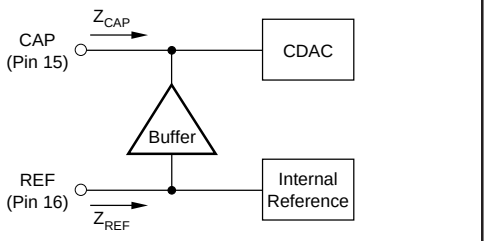


FIGURE 5. Circuit Diagrams Showing External and Internal Resistors.



	PWRD 0 REFD 0	PWRD 0 REFD 1	PWRD 1 REFD 0	PWRD 1 REFD 1
Z_{CAP} (Ω)	1	1	200	200
Z_{REF} (Ω)	6k	100M	6k	100M

FIGURE 6. Characteristic Impedances of Internal Buffer.