Feature

- Three-in-one 8 port 10/100 Ethernet switch
  - Built in an 8 port Ethernet switch engine
  - Built in 8 10/100M transceivers
  - Built in SSRAM
- Support flow control
  - Support IEEE802.3x for full duplex mode operation
  - Support backpressure for half duplex mode operation
- Built in up to 1K MAC address
- An 8 port switching fabric
  - Support two-level hashing algorithm to improve address collision
  - Support address aging
  - Store and forward mode
  - Broadcast storm protection
  - Full line speed capability of 148800 (14880) packets/sec for 100M (10M)
  - Support 1536 byte data transfer for VLAN traffic
  - Support one MII port
  - Support port base VLAN
  - Support CoS
- DSP approach transceivers
  - Auto negotiation
  - Fully digital adaptive equalizer and timing recovery module
  - Base line Wander correction
  - 10BaseT, 100BaseT, and 100BaseFX(port6, port7 only) operation
  - Automatic MDI/MDI-X configuration
- LED status of Link, Receive, Full duplex, and Speed
- LED with power on diagnostic function
- Set operation parameters via pins or EEPROM interface
- Utilize single clock source (25Mhz)
- Utilize single power supply (2.5v)
- 0.25um technology
- Packaged in 208 pin PQFP

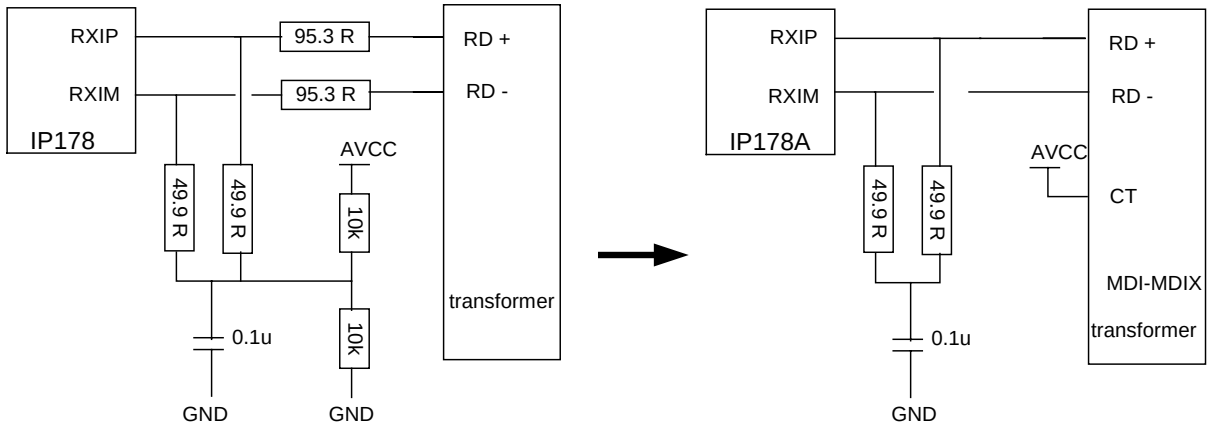
General Description

IP178A is an 8 port 10/100 Ethernet integrated switch. It consists of an 8-port switch controller and eight Fast Ethernet transceivers. Each of the transceivers complies with the IEEE802.3, IEEE802.3u, and IEEE802.3x specifications. The transceivers in IP178A are designed in DSP approach with advance 0.25um technology; this results in high noise immunity and robust performance. Two ports of IP178A can be configured as 100BaseFX.

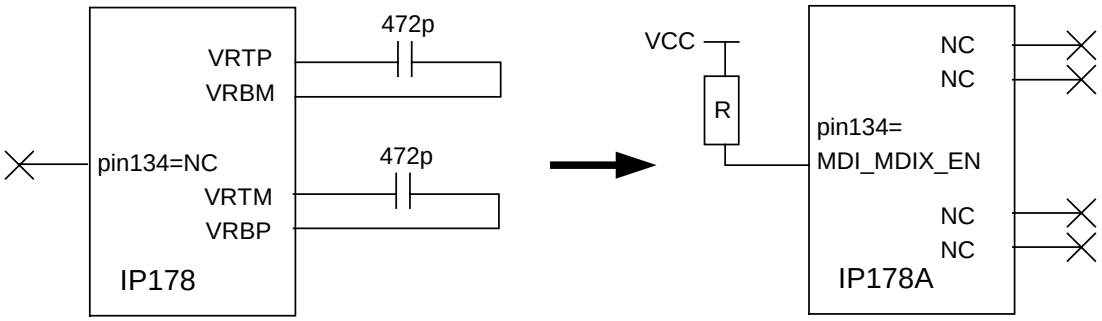
The IP178A operates in store and forward mode. It stores the incoming packet to the internal SSRAM and learns the SA (source address) automatically if the packet is error free. The SA is stored to the internal address table. IP178A forwards a packet according to DA and address table. When the segments of destination ports are free, it reads the packet from the internal SSRAM and forwards it to the appropriate ports according to the address table. The incoming packets with errors are dropped. IP178A supports IEEE802.3x, optional backpressure, Auto MDI/MDI-X, CoS, port base VLAN, one MII port and various LED functions, etc. These functions can be configured to fit the different requirements by feeding operation parameters via EEPROM interface or pull up/down resistors on specified pins.

The major differences in application circuit between IP178 and IP178A

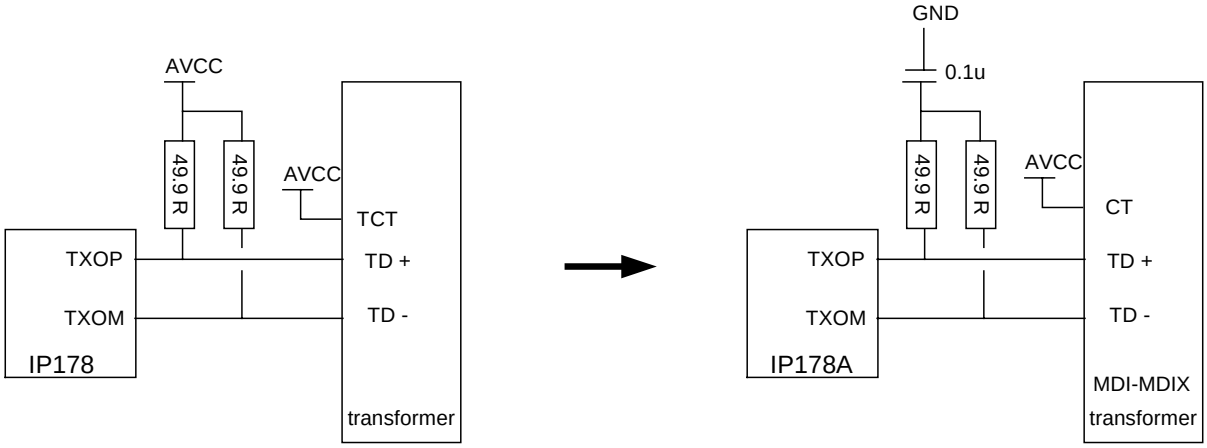
No more external bias and series resistors



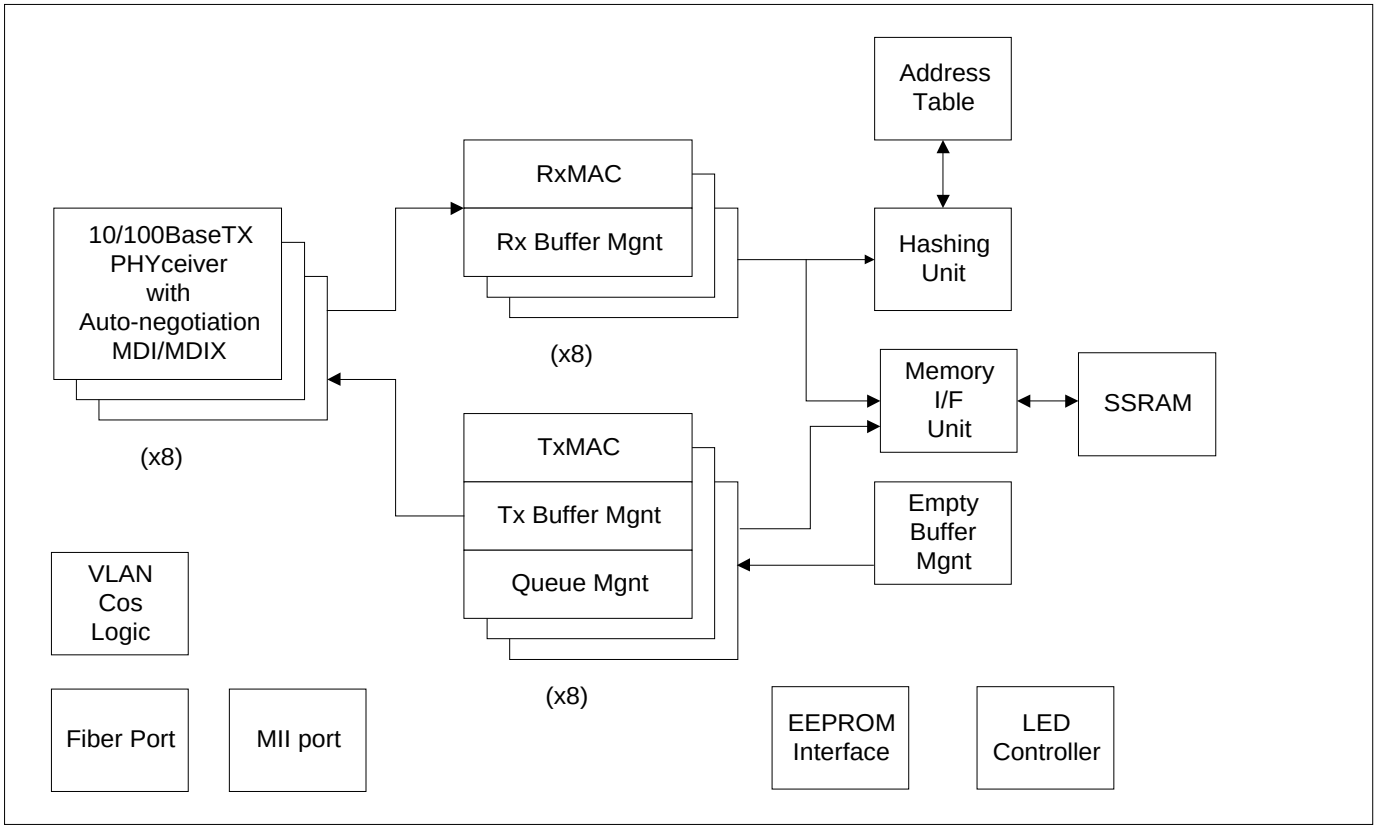
No more A/D bypass capacitors & add a pull up resistor to turn on auto MDI_MDIX



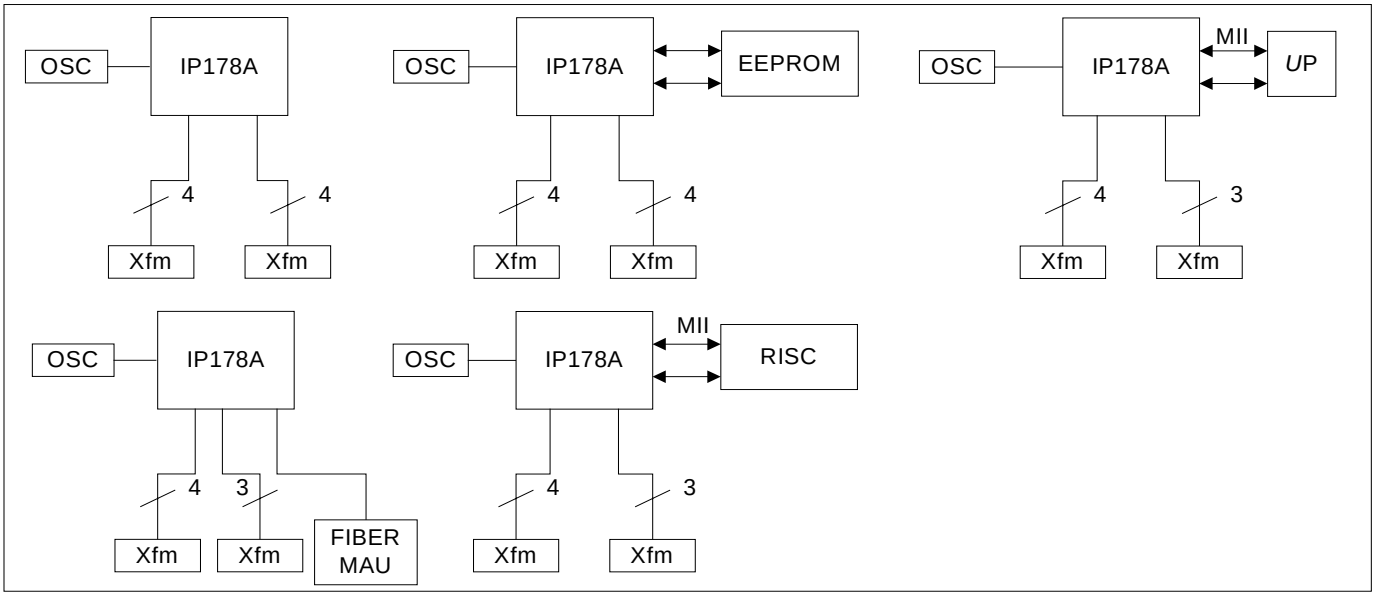
Transmit circuit is the same as receive circuit for MDI-MDIX function.



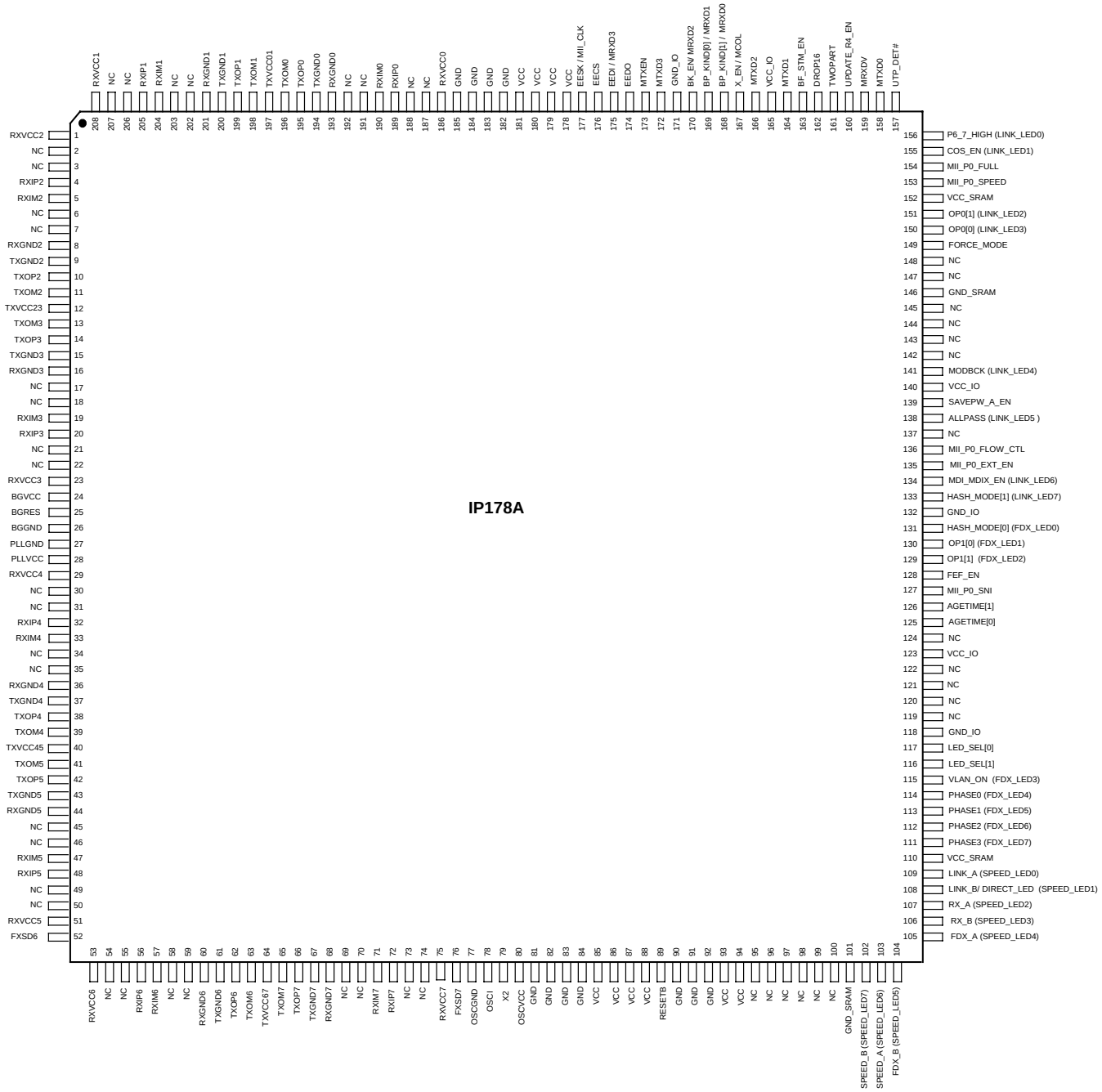
Block Diagram



System Block Diagram



PIN Assignments



PIN Description

Type	Description
I	Input pin
IPL	Input pin with internal pull low
IPH	Input pin with internal pull high
O	Output pin
I/O	Input and Output pin

Pin no.	Label	Type	Description
MLT3 signals			
25	BGRES	I	**Band gap resister** It is connected to GND through a 6.19k (1%) resistor in application circuit.
52, 76	FXSD6 FXSD7	I	**100Base-FX signal detect** Fiber signal detect of port 6 and 7 when the ports are configured to be fiber ports. Fiber signal detect is active if the voltage of FXSD is higher than 1.2v. If TP mode is selected, the pins must be connected to ground.
189, 190, 205, 204, 4, 5, 20, 19, 32, 33, 48, 47, 56, 57, 72, 71	RXIP0~7 RXIM0~7	I	**TP receive**
195, 196, 199, 198, 10,11, 14, 13, 38, 39, 42, 41, 62, 63, 66, 65	TXOP0~7 TXOM0~7	O	**TP transmit**

PIN Description (continued)

Pin no.	Label	Type	Description
174	EEDO	IPL	**Data input of EEPROM**
175	EEDI	IPL/O	**Data output of EEPROM** It is input during reset period. After reset, it is an output signal EEDI to read EEPROM. After reading EEPROM, this pin becomes an output signal MRXD3, if external MII port is enabled (MII_P0_EXT_EN=1); otherwise, it is an input signal.
176	EECS	IPL/O	**Chip select of EEPROM** It is input during reset period. After reset, it is an output signal EECS to read EEPROM. After reading EEPROM, this pin becomes an input signal.
177	EESK	IPL/O	**Clock input of EEPROM** It is input during reset period. After reset, it is an output signal EESK to read EEPROM. After reading EEPRM, this pin becomes an output signal MII_CLK, if external MII port is enabled (MII_P0_EXT_EN=1); otherwise, it is an input signal.
Misc.			
78	OSCI	I	**25Mhz system clock.** A 25Mhz clock from oscillator is fed to this pin. The X2 pin should be left open in this application.
79	X2	O	**Crystal pin** A 25Mhz crystal can be connected to OSCI and X2.
89	RESETB	I	**Reset** It is low active. It must be hold for more than 1ms. It is Schmitt trigger input.

PIN Description (continued)

Pin no.	Label	Type	Description
Direct mode LED.			
133, 134, 138, 141, 150, 151, 155, 156	LINK_LED[7:0]	O	LINK_LED of port 7~0 If pin 108 DIRECT_LED is pulled up, LINK_LED[7:0] are link LED of port 7~0. The detail functions are illustrated in the following table.
102, 103, 104, 105, 106, 107, 108, 109	SPEED_LED[7:0]	O	SPEED_LED of port 7~0 If pin 108 DIRECT_LED is pulled up, SPEED_LED[7:0] are speed LED of port 7~0. The detail functions are illustrated in the following table.
111, 112, 113, 114, 115, 129, 130, 131	FDX_LED[7:0]	O	FDX_LED of port 7~0 If pin 108 DIRECT_LED is pulled up, FDX_LED[7:0] are full duplex LED of port 7~0. The detail functions are illustrated in the following table.
116, 117	LED_SEL[1:0]	IPH	LED function selection The pins are latched at the end of reset to select LED functions. The detail functions are illustrated in the following table.

A table for direct mode LED

LED_SEL[1:0]	LinK_LED[7:0]	SPEED_LED[7:0]	FDX_LED[7:0]
00	Off: link fail On: 10M link ok Flash: Tx/Rx	Off: link fail On: 100M link ok Flash: Tx/Rx	Off: half duplex On: full duplex
01	Off: link fail On: link ok Flash: Rx	Off: 10M On: 100M	Off: half duplex On: full duplex Flash: collision
10	Off: link fail On: 10M link ok Flash: Tx/Rx	Off: link fail On: 100M link ok Flash: Tx/Rx	Off: half duplex On: full duplex Flash: collision
11 (default)	Off: link fail On: link ok Flash: Tx/Rx	Off: 10M On: 100M	Off: half duplex On: full duplex Flash: collision

PIN Description (continued)

Pin no.	Label	Type	Description
Direct mode LED.			
108	DIRECT_LED	IPL	Direct mode LED It is latched at the end of reset to select LED mode. It will be lathed as high, if it is connected to VCC through a resistor. It will be latched as low, if it is left open. 1: LED direct mode. IP178A provides 24 LED pins to drives 24 LED directly. The 24 LED are LINK_LED[7:0], SPEED_LED[7:0], and FDX_LED[7:0]. 0: LED scan mode (default) IP178A provides 12 LED pins to drives 32 LED in scan mode. The 32 LED are Link LED[7:0], Speed LED[7:0], Full duplex LED[7:0], and Rx LED[7:0]. It is compatible to the previous version of IP178.

PIN Description (continued)

Pin no.	Label	Type	Description
Scan mode LED.			
102	SPEED_B	O	It is a control signal of speed LED for port 4~7 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
103	SPEED_A	O	It is a control signal of speed LED for port 0~3 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
104	FDX_B	IPL/O	It is a control signal of full duplex LED for port 4~7 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
105	FDX_A	IPL/O	It is a control signal of full duplex LED for port 0~3 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
106	RX_B	IPL/O	It is a control signal of rx LED for port 4~7 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
107	RX_A	IPL/O	It is a control signal of rx LED for port 0~3 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
108	LINK_B	IPL/O	It is a control signal of link LED for port 4~7 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
109	LINK_A	IPL/O	It is a control signal of link LED for port 0~3 after reset if LED scan mode is selected. The detail functions are illustrated in the following table.
111, 112, 113, 114	PHASE[3:0]	IPL/O	These pins are phase control signals after reset if LED scan mode is selected.

A table for scan mode LED

LED_SEL[1:0]	Link LED	Rx LED	Full duplex LED	Speed LED
00	Off: link fail On: 10M link ok Flash: Tx/ Rx	Off: no collision Flash: collision	Off: half duplex On: full duplex	Off: link fail On: 100M link ok Flash: Tx/ Rx
01	Off: link fail On: link ok Flash: Rx	Off: idle Flash: Tx/ Rx	Off: half duplex On: full duplex Flash: collision	Off: 10M On: 100M
10	Off: link fail On: 10M link ok Flash: Tx/Rx	Off: no collision Flash: collision	Off: half duplex On: full duplex Flash: collision	Off: link fail On: 100M link ok Flash: Tx/Rx
11 (default)	Off: link fail On: link ok Flash: Tx/Rx	Off: no collision Flash: collision	Off: half duplex On: full duplex Flash: collision	Off: 10M On: 100M

PIN Description (continued)

Pin no.	Label	Type	Description
MII ports			
177	MII_CLK	IPL/O	**MII_CLK** It is an output signal MII_CLK, if external MII port is enabled (MII_P0_EXT_EN=1). Both MRXD and MTXD are synchronous to this clock. This pin is shared with EESK. Please reference pin description of EESK for more detail information MII_CLK is CLK in SNI mode.
159	MRXDV	IPL/O	**MRXDV** It is an output signal MRXDV, if external MII port is enabled (MII_P0_EXT_EN=1). MRXDV is CRS in SNI mode.
175	MRXD3	IPL/O	**MRXD3** It is an output signal MRXD3, if external MII port is enabled (MII_P0_EXT_EN=1). This pin is shared with EEDI. Please reference pin description of EEDI for more detail information
170	MRXD2	IPH/O	**MRXD2** It is an output signal MRXD2, if external MII port is enabled (MII_P0_EXT_EN=1). This pin is shared with BK_EN. Please reference pin description of BK_EN for more detail information
169	MRXD1	IPL/O	**MRXD1** It is an output signal MRXD1 if external MII port is enabled (MII_P0_EXT_EN=1).
168	MRXD0	IPL/O	**MRXD0** It is an output signal MRXD0 if external MII port is enabled (MII_P0_EXT_EN=1). MRXD0 is RXD in SNI mode.
167	MCOL	IPH/O	**MCOL** It is an output signal MCOL if external MII port is enabled (MII_P0_EXT_EN=1). This pin is shared with X_EN. Please reference pin description of X_EN for more detail information
173	MTXEN	IPL	**MTXEN** MTXEN is TXEN in SNI mode.
172, 166, 164, 158	MTXD3[3:0]	IPL	**MTXD[3:0]** MTXD0 is TXD in SNI mode.

PIN Description (continued)

Pin no.	Label	Type	Description
Basic operation parameter setting of switch			
170	BK_EN	IPH/O	**Backpressure enable** 1: enable (default), 0: disable This pin is input to set backpressure during reset. It becomes an output signal MRXD2 after reset, if external MII port is enabled.
168, 169	BP_KIND[1:0]	IPL/O	**Backpressure type selection** 00: carrier base backpressure (default) 01: (reserved) 10: (reserved) These two pins are input during reset. It becomes output signals MRXD0 and MRXD1 after reset, if external MII port is enabled. IP178A supports carrier base backpressure only.
167	X_EN	IPH/O	**IEEE 802.3x flow control enable** 1: enable (default), 0:disable This pin is an input to set flow control during reset. It becomes an output signal MCOL after reset, if external MII port is enabled.
163	BF_STM_EN	IPL	**Broadcast storm enable** 1: enable, 0: disable (default) IP178A drops the incoming packet if the number of broadcast packet in queue is over the threshold.
162	DROP16	IPL	**Drop the transmitting packet after 16 consecutive collisions** 1: drop, 0: not drop (default)
161	TWOPART	IPH	**Turn on twopartD (Twopart)** 1: enable (fixed), 0: disable IP178A examine the carrier for 64 bits only during its back off period if this function is enabled. It makes IP178A have higher priority in a collision event. IP178A uses the default value. User can't change the setting.
141	MODBCK	IPH/O	**Aggressive back off enable (MODBCK)** IP178A uses modified (aggressive) back off algorithm if this function is enabled. The maximum back off period is limited to 8-slot time. It makes IP178A have higher priority in a collision event. 1: aggressive mode enable (default), 0: standard back off It is link LED of port 4 after reset if LED direct mode is selected.
138	ALLPASS	IPL/O	It is for testing only. This pin should be left open to turn off the function for normal operation. It is link LED of port 5 after reset if LED direct mode is selected.

PIN Description (continued)

<table>
<tr><th>Pin no.</th><th>Label</th><th>Type</th><th>Description</th></tr>
<tr><td colspan="4">Basic operation parameter setting of switch</td></tr>
<tr><td>133, 131</td><td>HASH_MODE[1:0]</td><td>IPL</td><td>Hashing algorithm selection for 1st layer and 2nd layer
00: direct and CRC (default)
01: direct and CRC
10: CRC and CRC
11: reserved

The pins are input signals during reset and are latched at the end of reset to select hashing algorithm. HASH_MODE[0] is full duplex LED of port 0 after reset if LED direct mode is selected. HASH_MODE[1] is link LED of port 7 after reset if LED direct mode is selected.</td></tr>
<tr><td>126, 125</td><td>AGETIME[1:0]</td><td>IPH, IPL</td><td>Aging time selection of address table
An address tag in hashing table will be removed if this function is turned on and its aging timer expires.

<table>
<tr><td>AGETIME[1]</td><td>AGETIME[0]</td><td>Aging time</td></tr>
<tr><td>0</td><td>0</td><td>no aging</td></tr>
<tr><td>0</td><td>1</td><td>120s</td></tr>
<tr><td>1</td><td>0</td><td>240s (default)</td></tr>
<tr><td>1</td><td>1</td><td>480s</td></tr>
</table>
</td></tr>
</table>

PIN Description (continued)

Pin no.	Label	Type	Description
Advance operation parameter setting of switch			
156	P6_7_HIGH	IPL/O	**Port6 port7 are set to be high priority port** Packets received from port6 or port7 are handled as high priority packets if the function is enabled. 1: enable, 0: disabled (default) It is an input signal during reset and its value is latched at the end of reset to set high priority port. It is link LED of port 0 after reset if LED direct mode is selected.
155	COS_EN	IPL/O	**Class of service enable** Packets with high priority tag are handled as high priority packets if the function is enabled. 1: enable, 0: disabled (default) It is an input signal during reset and its value is latched at the end of reset to set CoS. It is link LED of port 1 after reset if LED direct mode is selected.
115	VLAN_ON	IPL/O	**VLAN enable** Enable a specified configuration of port base VLAN. It is an input signal during reset and its value is latched at the end of reset to set VLAN. It is full duplex LED of port 3 after reset if LED direct mode is selected. 0: disabled (default), 1: enable IP178A are separated into 7 VLANs if this function is enabled. The VLAN group is as follows, VLAN 1: port0, port 7 VLAN 2: port 1, port 7 VLAN 3: port 2, port 7 VLAN 4: port 3, port 7 VLAN 5: port 4, port 7 VLAN 6: port 5, port 7 VLAN 7: port 6, port 7 The configuration can be updated by programming EEPROM register. Please refer to EEPROM register 07h~0Ah for detail information.

PIN Description (continued)

Pin no.	Label	Type	Description
PHY operation parameter setting			
134	MDI_MDIX_EN	IPL/O	MDI/MDI-X enable MDI/MDI-X auto cross over 1: enable, 0:disable (default) It is an input signal during reset and its value is latched at the end of reset to set auto MDI/MDIX function. It is link LED of port 6 after reset if LED direct mode is selected. It is internally pulled low.
160	UPDATE_R4_EN	IPH	**Change capability enable** Force to be link at half duplex, if each node doesn't support IEEE802.3x. This will prevent the packet loss due to no flow control in full duplex mode. 1: enable (default), 0: disable It is internally pulled high. It is connected to GND through a resistor to turn off the function in IP178A application circuit.
139	SAVEPW_A_EN	IPH	Savepw_a_en, Power saving mode for fast link pulse 1: enable (default), 0:disable It is internally pulled high. The default value must be adopted normal operation.
157	UTP_DET#	I	**UTP detect enable** Power saving mode for unplugged port. 1: disable, FLP is sent out every 12~16ms. 0: enable FLP is sent out every 1.2 sec if cable is unplugged and the function is enabled. If a FLP is received, IP178A resumes to send out FLP every 12~16ms. This function is disabled in spite of the setting on this pin and it can be enable by EEPROM only.
128	FEF_EN	IPH	**Far end fault detect function of Fiber port** 1: enable (default), 0: disable

PIN Description (continued)

Pin no.	Label	Type	Description
PHY operation parameter setting			
149, 129, 130, 151, 150	FORCE_MODE OP1[1:0] OP0[1:0]	IPL	**Transceiver operation mode selection** These pins are internally pulled low.

Summary

	OP1 [1:0]	OP0 [1:0]	FORCE_MODE	Description
	0 0	x	0	Port1, 3, 5, 7 nway with all capability (default)
	1 0	x	0	Port7 FX full duplex, port1, 3, 5 nway with all capability
	1 1	x	0	Port7 FX half duplex, port1, 3, 5 nway with all capability
	x	0 0	0	Port0, 2, 4, 6 nway with all capability (default)
	x	1 0	0	Port6 FX full duplex, port0, 2, 4 nway with all capability
	x	1 1	0	Port6 FX half duplex, port0, 2, 4 nway with all capability

PIN Description (continued)

Pin no.	Label	Type	Description
External MII port operation parameter setting			
135	MII_P0_EXT_EN	IPL	**External MII port enable** 1: enable, 0: disable (default)
154	MII_P0_FULL	IPH	**Duplex setting of external MII port** 1: full (default), 0: half It is valid only if MII_P0_EXT_EN is set to logic high.
153	MII_P0_SPEED	IPH	**Speed setting of external MII port** 1: 10M (default), 0: 100M It is valid only if MII_P0_EXT_EN is set to logic high.
136	MII_P0_FLOW_CTL	IPL	**Flow control setting of external MII port** 1: on, 0: off (default) It is valid only if MII_P0_EXT_EN is set to logic high.
127	MII_P0_SNI	IPL	External Mac interface selection 1: SNI interface 0: MII interface (default) It is valid only if MII_P0_EXT_EN is set to logic high. If the SNI interface is enabled, port0 of switch core is forced to 10Mbps.
Power			
BGVCC	I	**Power of band gap circuit**	
BGGND	I	**Power of band gap circuit**	
PLLGND	I	**Power of PLL circuit**	
PLLVCC	I	**Power of PLL circuit**	
OSCGND	I	**Power of oscillator**	
OSCVCC	I	**Power of oscillator**	
GND	I	**Power of internal logic**	
VCC	I	**Power of internal logic**	
GND_SRAM	I	**Power of internal SRAM**	
VCC_SRAM	I	**Power of internal SRAM**	
GND_IO	I	**Power for LED and EEPROM**	
VCC_IO	I	**Power for LED and EEPROM**	
RXVCC0~7	I	**Power of analog receive block**	
RXGND0~7	I	**Power of analog receive block**	
TXGND0~7	I	**Power of analog transmit buffer**	
TXVCC01 TXVCC23 TXVCC45 TXVCC67	I	**Power of analog transmit buffer**	
NC		**No connection. They should be left open for normal operation.**	

Functional Description

Basic Operation

IP178A consists of eight switching ports. Full/half duplex and speed of each port depends on the result of auto negotiation of its corresponding transceiver. It is not necessary to use an external memory to buffer packets.

Each port of IP178A has its own receive buffer management, transmit buffer management, transmit queue management, transmit MAC and receive MAC. All ports share a hashing unit, a memory interface unit, an empty buffer management, and an address table.

An incoming packet is stored to the internal memory if the packet is error free. A packet is error free if its crc field is correct and its length is between 64 and 1536 byte. At the same time, IP178A examines the address field of the packet. By the way, switch learns the locations of every station (source address) and records them on the address table. IP178A then reads the packet from the internal memory and sends it to the appropriate ports according to the address table. Eventually, IP178A supports the switching function by dropping or forwarding the incoming packets.

Block Description

The basic function of each block in the block diagram is illustrated in the following context. Hashing unit is responsible to learn and to recognize address. Transmit buffer management and receive buffer management are responsible to store data to or to read data from the internal memory through memory interface unit. Transmit MAC and receive MAC interface to transceivers and implement Ethernet protocol.

Receive MAC receives the incoming data from transceiver and converts nibble data into double word data. As a 32 bit data is ready, it feeds the data into receive FIFO and requests receive buffer management for data transfer. When receive buffer management receives the request, it gets a empty block from empty buffer management and writes the double word data to the buffer, which is located in the internal SSRAM, through memory interface unit. The incoming packet is fed to hashing unit at the same time. Hashing unit extracts the source address of incoming packet to set up an address table. An incoming packet is dropped or forwarded according to the table. The address table is built in the SSRAM of IP178A.

All ports share an empty buffer management. After reset, the empty buffer management provides 8 addresses of empty blocks. When a packet comes in, it searches for a new empty block. After a packet is forwarded, the corresponding blocks are released. Empty buffer management treats the block as an empty block and provides its address to desired receive buffer management. Eight addresses are always ready for receive buffer management.

Back off Algorithm

IP178A provides two parameters to modify its back off algorithm. They are Modbck and Drop16. IP178A implements the IEEE802.3 standard binary exponential back off algorithm (Modbck=0) and modified back off algorithm (Modbck=1) when it works at half duplex mode. If Modbck is set, the maximum back off time is limited to eight-slot time. The minimum defer time is separated into the two periods. The first period consists of the first 64-bit time and the 2nd period consists of the rest 32 bit-time. In the case of minimum defer time IP178A transmits a packet after 96-bit time immediately in spite of the status of cable on the 2nd period. After 16 consecutive collisions, the transmitting packet is dropped if Drop16 is set.

Operation Parameter

IP178A supports many optional functions. They can be configured to fit different requirements by setting appropriate parameters. These parameters can be fed into IP178A through EEPROM interface or through pins.

Flow Control

IP178A provides two mode of flow control. Backpressure is for half duplex mode and IEEE802.3x flow control is for full duplex.

Backpressure

The backpressure is used for flow control in half duplex mode if Bk_en is turned on. When the buffer of a port is full, it will start to send jam signals. The remote station will defer transmission after detecting the jam signals.

Carrier based backpressure is sent by IP178A, when the buffer of a port is full. IP178A sends jam packets continuously to defer the remote station. The length of jam packet is 1518 byte and the IPG is equal to 96-bit time. If the port has packets to transmit during this period, it transmits the queuing packet instead of the jam packets. After the queuing packets are transmitted, IP178A resumes to jam the segment by sending jam packets if the buffer of a port is full. If a collision occurs, the back off algorithm is skipped and the jam packets are generated immediately. The definition of buffer full for carrier base backpressure is there is only one empty buffer for a port.

IEEE 802.3x

The IEEE 802.3x is used for flow control in full duplex mode if both IP178A (X_en=1) and the remote station have IEEE802.3x capability. When the level of occupied buffer of a port is over set threshold, it will send a PAUSE frame with maximum delay FFFF. The remote station will stop to transmit the next packet after receiving the PAUSE frame. After level of the occupied buffer is below release threshold, the port sends out a PAUSE frame with zero delay to resume receiving the incoming packets. The remote station is re-enable to transmit packets after receiving the PAUSE frame with zero delay. While level of the occupied buffer of a port is over set threshold, IP178A re-transmits the PAUSE frame with maximum delay to ensure the pause timer of the remote station does not expire and begins transmission. The IPG between PAUSE frames is 42ms(100M) or 420ms(10M).

When an incoming PAUSE frame with non-zero delay is received, the port stops the next frame transmission and starts its pause timer. It is re-enabled transmission function either the pause timer is expired or a PAUSE frame with zero delay is received. If another pause frame is received before the timer expires, the timer will be updated with the new value. During this period, only PAUSE frame from IP178A will be transmitted.

PAUSE Frame Format

Destination	Source	Type	Opcode	Pause Timer	Pad	CRC
01-80-C2-00-00-01	SA	8808	0001	FFFF(0000)	PAD with zero	CRC
6 bytes	6 bytes	2 bytes	2bytes	2 bytes	42 bytes	4 bytes

Capability Changing

If the remote station does not support IEEE802.3x and has full duplex capability, IP178A supports a private mechanism to handle flow control to prevent packet loss. It is called capability changing and is controlled by the parameter Update_r4_en. This function prevents the packet loss due to no IEEE802.3x.

When the remote station does not support IEEE802.3x and has full duplex capability and Update_r4_en is turned on, the port changes its ability to half duplex to make the remote station link at half duplex after Nway. IP178A handles the data flow of segment by backpressure. To do this, the port keeps silence to force the remote node link failure and changes its capability to half duplex then restarts Nway. Both side of the segment will be link at half duplex.

When the remote station does not support IEEE802.3x and has full duplex capability and Update_r4_en is turned off, the port turns off its IEEE802.3x capability and is link at full duplex after Nway. There is no flow control between these two nodes in this application. The detail operation is illustrated in the following table.

Conditions						Result			
X_EN	REMOTE_IEEE 802.3X	UPDATE_ R4_E	BK_EN	Remote site	My site	Remote site	My site	My 802.3x	My back pressure
x	x	x	0	half	X	half	half	off	off
x	x	x	1	half	X	half	half	off	on
1	1	0	x	full/half	full/half	full	full	on	off
0	1	0	x	full/half	full/half	full	full	off	off
1	0	0	x	full/half	full/half	full	full	off	off
0	0	0	x	full/half	full/half	full	full	off	off
1	1	1	x	full/half	full/half	full	full	on	off
0	1	1	x	full/half	full/half	half	half	off	on
1	0	1	x	full/half	full/half	half	half	off	on
0	0	1	x	full/half	full/half	half	half	off	on

Aging

IP178A supports address aging. If the address aging is enabled (Agetime≠0), the learned SA will be cleared if it is not refreshed within the specified aging time.

Broadcast Storm Protection

IP178A is able to prevent receiving too many broadcast packets to waste the switch resource. IP178A discards the incoming broadcast packets depending on the setting of Bf_stm_en if the number of broadcast packets from a port exceeds threshold.

Automatic MDI/MDI-X configuration

IP178A supports MDI/MDI-X function if the function is enabled. The RX and TX pairs will be corrected automatically. That is, IP178A can be connected to another devices with either crossover cable or non-crossover cable.

When a cable is plugged, IP178A looks for NLP, FLP or MLT3 signals to make sure if the receive path is correct. If IP178A finds nothing in the receiving path, it crosses over the RX and TX pairs and examines the inputs again. The process will go on until IP178A sees a stable NLP, FLP or MLT3 signals. The process starts prior to the auto-negotiation.

The MDI/MDI-X function needs specific type of transformer. The PCB for previous version of IP178A also supports MDI/MDI-X function if the specific type of transformer is adopted.

CoS

IP178A supports two type of CoS. One is port base priority function and the other is frame base priority function. A high priority packet will be queued to the high priority queue to guarantee its faster delivery. IP178A supports two levels of priority queues.

The packets received from port 6 or port7 are handled as high priority frames if the port base priority is enabled. It is enabled if pin p6_7_high is pulled high or the bit 02H[14] of EEPROM register is set. The setting in register takes precedence of the setting on pins.

IP178A examines the specific bits of VLAN tag and TCP/IP TOS/DS for priority frames if the frame base priority is enabled. The packets will be handled as high priority frames if the value of VLAN tag or TCP/IP TOS/DS field meets the high priority requirement. It is enabled if pin Cos_en is pulled high or EEPROM register 02H[15] is set. The setting in register takes precedence of the setting on pins.

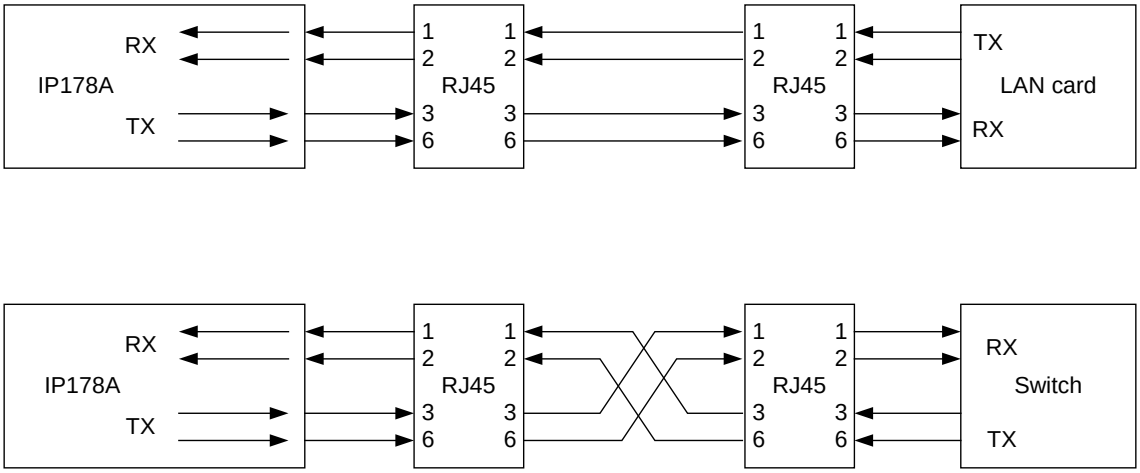
VLAN

IP178A supports port base VLAN functions if the function is enabled. It separates IP178A into some groups (VLAN). A port is limited to communicate with the ports within the same group (VLAN). Frames will be limited in a VLAN and will not be forwarded to other VLANs. A port can be assigned to one or more VLANs. The members (ports) of a VALN are assigned by programming the content of EEPROM register 07H~0AH.

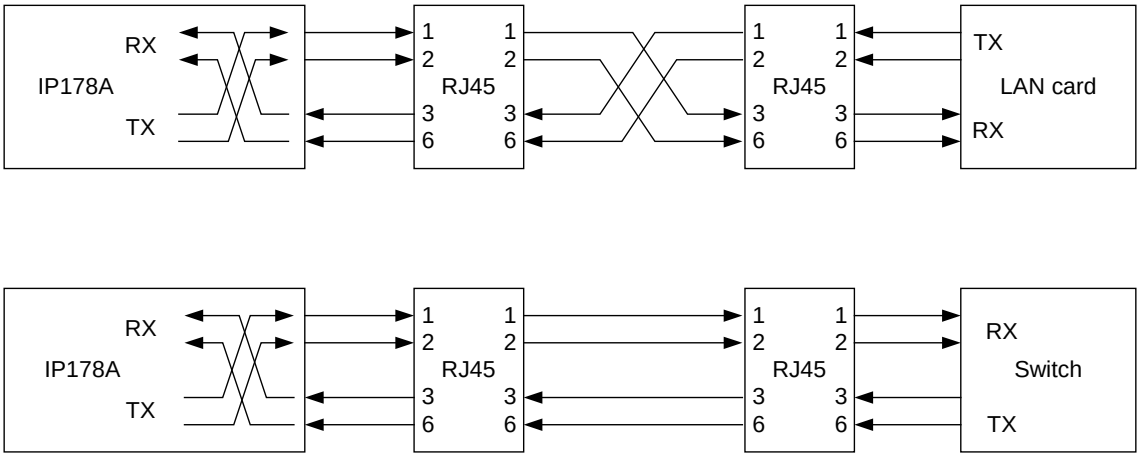
The VLAN function can be enabled even if there is no EEPROM. IP178A supports an easy way to utilize VLAN function without EEPROM. A specific configuration of VLAN is adopted if pin VLAN_ON is pulled high. It is benefit in a router application that an individual LAN port shares a WAN port but doesn't communicate each other. The VLAN group in this mode is illustrated in the pin description of VLAN_ON.

The VLAN function is enabled if pin VLAN_on is pulled high or filling the content of EEPROM register 07H~0AH. The setting in register takes precedence of the setting on pins.

MDI-MDIX

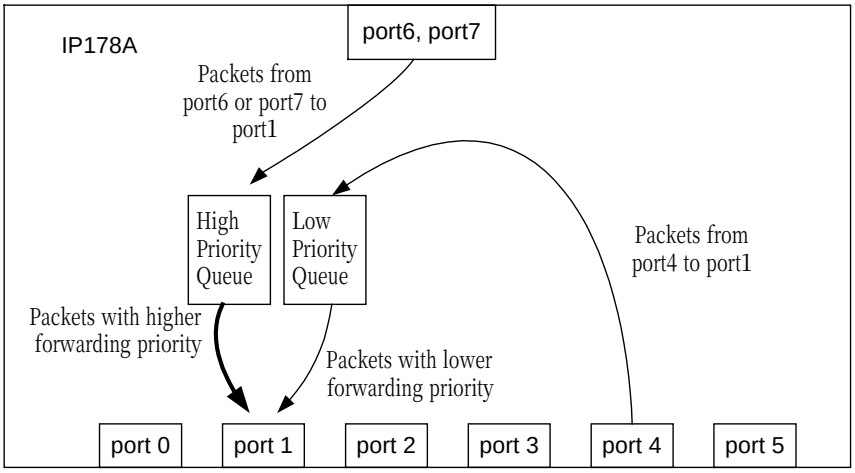


IP178A works at MDI mode

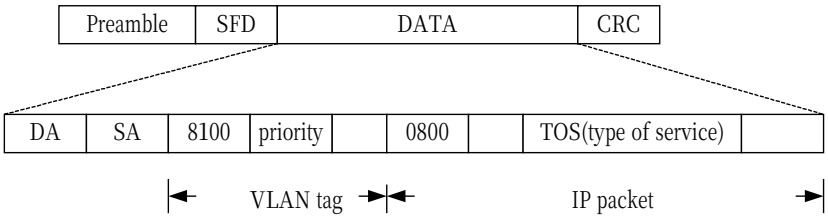


IP178A works at MDIX mode

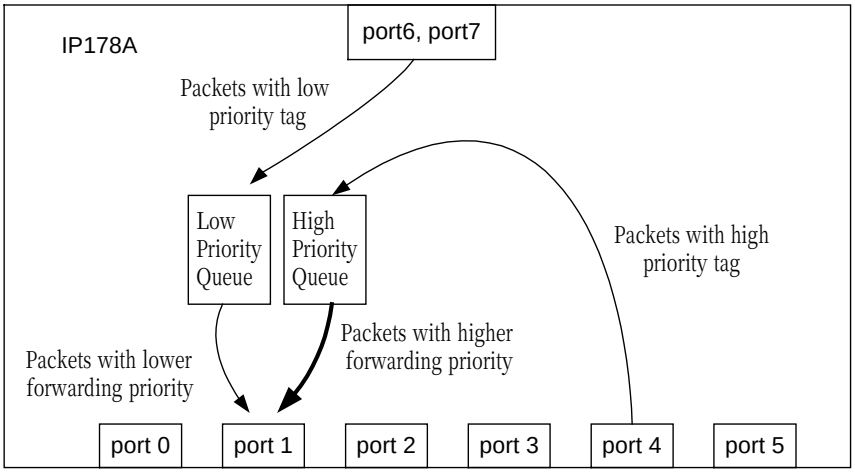
CoS



The port base Cos operation

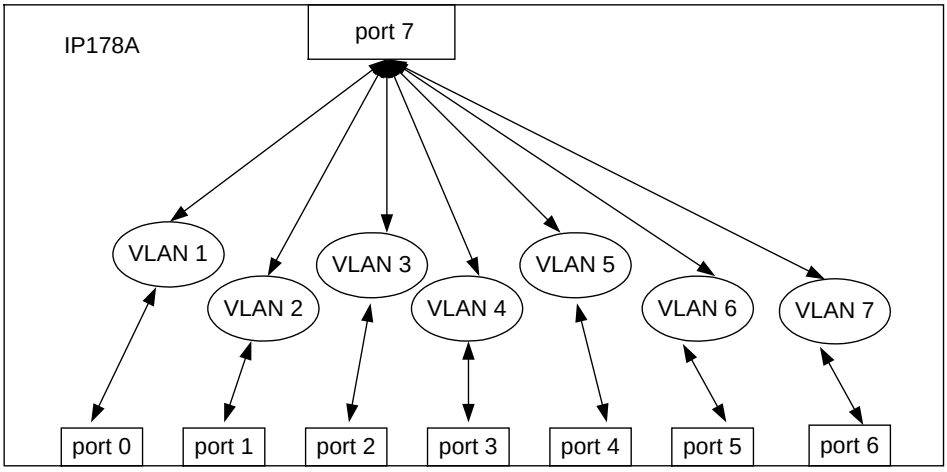


The frame format of frame base Cos

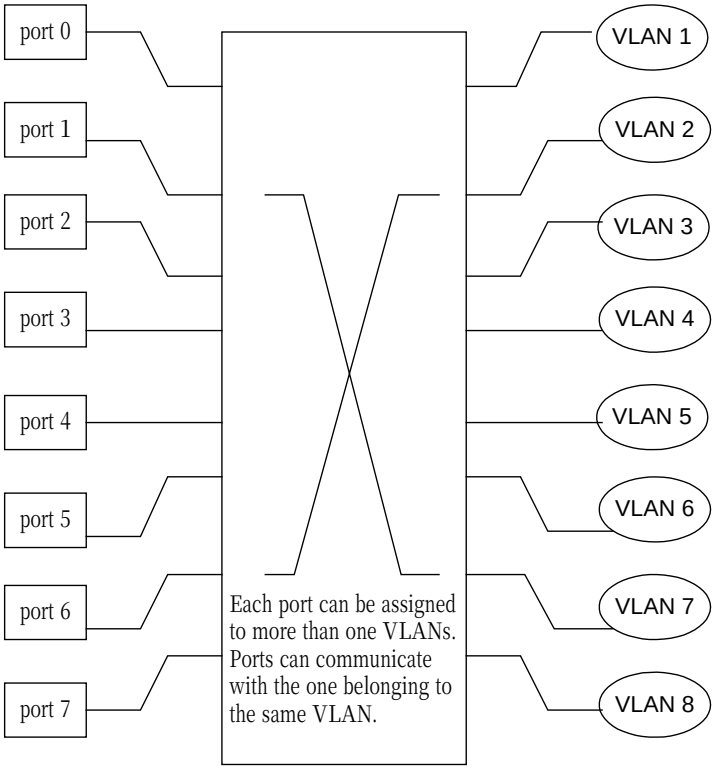


The frame base Cos operation

VLAN



The VALN group in IP178A when VLAN_ON pin is pulled high

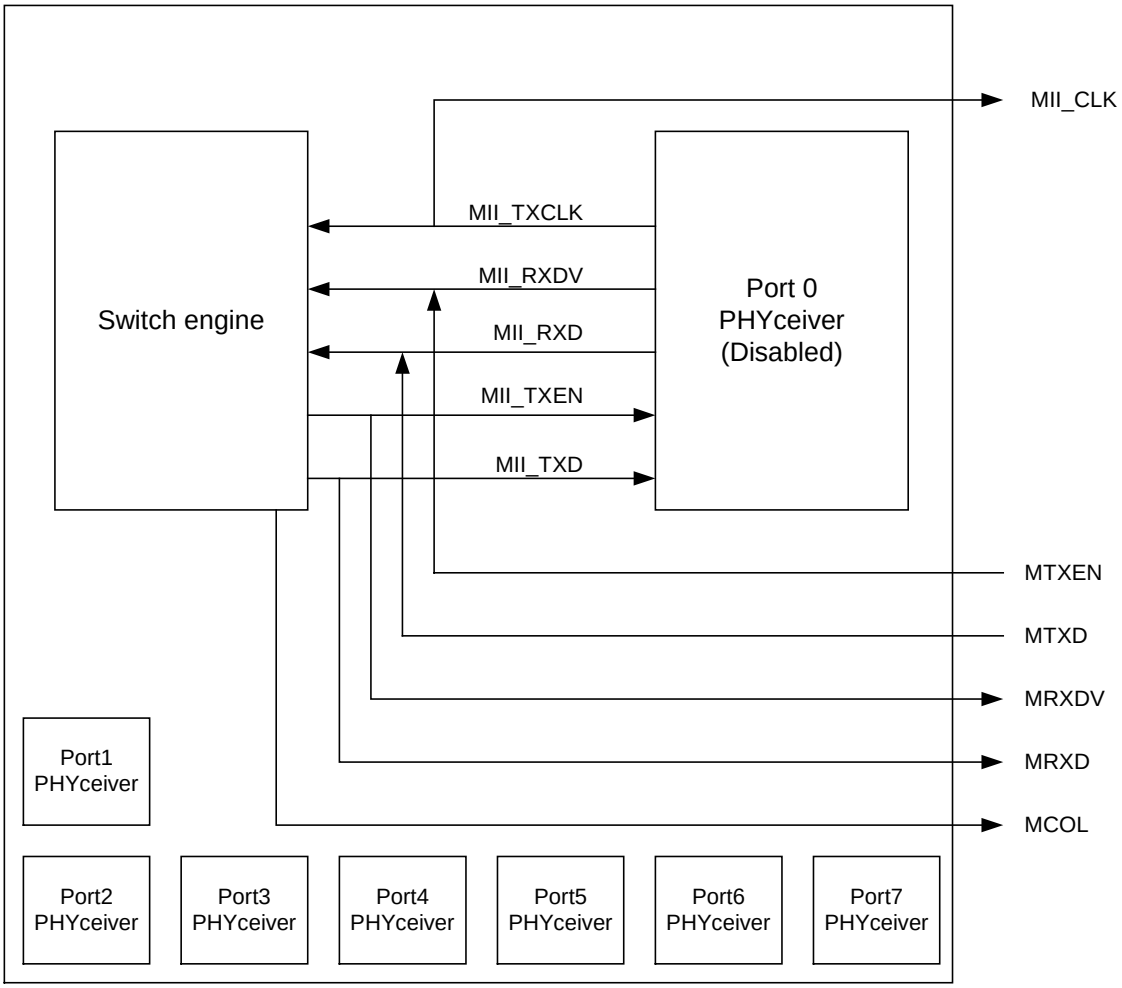


The VALN group in IP178A when VLAN registers are enabled

MII

IP178A supports one MII. When the interface is active (MII_P0_EXT_EN=1), the Phyceiver of port0 is disabled and the switch core interfaces the MII directly. This make IP178A can behave like a Fast Ethernet Phyceiver on port 0.

The major difference between the MII and IEEE standard MII are clock and RXER signals. There is only one clock and there is no RXER signal on the interface. For half duplex operation, MCOL is used as a collision during transmission. The following diagram illustrates the MII of IP178A.



IP178A works at 7TP + 1 MII mode

LED Interface

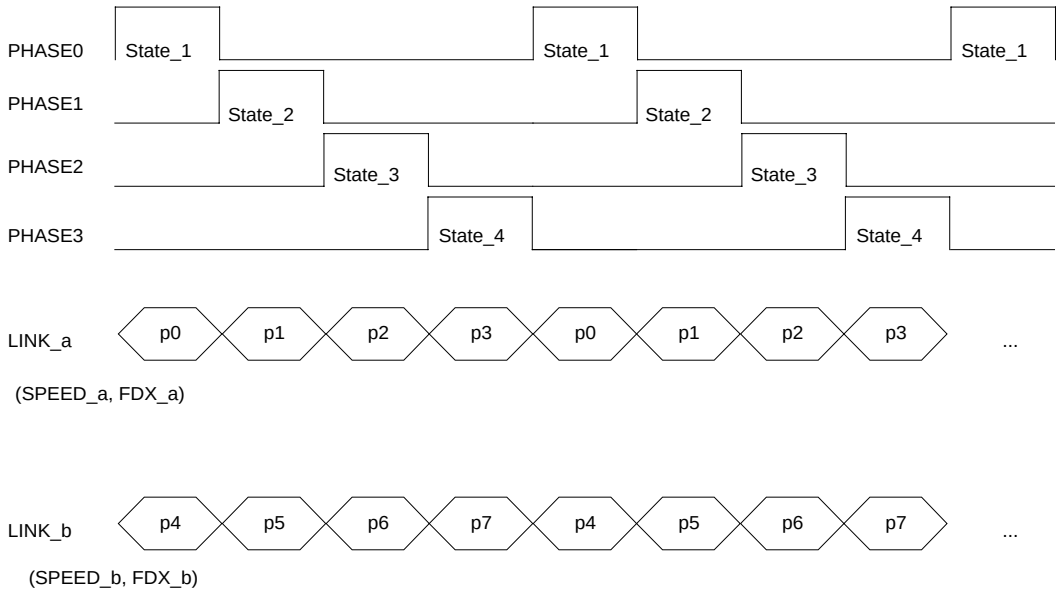
IP178A provides four kinds of LED information and two kinds of LED interfaces. The LED information is selected by LED_O_SEL[1:0] pins and the LED interface is selected by DIRECT_LED pin.

When IP178A works at direct mode (DIRECT_LED pin pulled high), it drives 24 LED pins directly to provide link, speed and fdx LED. The operation of link, speed and fdx LED are defined by LED_O_SEL[1:0] pins.

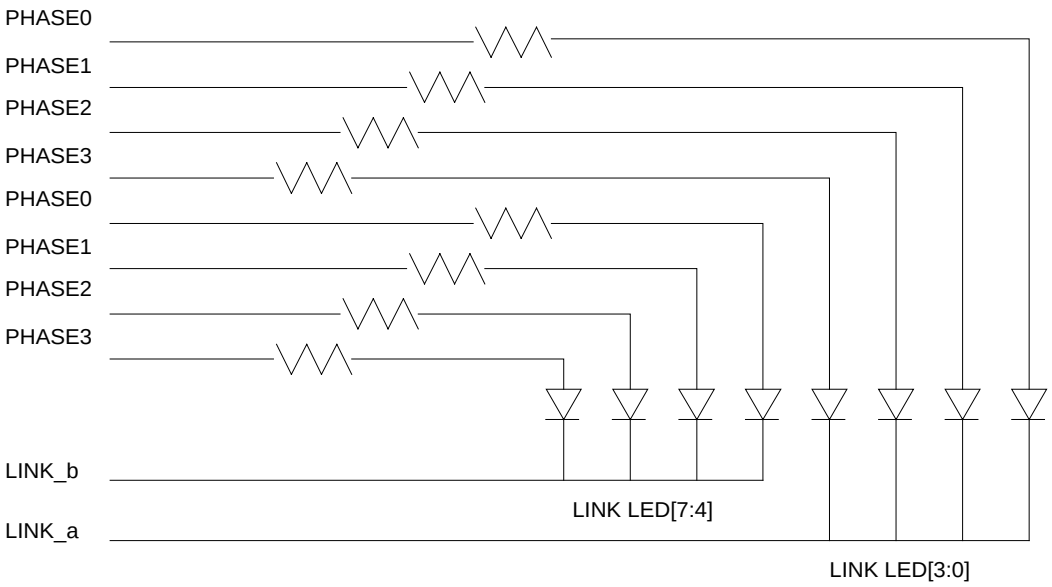
When IP178A works at scan mode (DIRECT_LED pin pulled low), it drives 12 LED control pins with scan mythology to provide link, speed, fdx and rx LED. The operation of link, speed, fdx and rx LED are defined by LED_O_SEL[1:0] pins.

When IP178A works at scan mode, phase pins run periodically to generate state_1 to state_4. Link_a sends out the link status of port0 at state_1 and Link_b sends out the link status of port4 at state_1. IP178A supports rx, fdx and speed LED in the same way. The detail description and waveforms are shown in the following diagram.

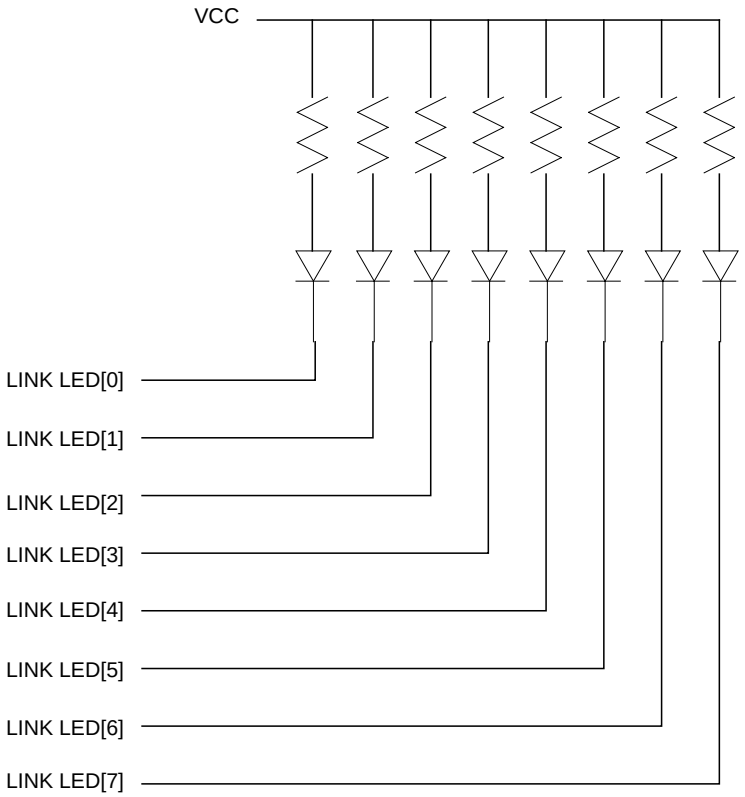
Label	State_1	State_2	State_3	State_4
PHASE0	1	0	0	0
PHASE1	0	1	0	0
PHASE2	0	0	1	0
PHASE3	0	0	0	1
LINK_A	Port0 link	Port1 link	Port2 link	Port3 link
RX_A	Port0 rx	Port1 rx	Port2 rx	Port3 rx
FDX_A	Port0 fdx	Port1 fdx	Port2 fdx	Port3 fdx
SPEED_A	Port0 speed	Port1 speed	Port2 speed	Port3 speed
LINK_B	Port4 link	Port5 link	Port6 link	Port7 link
RX_B	Port4 rx	Port5 rx	Port6 rx	Port7 rx
FDX_B	Port4 fdx	Port5 fdx	Port6 fdx	Port7 fdx
SPEED_B	Port4 speed	Port5 speed	Port6 speed	Port7 speed



Application circuit of link LED in scan mode



Application circuit of link LED in direct mode



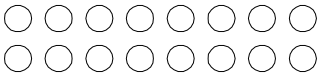
LED information

IP178A provides four types of LED function for link, rx, fdx, and speed. User can select the desired features by setting Led_o_sel[1:0]. The detail information is list in the following table. The default value is the same as the IP178A previous version. It is noted that Rx LED is supported in LED scan mode only.

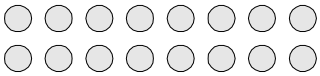
LED_O_SEL [1:0]	LINK LED[7:0]		RX LED[7:0]		FDX LED[7:0]		SPEED LED[7:0]	
00	On Off Flash	10M link ok 10M link fail ACT	Flash Off	collision idle	On Off	full duplex half duplex	On Off Flash	100M link ok 100M link fail ACT
01	On Off Flash	link ok link fail receive	Flash Off	rx/tx idle	On Off Flash	full duplex half duplex collision	On Off	100M 10M
10	On Off Flash	10M link ok 10M link fail ACT	Flash Off	collision idle	On Off Flash	full duplex half duplex collision	On Off Flash	100M link ok 10M link fail ACT
11 (default)	On Off Flash	link ok link fail rx/tx	Flash Off	collision idle	On Off Flash	full duplex half duplex collision	On Off	100M 10M

Power on Diagnostic of LED (LED array = 8 × 4)

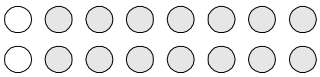
(0) T = 0 sec



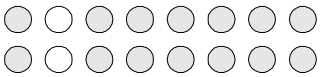
(1) T = 0.25 sec



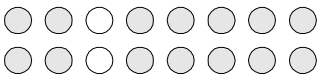
(2) T = 0.50 sec



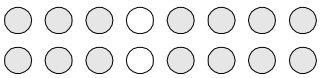
(3) T = 0.75 sec



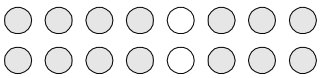
(4) T = 1.00 sec



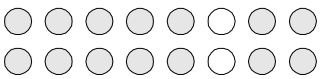
(5) T = 1.25 sec



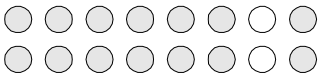
(6) T = 1.50 sec



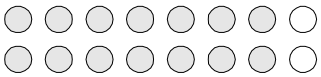
(7) T = 1.75 sec



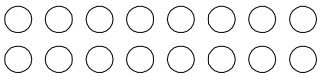
(8) T = 2.00 sec



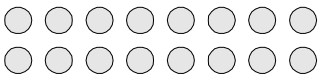
(9) T = 2.25 sec



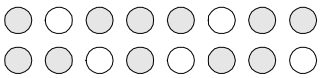
(10) T = 2.50 sec



(11) T = 2.75 sec



(12) After T = 3.0 sec, LED becomes normal operation

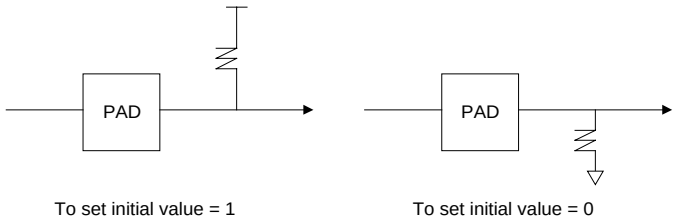


Operation parameters setting

IP178A supports two ways to modify its initial values of operation parameters to fit different applications. It read the initial value via pins or EPROM interface. The detail description of each pins and each bit in the EEPROM is illustrated in the next paragraph. Some settings are duplicated on pins. EEPROM setting takes precedence of resistor setting.

Initial value set via pins

To set the parameter via pins, connect them to VCC or ground through resistors. IP178A reads initial value via configuration pins during the period of reset. An initial value is set to 1 (0) by connecting a pin to VCC (GND) through a 10kΩ (1kΩ) resistor as shown on the following figure. IP178A begins to work after the internal PLL clock active. To make sure the proper operation of PLL, the duration of reset must be more than 1 ms. If there is no setting resistor, IP178A uses the default value.

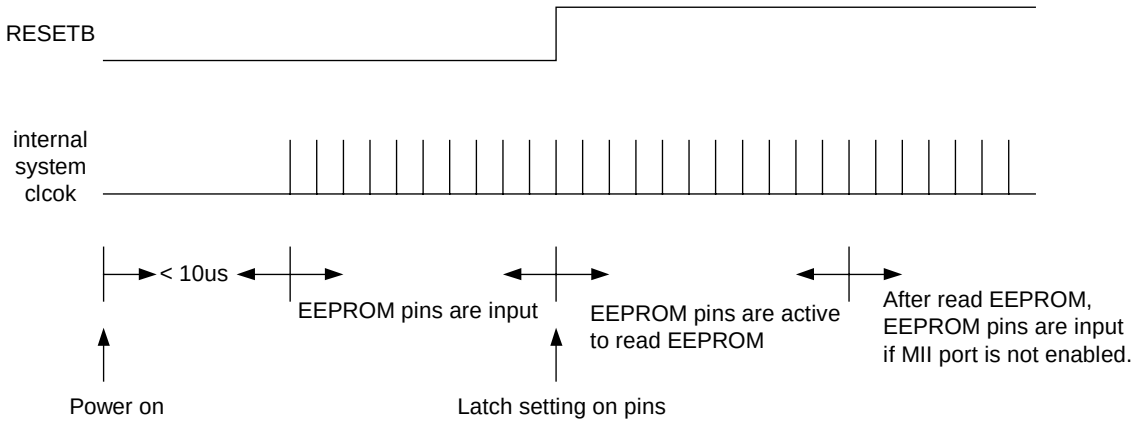


EEPROM Interface

During reset, the pins of EEPROM interface are input signals. At the end of reset, IP178A latches the setting on configuration pins and begins to read the content in the EEPROM. The data in EEPROM is valid only if there is a specific pattern 55AA found in the register 0. If there is no valid data in EEPROM, IP178A will keep the value read from resistors setting. After reading the EEPROM, the pins of EEPROM interface are input signals.

All fields in EEPROM corresponding to the registers of IP178A should be filled with correct value if an EEPROM is used. The initial value of IP178A will be replaced with the content in EEPROM if it is valid. That is, the EEPROM takes precedence of the pin setting.

IP178A uses a 93C46 EEPROM device. The detail operation of reading EEPROM is illustrated in the following figure.



EEPROM Register Description

Offset	Default Value	Corresponding Pin	Description
00H[15:0]	55AA	-	**EEPROM enable register** This register should be filled with 55AA. IP178A will examine the specified pattern to confirm if there is a valid EEPROM. The initial setting is updated with the content of EEPROM only if the specified pattern 55AA is found.
LED output selection register			
01H[15:2]	12'b0	-	**Reserved**
01H[1:0]	11	LED_O_SEL[1:0]	**LED_O_SEL, LED mode selection**

Bit1	Bit0	LINK a/b	RX a/b	FDX a/b	SPEED a/b
0	0	10 Link/act	Col	Fdx	100 link/act
0	1	Link/rt	Act	Fdx/col	Speed
1	0	10 Link/act	Col	Fdx/col	100 link/act
1	1	Link/act	Col	Fdx/col	Speed

Switch control register 1			
02H[15]	1'b0	COS_EN	**Class of service enable** 1: enable, 0: disabled (default) Packets with high priority tag are handled as high priority packets. It is enabled only if P6_7_high is disabled.
02H[14]	1'b0	P6_7_HIGH	**Port6 port7 are set to be high priority port** 1: enable, 0: disabled (default) Packets received from port6 or port7 are handled as high priority packets.
02H[13]	1'b0	-	**Reserved**
02H[12:11]	00	BP_KIND[1:0]	**Bp_kind, Backpressure type selection** It is valid only if Bk_en (02H[4]) is set to 1'b1. 00: carrier base backpressure 01: (reserved) 10: (reserved)
02H[10]	0	-	**Reserved**
02H[8]	0	-	**Reserved**
02H[7]	1	X_EN	X_en, IEEE 802.3x flow control enable 1: enable, 0:disable
02H[6:5]	2'b0	-	**Reserved**
02H[4]	1	BK_EN	**Bk_en, Backpressure enable** 1: enable, 0: disable

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
02H[3]	0	-	**Reserved**
02H[2]	0	BF_STM_EN	**Bf_stm_en, Broadcast storm enable** 1: enable IP178A drops the incoming packet if the number of broadcast packet in queue is over the threshold. 0: disable
02H[1:0]	2'b0	-	**Reserved**
Switch control register 2			
03H[15:13]	3'b0	-	**Reserved**
03H[12]	1	MII_P0_FULL	**Duplex of external MII port** 1: full (default), 0: half
03H[11]	1	MII_P0_SPEED	**Speed of external MII port** 1: 10M (default), 0: 100M
03H[10]	0	MII_P0_FLOW_CTL	**Flow control of external MII port** 1: on, 0: off (default)
03H[9]	0	MII_P0_EXT_EN	**External MII port enable** 1: enable, 0: disable (default)
03H[8]	0	-	**Reserved**
03H[7]	0	DROP16	**Drop16**, A port will drop the transmitting packet after 16 consecutive collisions if this function is turned on. 1: drop, 0: not drop
03H[6:5]	00	HASH_MODE[1:0]	It is hashing algorithm selection for 1st layer and 2nd layer at the end of reset. 00: direct and CRC(default) 01: direct and CRC 10: CRC and CRC 11: reserved
03H[4:3]	10	AGETIME[1:0]	**Agetime, Aging time of address table selection** An address tag in hashing table will be removed if this function is turned on and its aging timer expires. 03H[4:3] / **Aging time** / **note** 00 / no aging / 01 / 120s / 10 / 240s / default 11 / 480s /
03H[2]	0	ALLPASS	**ALLPASS** IP178A forwards all packets. It is for testing only. The default value must be adopted for normal operation. 1: turn on, 0: turn off
03H[1]	1	MODBCK	**MODBCK, Turn on modified back off algorithm** The maximum back off period is limited to 8-slot time if this function is turned on. 1: turn on, 0: turn off
03H[0]	0	-	**Reserved**

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
Transceiver control register			
04H[15:14]	00	OP1[1:0]	**OP1** Bit[15:14] are corresponding to op1[1:0] The default value must be adopted for normal operation.
04H[13:11]	000	OP0[1:0], FORCE_ MODE	**OP0 and FORCE_MODE** Bit[13:11] are corresponding to op0[1:0] and force_mode The default value must be adopted for normal operation.
Summary			

04H[15:11]	**OP1 [1:0]**	**OP0 [1:0]**	**FORCE_ MODE**	**Description**
	0 0	x	0	Port1, 3, 5, 7 nway with all capability, mode0
	1 0	x	0	Port7 FX full duplex, port1, 3, 5 mode0
	1 1	x	0	Port7 FX half duplex, port1, 3, 5 mode0
	x	0 0	0	Port0, 2, 4, 6 nway with all capability, mode0
	x	1 0	0	Port6 FX full duplex, port0, 2, 4 mode0
	x	1 1	0	Port6 FX half duplex, port0, 2, 4 are mode0

04H[10]	1	FEF_EN	**Fef_en, Far end fault enable** 1: enable, 0: disable
04H[9]	1	SAVEPW_A_EN	**Savepw_a_en**, Save power mode for auto-negotiation 1: enable, 0: disable The default value must be adopted for normal operation.
04H[8]	0	MDI_MDIX_EN	**MDI/MDI-X enable** 1: enable, 0:disable
04H[7:0]	8'b0		

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
Transceiver verification register			
05H[15:14]	2'b0	-	**Reserved**
05H[13]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[12]	1	UPDATE_R4_EN	**Update_r4_en, Change capability enable** A full duplex port will change its capability to half duplex, if the remote node works at full duplex and does not support IEEE802.3x and this function is enabled. 1: enable, 0: disable
05H[11]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[10]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[9]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[8]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[7:6]	00	-	This function is for testing only. The default value must be adopted for normal operation.
05H[5]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[4]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[3]	1	UTP_DET#	**Utpdet, UTP detect enable** Fewer FLP will be sent out if cable is unplugged and the function is enabled. 1: disable, 0: enable The default value is suggested for normal operation.
05H[2]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[1]	0	-	This function is for testing only. The default value must be adopted for normal operation.
05H[0]	0	-	This function is for testing only. The default value must be adopted for normal operation.
Testing & verify mode register			
06H[15:7]	9'b0	-	**Reserved**
06H[6]	0	-	This function is for testing only. The default value must be adopted for normal operation.
06H[5:0]	6'b0	-	This function is for testing only. The default value must be adopted for normal operation.

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
VLAN register 1			
07H[15:8]	8'hff	-	**Port1 VLAN look up table** The register defines the ports in the same VLAN as port1. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port1 0: a port is not in the same VLAN as port1 Bit8=1, port 0 and port1 are in the same VLAN; Bit9, don't care; Bit10=1, port 2 and port1 are in the same VLAN; Bit11=1, port 3 and port1 are in the same VLAN; Bit12=1, port 4 and port1 are in the same VLAN; Bit13=1, port 5 and port1 are in the same VLAN; Bit14=1, port 6 and port1 are in the same VLAN; Bit15=1, port 7 and port1 are in the same VLAN;
07H[7:0]	8'hff	-	**Port0 VLAN look up table** The register defines the ports in the same VLAN as port0. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port0 0: a port is not in the same VLAN as port0 Bit0, don't care; Bit1=1, port 1 and port0 are in the same VLAN; Bit2=1, port 2 and port0 are in the same VLAN; Bit3=1, port 3 and port0 are in the same VLAN; Bit4=1, port 4 and port0 are in the same VLAN; Bit5=1, port 5 and port0 are in the same VLAN; Bit6=1, port 6 and port0 are in the same VLAN; Bit7=1, port 7 and port0 are in the same VLAN;

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
VLAN register 2			
08H[15:8]	8'hff	-	**Port3 VLAN look up table** The register defines the ports in the same VLAN as port3. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port3 0: a port is not in the same VLAN as port3 Bit8=1, port 0 and port3 are in the same VLAN; Bit9=1, port 1 and port3 are in the same VLAN; Bit10=1, port 2 and port3 are in the same VLAN; Bit11, don't care; Bit12=1, port 4 and port3 are in the same VLAN; Bit13=1, port 5 and port3 are in the same VLAN; Bit14=1, port 6 and port3 are in the same VLAN; Bit15=1, port 7 and port3 are in the same VLAN;
08H[7:0]	8'hff	-	**Port2 VLAN look up table** The register defines the ports in the same VLAN as port2. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port2 0: a port is not in the same VLAN as port2 Bit0=1, port 0 and port2 are in the same VLAN; Bit1=1, port 1 and port2 are in the same VLAN; Bit2, don't care; Bit3=1, port 3 and port2 are in the same VLAN; Bit4=1, port 4 and port2 are in the same VLAN; Bit5=1, port 5 and port2 are in the same VLAN; Bit6=1, port 6 and port2 are in the same VLAN; Bit7=1, port 7 and port2 are in the same VLAN;

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
VLAN register 3			
09H[15:8]	8'hff	-	**Port5 VLAN look up table** The register defines the ports in the same VLAN as port5. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port5 0: a port is not in the same VLAN as port5 Bit8=1, port 0 and port5 are in the same VLAN; Bit9=1, port 1 and port5 are in the same VLAN; Bit10=1, port 2 and port5 are in the same VLAN; Bit11=1, port 3 and port5 are in the same VLAN; Bit12=1, port 4 and port5 are in the same VLAN; Bit13, don't care; Bit14=1, port 6 and port5 are in the same VLAN; Bit15=1, port 7 and port5 are in the same VLAN;
09H[7:0]	8'hff	-	**Port4 VLAN look up table** The register defines the ports in the same VLAN as port4. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port4 0: a port is not in the same VLAN as port4 Bit0=1, port 0 and port4 are in the same VLAN; Bit1=1, port 1 and port4 are in the same VLAN; Bit2=1, port 2 and port4 are in the same VLAN; Bit3=1, port 3 and port4 are in the same VLAN; Bit4, don't care; Bit5=1, port 5 and port4 are in the same VLAN; Bit6=1, port 6 and port4 are in the same VLAN; Bit7=1, port 7 and port4 are in the same VLAN;

EEPROM Register Description (continued)

Offset	Default Value	Corresponding Pin	Description
VLAN register 4			
0AH[15:8]	8'hff	-	**Port7 VLAN look up table** The register defines the ports in the same VLAN as port7. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port7 0: a port is not in the same VLAN as port7 Bit8=1, port 0 and port7 are in the same VLAN; Bit9=1, port 1 and port7 are in the same VLAN; Bit10=1, port 2 and port7 are in the same VLAN; Bit11=1, port 3 and port7 are in the same VLAN; Bit12=1, port 4 and port7 are in the same VLAN; Bit13=1, port 5 and port7 are in the same VLAN; Bit14=1, port 6 and port7 are in the same VLAN; Bit15, don't care;
0AH[7:0]	8'hff	-	**Port6 VLAN look up table** The register defines the ports in the same VLAN as port6. The bit 0~7 are corresponding to port 0~7. 1: a port is in the same VLAN as port6 0: a port is not in the same VLAN as port6 Bit0=1, port 0 and port6 are in the same VLAN; Bit1=1, port 1 and port6 are in the same VLAN; Bit2=1, port 2 and port6 are in the same VLAN; Bit3=1, port 3 and port6 are in the same VLAN; Bit4=1, port 4 and port6 are in the same VLAN; Bit5=1, port 5 and port6 are in the same VLAN; Bit6, don't care; Bit7=1, port 7 and port6 are in the same VLAN;

A summary of EEPROM registers and their corresponding pins

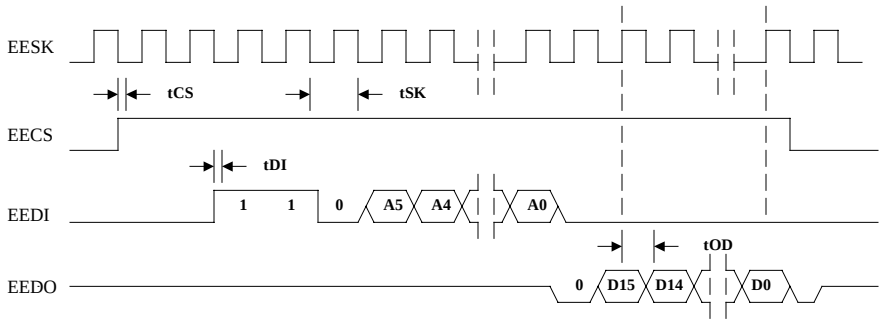
Offset	Default	Corresponding pin	Description	Register content
00H[15:0]	55AA	-		PROM ENABLE
01H[1:0]	11	LED_O_SEL[1:0]		LED_O_SEL
02H[15]	0	COS_EN		COS_EN
02H[14]	0	P6_7_HIGH		P6_7_HIGH
02H[12:11]	00	BP_KIND[1:0]		BP_KIND
02H[7]	1	X_EN		X_EN
02H[4]	1	BK_EN		BK_EN
02H[2]	0	BF_STM_EN		BF_STM_EN
03H[12]	1	MII_P0_FULL		MII_P0_FULL
03H[11]	1	MII_P0_SPEED		MII_P0_SPEED
03H[10]	0	MII_P0_FLOW_CTL		MII_P0_FLOW_CTL
03H[9]	0	MII_P0_EXT_EN		MII_P0_EXT_EN
03H[7]	0	DROP16		DROP16
03H[6:5]	00	HASH_MODE [1:0]		HASH_MODE[1:0]
03H[4:3]	10	AGETIME[1:0]		AGETIME
03H[2]	0	--		ALLPASS
03H[1]	1	MODBCK		MODBCK
04H[15]	0	OP1[1]		OP1[1]
04H[14]	0	OP1[0]		OP1[0]
04H[13]	0	OP0[1]		OP0[1]
04H[12]	0	OP0[0]		OP0[0]
04H[11]	0	FORCE_MODE		FORCE_ MODE
04H[10]	1	FEF_EN		FEF_EN
04H[9]	1	SAVEPW_A_EN		SAVEPW_A_EN
04H[8]	0	MDI_MDIX_EN		MDI_MDIX_EN
04H[7:0]	8'b0	-		-
05H[13]	0	-		-
05H[12]	1	UPDATE_R4_EN		UPDATE_R4_EN
05H[11]	0	-		-
05H[10]	0	-		-
05H[9]	0	-		-
05H[8]	0	-		-
05H[7:6]	00	-		-
05H[5]	0	-		-
05H[4]	0	-		-
05H[3]	1	UTP_DET#		UTP_DET#
05H[2]	0	-		-
05H[1]	0	-		-
05H[0]	0	-		-
06H[6]	0	-		-
06H[5]	0	-		-
06H[4]	0	-		-
06H[3]	0	-		-
06H[2]	0	-		-
06H[1]	0	-		-
06H[0]	0	-		-

A summary of EEPROM registers and their corresponding pins (continued)

Offset	Default	Corresponding pin	Description	Register content
07H[15:8]	8'hff	-		PORT1 VALN TABLE
07H[7:0]	8'hff	-		PORT0 VALN TABLE
08H[15:8]	8'hff	-		PORT3 VALN TABLE
08H[7:0]	8'hff	-		PORT2 VALN TABLE
09H[15:8]	8'hff	-		PORT5 VALN TABLE
09H[7:0]	8'hff	-		PORT4 VALN TABLE
0AH[15:8]	8'hff	-		PORT7 VALN TABLE
0AH[7:0]	8'hff	-		PORT6 VALN TABLE

AC Characteristic

Read EEPROM



Parameter	Description	Min	Typical	Max	Units
TSK	Clock period		5.12		us
TCS	Chip select delay			2	ns
TDI	Data input delay			2	ns
TOD	Output delay			2000	ns

Absolute Maximum Rating

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Functional performance and device reliability are not guaranteed under these conditions. All voltages are specified with respect to GND.

Supply Voltage	–0.3V to 4.0V
Input Voltage	–0.3V to 5.0V
Output Voltage	–0.3V to 5.0V
Storage Temperature	-65°C to 150°C
Ambient Operating Temperature (Ta)	0°C to 70°C

DC Characteristic

■ Operating Conditions

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VCC2.5	2.375	2.5	2.625	V	
	TXVCC	2.375	2.5	2.625	V	
Power Consumption			2.9		W	All ports link at 10M/ full.
			2.75		W	All ports link at 100M/ full.
			1.55		W	Unlink situation

■ Input Clock

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Frequency			25		MHz	
Frequency Tolerance		-50		+50	PPM	

■ I/O Electrical Characteristics

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Input Low Voltage	VIL			0.8	V	
Input High Voltage	VIH	2.0			V	
Output Low Voltage	VOL			0.4	V	IOH=4mA, VCC=3.3V
Output High voltage	VOH	2.4			V	IOL=4mA, VCC=3.3V

■ **TX Transceiver Electrical Characteristics**

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Peak Differential Output Voltage	VP	0.95	1.0	1.05	V	
Signal Amplitude Symmetry	-	98	100	102	%	
Signal Rise/Fall Time	TRF	3	4	5	ns	
Rise/Fall Time Symmetry	TRFS			0.5	ns	
Duty Cycle Distortion	-			0.5	ns	
Overshoot	VO			5	%	

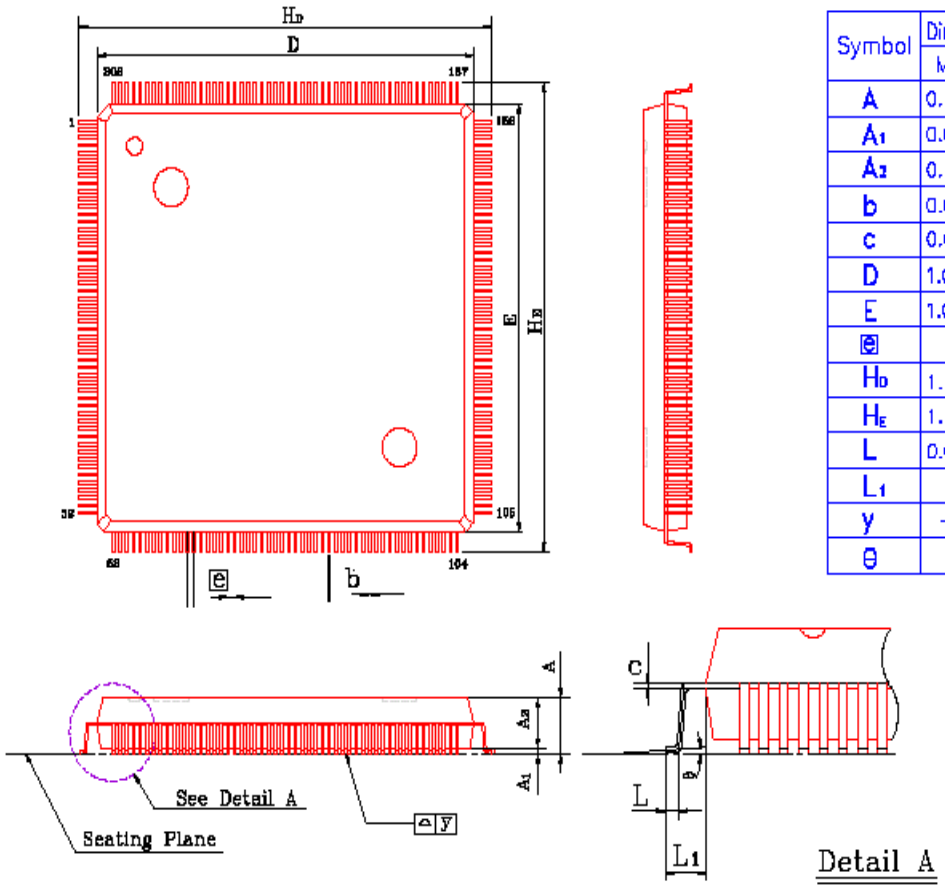
Order Information

Part No.	PIN	Notice
IP178A	208 PIN PQFP	-

Package Detail

QFP 208L Outline Dimensions

Unit: Inches/mm



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	0.154	—	0.160	3.92	—	4.07
A_1	0.010	—	—	0.25	—	—
A_2	0.124	0.127	0.130	3.15	3.23	3.30
b	0.007	—	0.011	0.18	—	0.28
c	0.005	—	0.009	0.13	—	0.23
D	1.098	1.102	1.106	27.90	28.00	28.10
E	1.098	1.102	1.106	27.90	28.00	28.10
e	0.020 BSC			0.50 BSC		
H_D	1.195	1.205	1.215	30.35	30.60	30.85
H_E	1.195	1.205	1.215	30.35	30.60	30.85
L	0.014	0.020	0.026	0.35	0.50	0.65
L_1	0.051 REF			1.30 REF		
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°