



P-Channel 150-V (D-S) MOSFET

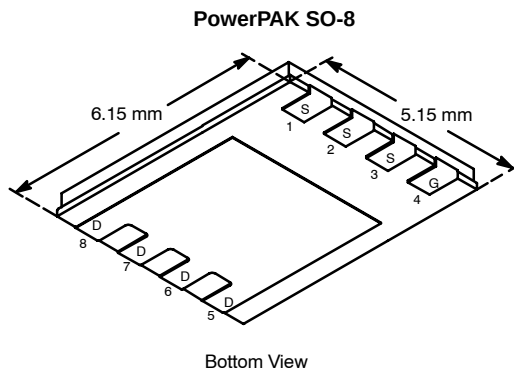
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-150	0.090 @ $V_{GS} = -10$ V	-5.2
	0.095 @ $V_{GS} = -6$ V	-5.0

FEATURES

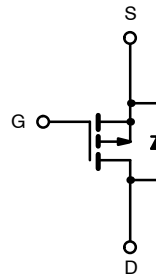
- TrenchFET® Power MOSFETS
- Ultra-Low On-Resistance Critical for Application
- Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- 100% R_g and Avalanche Tested

APPLICATIONS

- Active Clamp in Intermediate DC/DC Power Supplies



Ordering Information: Si7439DP-T1—E3



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	−150		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	−5.2	−3.0	A
	T _A = 70°C		−4.1	−2.4	
Pulsed Drain Current		I _{DM}	−50		
Continuous Source Current (Diode Conduction) ^a		I _S	−4.2	−1.6	
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	−40		
Single Pulse Avalanche Energy		E _{AS}	80		
Maximum Power Dissipation ^a	T _A = 25°C	P _D	5.4	1.9	W
	T _A = 70°C		3.4	1.2	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS				
Parameter		Symbol	Typical	Maximum
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	18	23
	Steady State		50	65
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.5

Notes

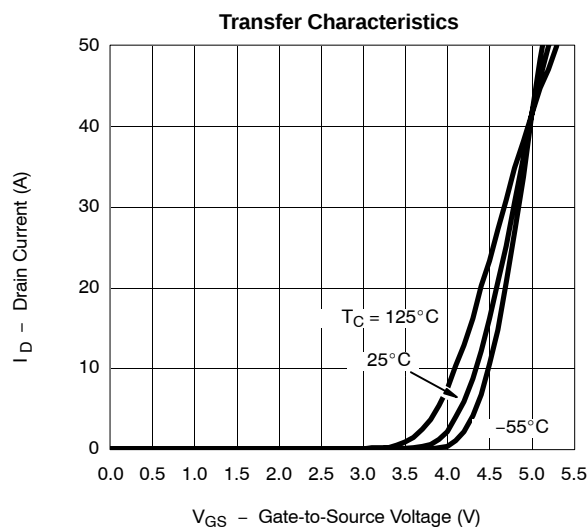
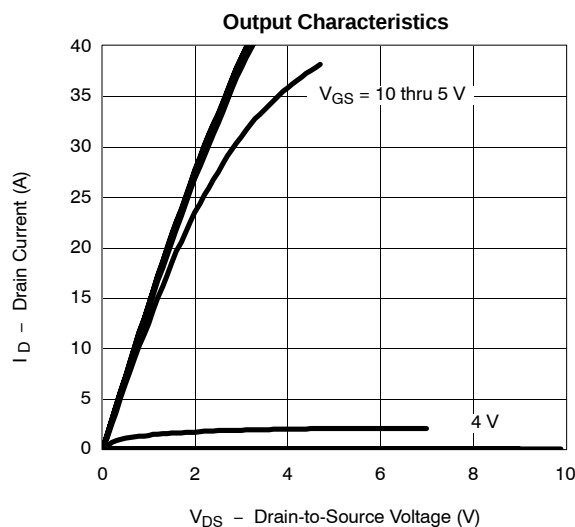
a. Surface Mounted on 1" x 1" FR4 Board.

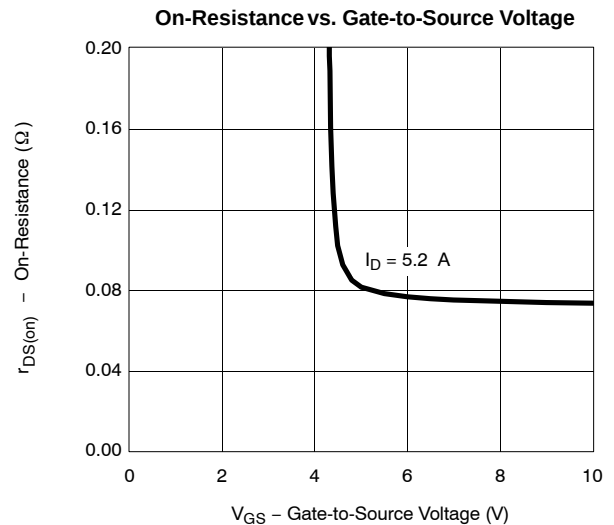
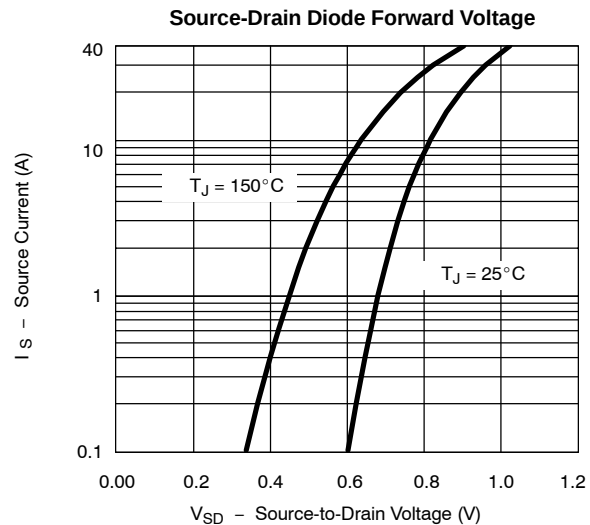
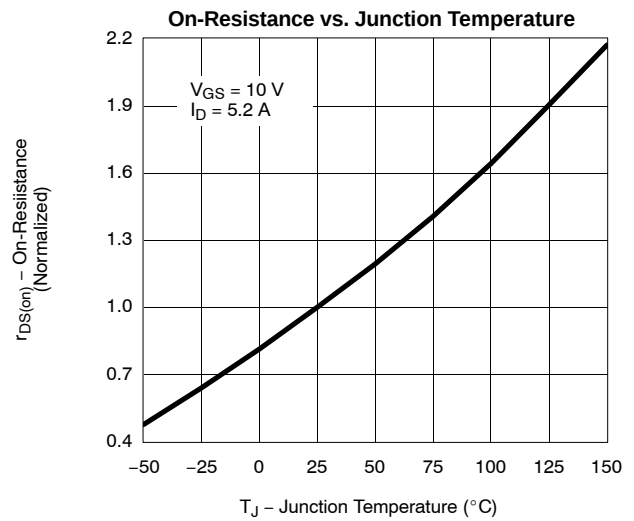
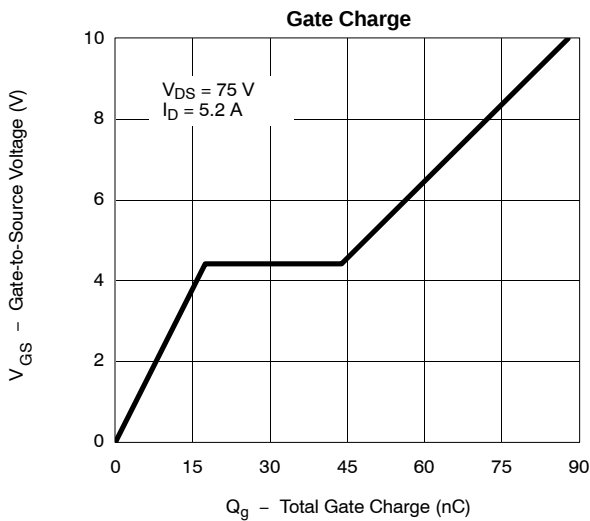
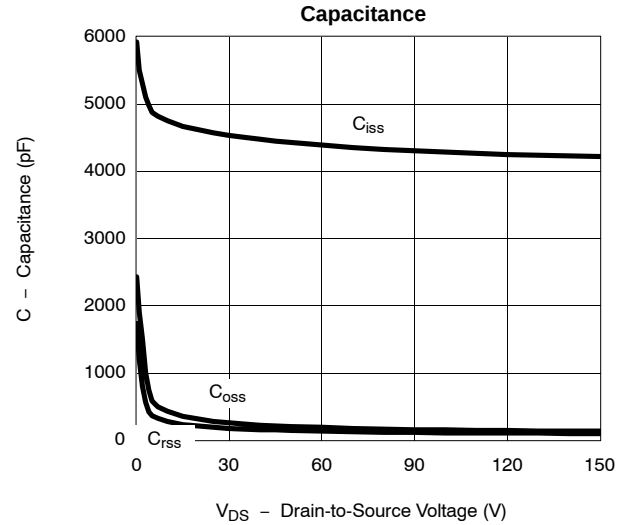
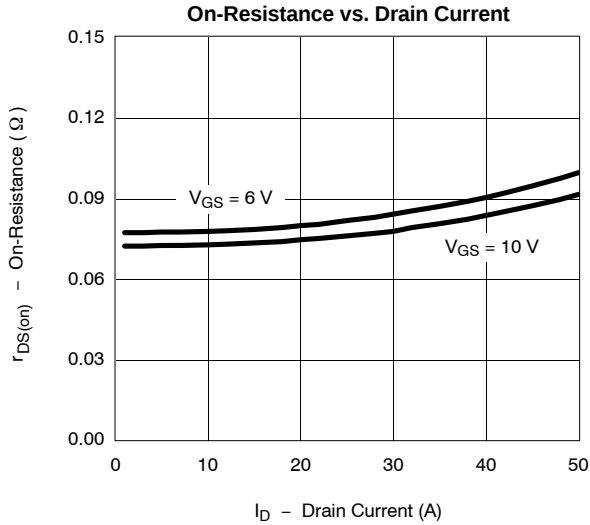
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

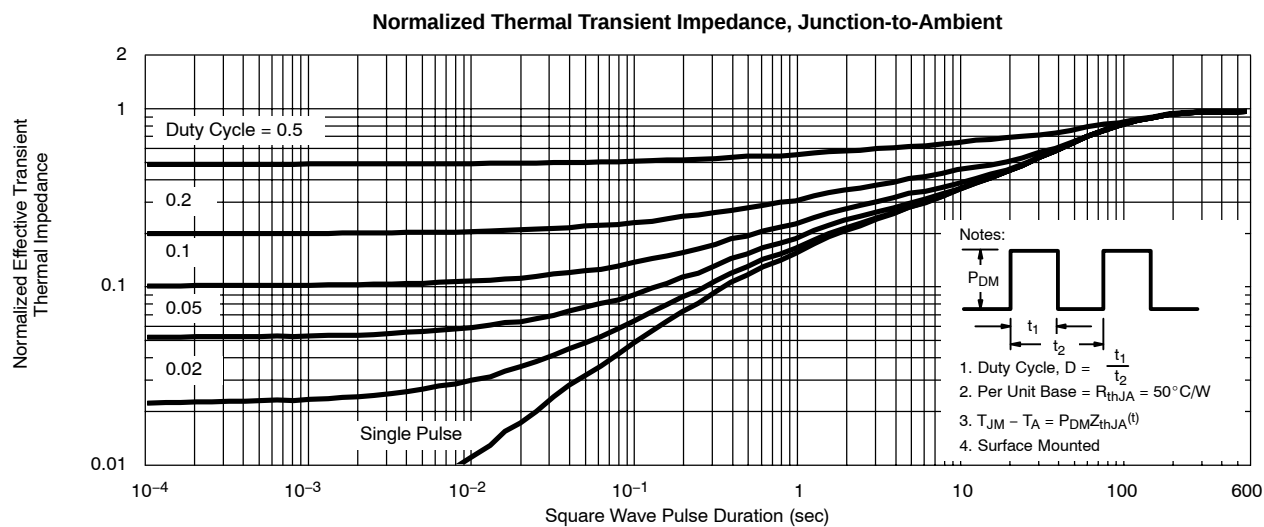
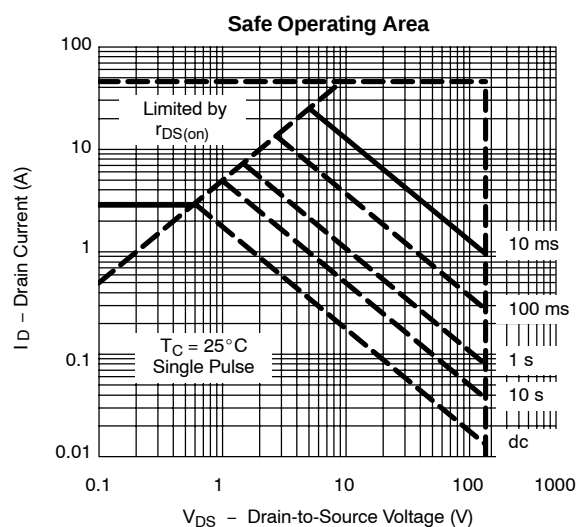
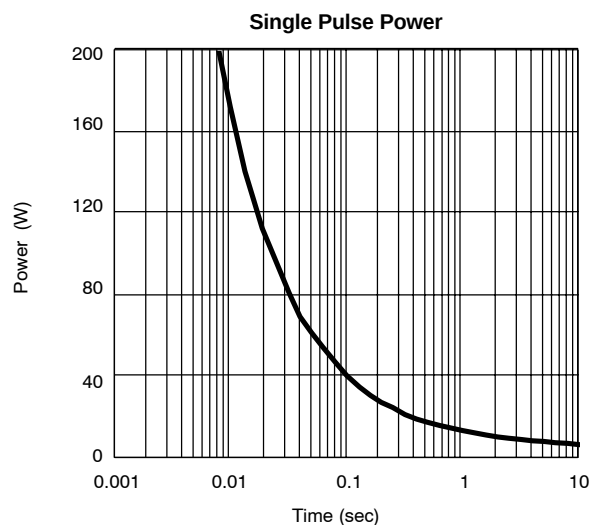
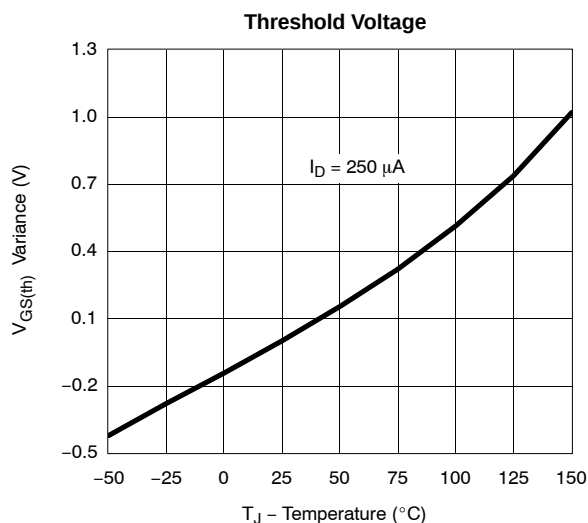
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0		-4.0	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -150\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -150\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 70^\circ\text{C}$			-10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -10\ \text{V}, V_{GS} = -10\ \text{V}$	-30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -5.2\ \text{A}$		0.073	0.090	Ω
		$V_{GS} = -6\ \text{V}, I_D = -5.0\ \text{A}$		0.077	0.095	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -5.2\ \text{A}$		19		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -4.2\ \text{A}, V_{GS} = 0\ \text{V}$		-0.78	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -75\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -5.2\ \text{A}$		88	135	nC
Gate-Source Charge	Q_{gs}			17.5		
Gate-Drain Charge	Q_{gd}			26.5		
Gate Resistance	R_g		1.5	3	4.5	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -75\ \text{V}, R_L = 15.5\ \Omega$ $I_D \cong -4.8\ \text{A}, V_{GEN} = -10\ \text{V}, R_g = 6\ \Omega$		25	40	ns
Rise Time	t_r			46	70	
Turn-Off Delay Time	$t_{d(off)}$			115	180	
Fall Time	t_f			64	100	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.9\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		100	150	

Notes

- a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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