SIEMENS

SIEMENS AKTIENGESELLSCHAF

Data Slicer for Teletext

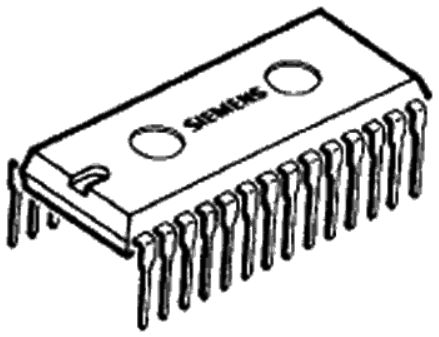
SDA 5231-2

Preliminary Data

Bipolar IC

Features

- Crystal-stable data clock regeneration for a bit rate of 6.9375 MHz
- Separation and regeneration of teletext information
- Separation of the horizontal and vertical synchronization signals
- Phase-locked coupling of 6-MHz oscillator with comp. video
- Optional adjustment to 1 V or 2.5 V comp. video level
- Processing of externally separated teletext data
- Output of negative and positive synchronous signals to television set



VPD 05097

P-DIP-28

Type	Ordering Code	Package
SDA 5231-2	Q 67000-A5006	P-DIP-28

The SDA 5231-2 has been designed to separate teletext signals from TV signals for a microcontroller-operated I²C bus concept. The video processor meets the requirements for teletext data clock regeneration and synchronization of the TV set during teletext operation. At the same time, the video signals (CVBS) provided by the television set are evaluated for the teletext decoder.

Functional Description

The SDA 5231-2 is used in an I²C bus controlled teletext system. Its function is the processing of the teletext informations, the system clock generation and the switching of HV synchronization signals.

The SDA 5231-2 can also be used to process the data line 16 (VPS).

a) **Signal Processing**

The analog signal is processed at the amplitude filter (clamping of the video input signal and separation of the sync. impulse) and by means of the data slicing level. The data slicer compensates the attenuation of the data signal due to mistuning and a non linear frequency response the IF-amplifier.
As in case of sync. impulse separation, an adaptive circuit is used for separating the data, i.e. the clipping level is always in the middle of the sync. impulse and/or the data signal, independent of the signal amplitude.
Both the clipping level and the control voltage for the AGC (Automatic Gain Control) are generated while bit synchronization takes place at the beginning of the teletext line and are stored until the teletext line has been fully scanned.

b) **Synchronization of Data Clock**

Clock synchronization is obtained by means of a phase detector + a phaseshifter.
A control voltage proportional to the phase difference between the free running oscillator and the incoming data bits is generated by the phase detector. A small time constant is used during bit synchronization, for the rest of the time a 10 times larger constant is used.

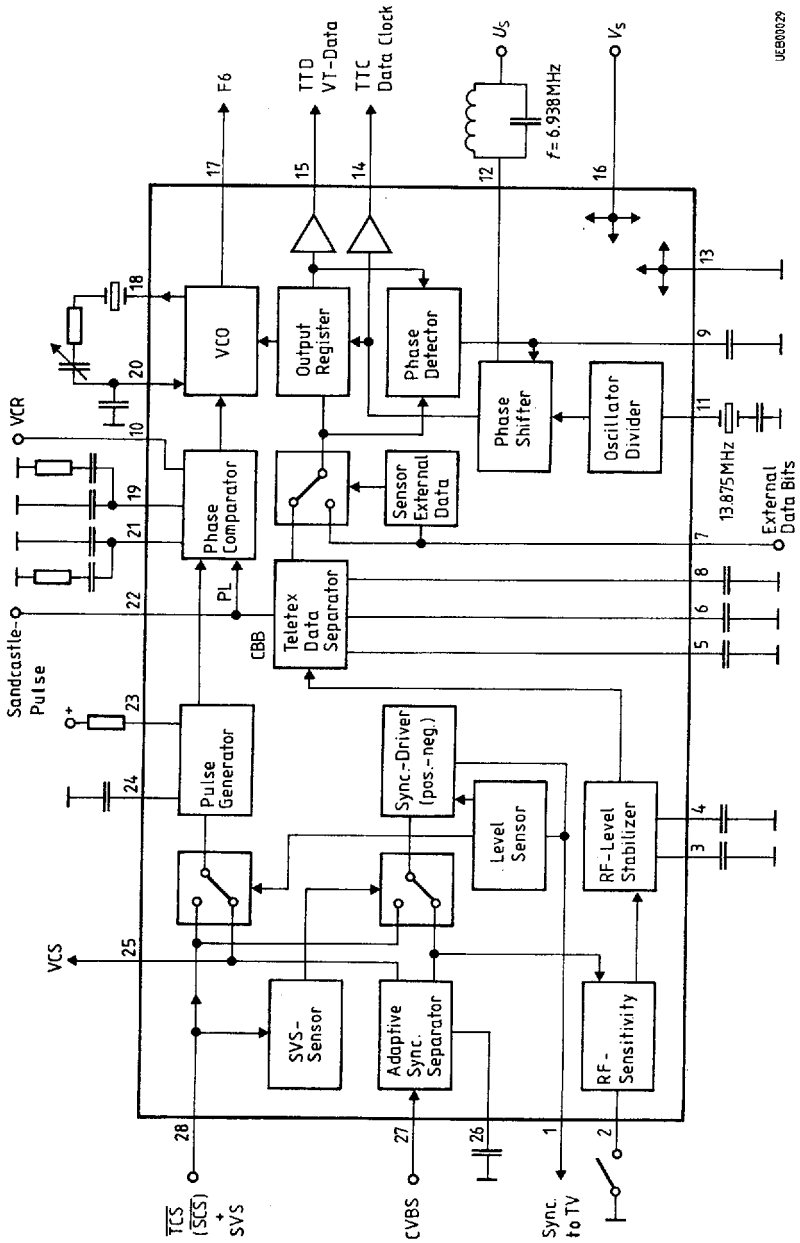
c) **Generation of 6-MHz System Clock**

The teletext processor generates a picture pixel raster from the 6-MHz system clock. Thus, synchronization of the 6-MHz clock with the CVBS line frequency is necessary for any mixed-mode with teletext.
By shortening all sync. impulses to approximately 2 µs, interference from synchronization frame pulses can be avoided by means of a mono flop. The SANDCASTLE derived from the 6-MHz clock signal is synchronized in a phase-locked loop to the shortened sync. impulse. A shorter time constant is used during synchronization: If the CVBS signal is noisy or during after-hours operation, 2 points are important: Data acquisition has to be stopped, and the 6-MHz VCO must oscillate with its nominal frequency. For this purpose the teletext processor controls the VCS signal and switches off the signal component PL of the SANDCASTLE signal, if the CVBS signal is noisy or does not exist.

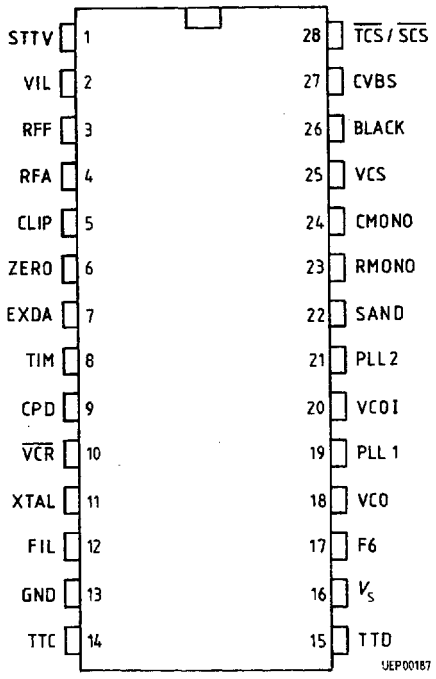
d) **Operating-Mode Switch**

Operation Mode	**Switch by**	**System Clock Sync. to**	**Usage**
CVBS	Pin 28 = NC	CVBS	i.e. sub-titles
TCS	$V_{28} < 6.1$ V	CVBS	interlace/non-interlace mode
SCS	Pin 1 = NC	SCS	Slave-Mode i.e. external synchronization

Block Diagram



Pin Configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Function	Description
1	STTV	Sync.-output	**Sync.-Output:** positive or negative synchronous signal to synchronize the TV set. Connection of load resistor to pin 1 (1.2 kΩ) against V_S = negative synchronous signal. Connection of load resistor to pin 1 against ground = positive synchronous signal.
2	VIL	Level selection	**CVBS Input Level Selection:** with LOW the gain is adjusted to a 1 V level and with an open input to 2.5 V level.
3	RFF	RF-filter	**RF-Level Stabilizer:** capacitor for filter time constant
4	RFA	RF-amplitude	**RF-Level Stabilizer:** capacitor for internal amplitude-dependent control voltage
5	CLIP	Clipping level	Input capacitor for **Clipping Level** of adapted **Data Separation**
6	ZERO	Zero level	Input capacitor for **Zero Level** of adapted **Data Separation**
7	EXDA	External teletext data	Data input for **External Teletext Data** (already separated)
8	TIM	Time characteristics	Capacitor for **Time Characteristics** of adapted **Data Separation**
9	CPD	Clock phase detector	**Clock Phase Detector:** connection for input capacitor
10	$\overline{\text{VCR}}$	Video tape recorder mode	**Video Tape Recorder Mode:** switch-over to short horizontal hold-time constant
11	XTAL	Crystal	**13.875-MHz Crystal Connection:** frequency for double teletext data rate
12	FIL	Filter connection	**Filter Connection** for 6.9375-MHz data clock
13	GND	Ground	**Ground** (0 V)
14	TTC	TTC-output	**TTC Output**
15	TTD	TTD-output	**TTD Output**
16	V_S	V_S	**Supply Voltage** +
17	F6	F6-output	**F6 Output:** 6-MHz clock (signal with negligible harmonic wave)
18	VCO	VCO-output	**6-MHz VCO Output** for frequency-determining resonant circuit
19	PLL1	PLL-low-pass-filter	**PLL-Low-Pass-Filter** with small time-constant by async. operation (filter 2)

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Function	Description
20	VCOI	VCO-input	**6-MHz VCO input** for frequency-determining resonat circuit
21	PLL2	PLL-low-pass-filter	**PLL-Low-Pass-Filter** with bigger time-constant for standard operation
22	SAND	Sandcastle pulse	**Sandcastle Pulse**
23	RMONO	R-Monoflop	**Chronology Resistor** of the monoflops
24	CMONO	C-Monoflop	**Chronology Capacitor** of the monoflops
25	VCS	VCS-output	**VCS-Output:** synchronous signal separated from comp. video
26	BLACK	Black level input capacitor	**Black Level Input Capacitor** for the adapted synchronous pulse separator
27	CVBS	CVBS-input	**CVBS Input Signal** via coupling capacitor with 1 V signal level when pin 2 is connected to ground
28	$\overline{\text{TCS}}$/ $\overline{\text{SCS}}$	$\overline{\text{TCS}}$-, ($\overline{\text{SCS}}$)-input	**Synchronous Signal-Input** $\overline{\text{TCS}}$ during text playback (or $\overline{\text{SCS}}$, when pin 1 is open)

Absolute Maximum Ratings
T_A = 25 °C (all voltages are referred to V_{SS})

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_{16/13}$		13.2	V
Storage temperature range	T_{stg}	– 40	125	°C
Output current VCS	$-I_{25H}$		5	mA
Output current TTD	$-I_{15H}$		10	mA
Output current TTC	$-I_{14H}$		10	mA
Output current F6	$-I_{17H}$		10	mA
Output current sync.	I_1		5	mA
Thermal resistance system-air	R_{thSA}		50	K/W

Operating Range

Supply voltage	$V_{16/13}$	10.8	13.2	V
Ambient temperature in operation	T_A	0	70	°C

Characteristics
$T_A = 25°C$; $V_S = 12\ V \pm 10\%$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Supply current	I_S	53	70	100	mA
CVBS Input, pin 27					
Input signal level Pin 2 to ground Pin 2 open	 V_{27} V_{27}	 0.7 1.75	 1 2.5	 1.4 3.5	 V V
Synchronous signal amplitude	$V_{27\,Sync}$	0.1		1	V
Teletext data level Pin 2 to ground Pin 2 open	 $V_{27\,VTD}$ $V_{27\,VTD}$	 0.3 0.75	 0.46 1.15	 0.7 1.75	 V V
Generator resistor	R_{G27}			250	Ω
Adaptation to CVBS Level					
Input voltage V_{27} = 1 V when V_{27} = 2.5 V when	 $V_{2/13\,L}$ $V_{2/13\,H}$	 0 2.0		 0.8 5.5	 V V
Input current	$-I_{2L}$ I_{2H}	0 0		150 1.3	µA mA
Teletext Data					
Output signal TTD	υ_{15}	2.5	3.5	4.5	V
Transition times	t_r, t_f	20	30	45	ns
Max. permissible capacitative load	$C_{15/13}$			40	pF
Data clock signal TTC	υ_{14}	2.5	3.5	4.5	V
Transition times	t_r, t_f	20	30	45	ns
Max. permissible capacitative load	$C_{14/13}$			40	pF
Time deviation with respect to TTD	t_d	– 20	0	20	ns
DC voltage at outputs	$V_{14,\,15/13}$		4		V

Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Synchronous Pulse Separation VCS (Signal at teletext decoder)					
Output voltage	V_{25L} V_{25H}	0 2.4		0.4 5.5	V V
Output current	I_{25L} $-I_{25H}$			0.5 1.5	mA mA
Delay with respect to CVBS sync.	t_d		0.5		µs
Sync Output Driver (Signal at TV set)					
Output voltage TCS operation Comp. video operation	 V_1 V_1		0.45	 1	 V V
Positive synchronous signal DC voltage load resistor to ground		1.4			V
Output current	$-I_1$			3	mA
Negative synchronous signal DC voltage load resistor to V_S	$V_{1/13}$		10.1		V
Output current	I_1			3	mA
6-MHz Clock F6					
F6-output signal (negligible harmonic content)	V_{17}	1	2	3	V
Transition times	t_r, t_f	20		40	ns
Max. permissible capacitative load	$C_{17/13}$			40	pF
DC voltage at output	$V_{17/13}$	4		8.5	V
Synchronisation Selection SVS					
Input current during TCS operation V_{28} = 0 ... 6.1 V CVBS[1] CVBS V_{28} = 10 ... V_S	 $-I_{28}$ $-I_{28}$ I_{28}	 40 – 5	70	 100 15 5	 µA µA µA
TCS Operation					
Input voltage Load resistor at pin 1 Load resistor at pin 1	 V_{28L} V_{28H}	 0 2		 0.8 6.1	 V V

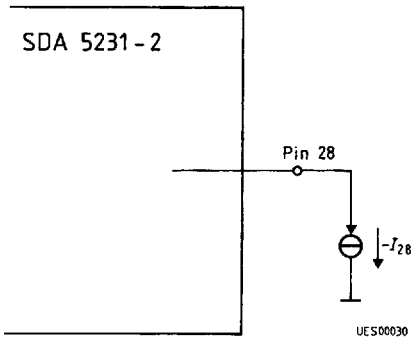
Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
SCS Operation					
Input voltage Pin 1 open Pin 1 open	 V_{28L} V_{28H}	 0 3.5		 1.5 6.1	 V V
Line synchronous pulse width TCS operation SCS operation	 t_p t_p		 2 3		 µs µs
VCR Operation					
Input voltage during VCR operation Standard operation	 $V_{10/13L}$ $V_{10/13H}$	 0 2		 0.8 V_S	 V V
Input current	I_{10}	– 10	0	10	µA
Sandcastle Pulse Input					
Phase locked mode Input voltage PL Input voltage PL	 $V_{22/13L}$ $V_{22/13H}$	 0 3.9		 3 5.5	 V V
PL-low-time for free-wheeling oscillator	t_{PL}	100			ms
Reset pulse for data separation Input voltage CBB Input voltage CBB	 $V_{22/13L}$ $V_{22/13H}$	 0 1		 0.5 5.5	 V V
Input current	I_{22}	– 10		10	µA
Input for External Data (current source driving)					
Internal data processing Input current[2] Voltage I_7 = – 10 to + 100 µA	 I_7 V_7	– 10	0	100	µA
External data processing Input current for low [2] for high [2] Voltage I_7 = – 25 to – 1000 µA	 I_{7L} I_{7H} V_7	 – 175 – 1000 7	 – 40 – 500 8	 – 25 – 325	 µA µA V

[1] **Remarks:** Test circuit 1
[2] Test circuit 2

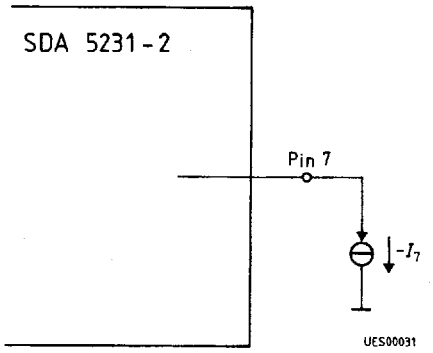
Test Circuits

Test Circuit 1



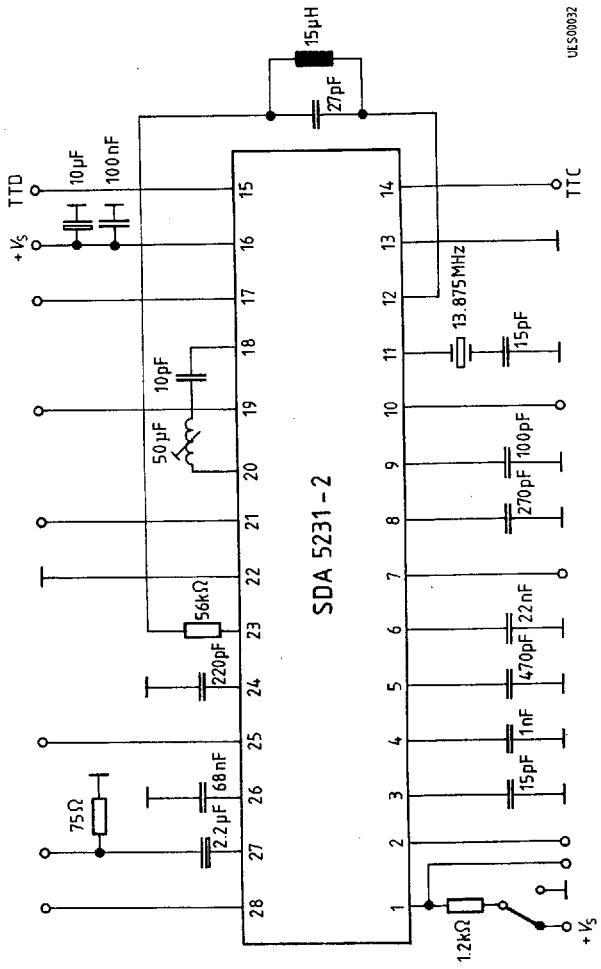
During CVBS operation the output current of pin 28 shall not exceed 15 µA (the pin 12 of the decoder SDA 5242-3 is high-impedance connected)

Test Circuit 2

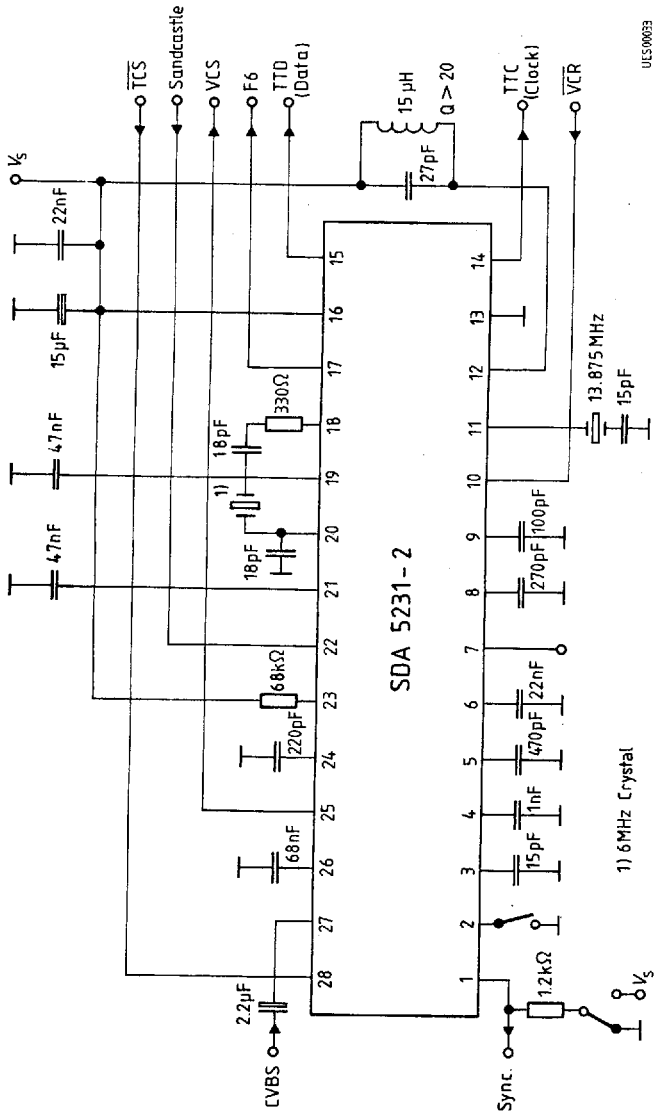


The output current of pin 7 cannot be higher than 10 µA if the processing of the teletext data (wich is in CVBS) must occur.

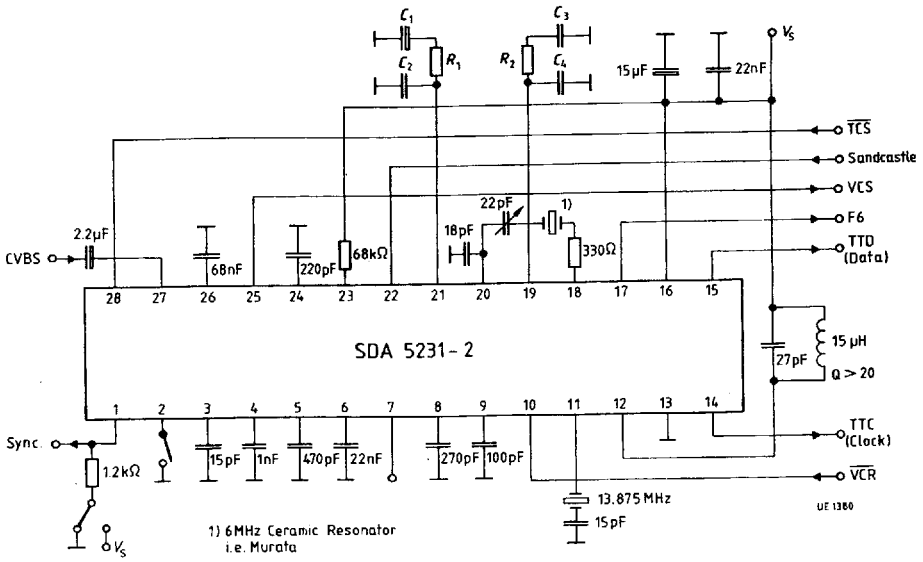
Test Circuit 3



Application Circuit Crystal

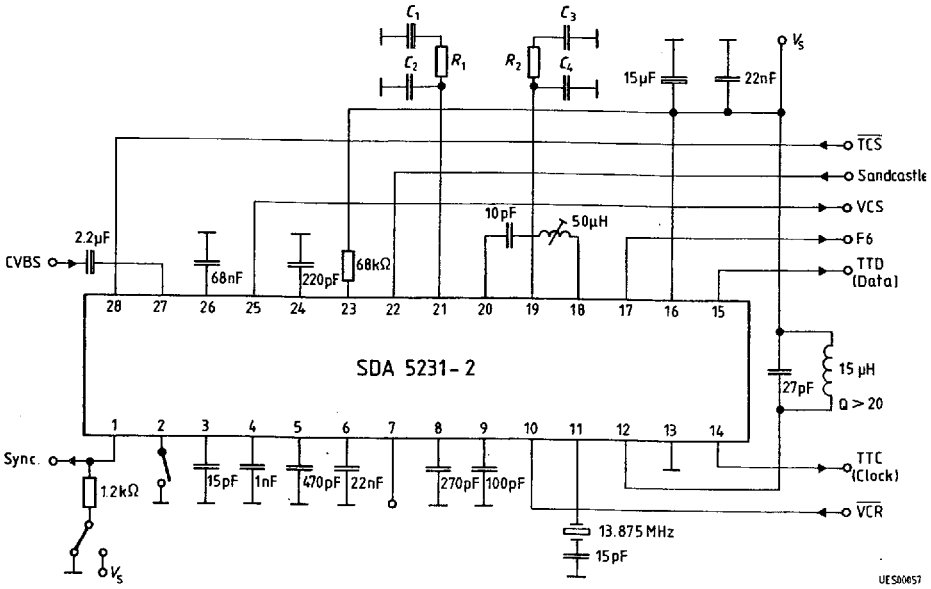


Application Circuit Ceramic Resonator



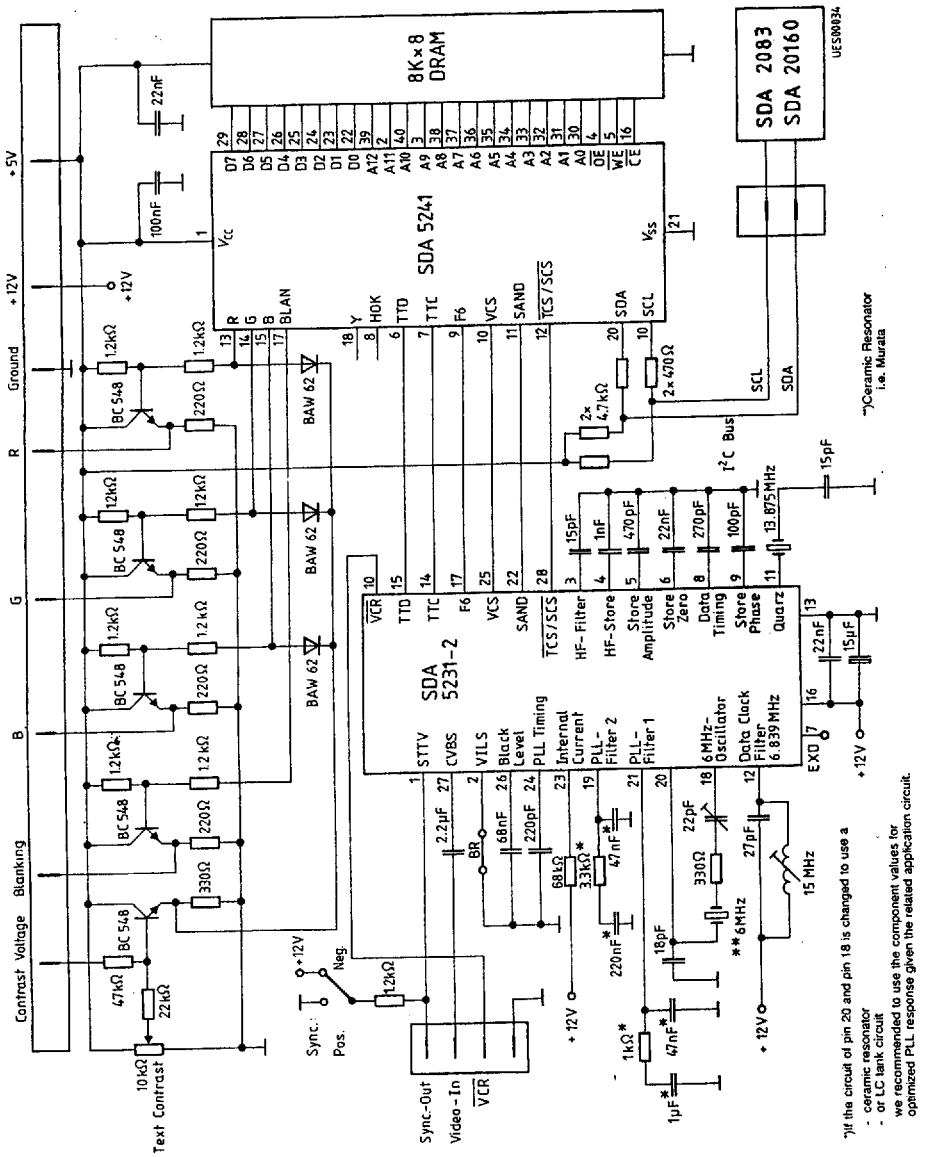
Loop Filter Components	Standard Application	Optimized PLL Behaviour
C_1	1 µF	10 µF
C_2	47 nF	1 µF
C_3	220 nF	330 nF
C_4	47 nF	33 nF
R_1	1 kΩ	500 Ω
R_2	3.3 kΩ	3.3 kΩ

Application Circuit LC-Tank-Circuit

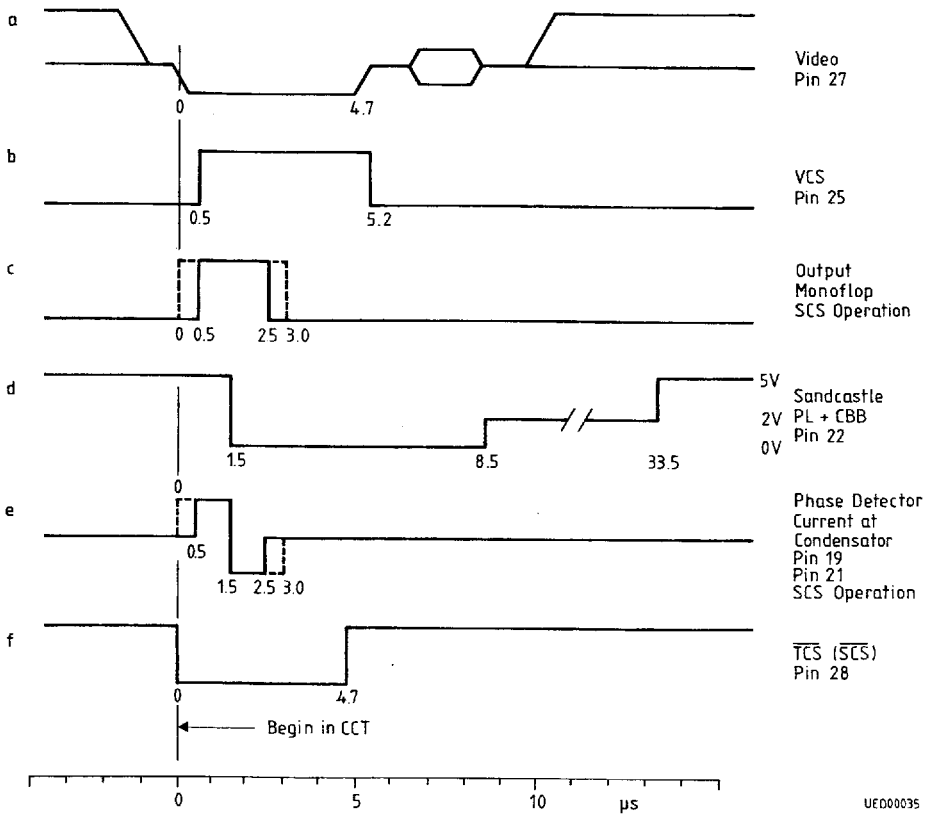


Loop Filter Components	Standard Application	Optimized PLL Behaviour
C_1	47 µF	47 µF
C_2	47 nF	4.7 µF
C_3	47 nF	2.2 µF
C_4	47 nF	220 nF
R_1	82 Ω	82 Ω
R_2	3,3 kΩ	390 Ω

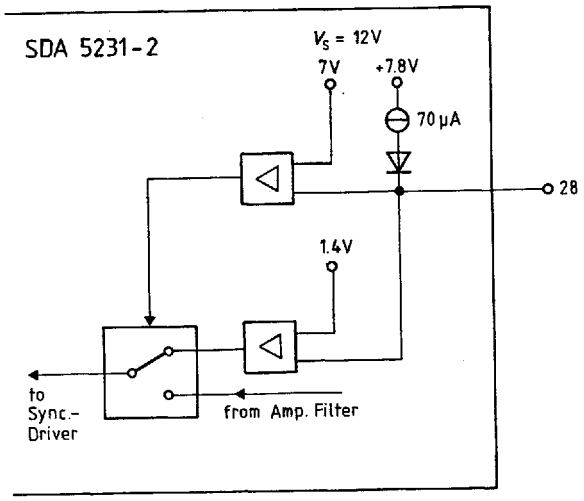
Application Circuit with SDA 5241



Pulse Diagrams

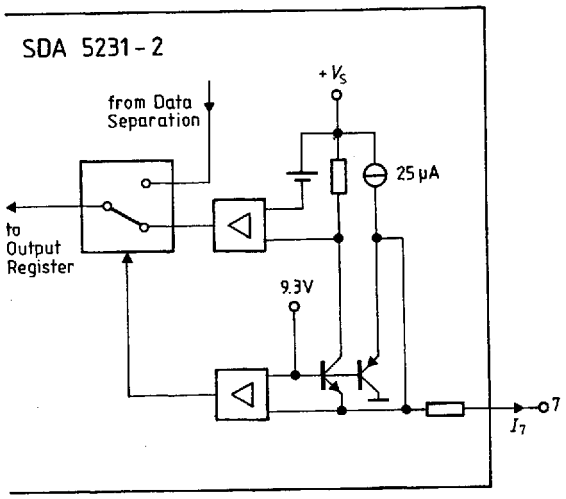


Pin 28



TCS Operation: $V_{28} < 6.1V$ UES00037

PIN 7



External Data Processing: $I_7 > 25\ \mu A$ UES00038