FAIRCHILD SEMICONDUCTOR®

July 1997
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74VHCT74A
Dual D-Type Flip-Flop with Preset and Clear

General Description

The VHCT74A is an advanced high speed CMOS Dual D-Type Flip-Flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The signal level applied to the D INPUT is transferred to the Q OUTPUT during the positive going transition of the CK pulse. CLR and PR are independent of the CK and are accomplished by setting the appropriate input LOW.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with V_{CC} = 0V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

Features

- High speed: f_{MAX} = 160 MHz (typ) at T_A = 25°C
- High noise immunity: V_{IH} = 2.0V, V_{IL} = 0.8V
- Power down protection is provided on all inputs and outputs
- Low power dissipation:
  I_{CC} = 2 μA (max) at T_A = 25°C
- Pin and function compatible with 74HCT74

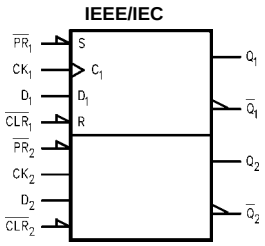
Ordering Code:

Order Number	Package Number	Package Description
74VHCT74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHCT74AMX_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHCT74ASJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT74AMTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

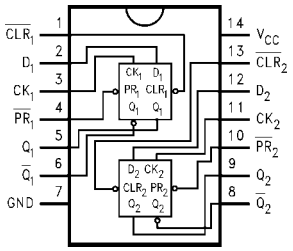
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
D_1, D_2	Data Inputs
CK_1, CK_2	Clock Pulse Inputs
$\overline{CLR}_1$, $\overline{CLR}_2$	Direct Clear Inputs
$\overline{PR}_1$, $\overline{PR}_2$	Direct Preset Inputs
Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$	Outputs

Truth Table

Inputs				Outputs		Function
$\overline{CLR}$	$\overline{PR}$	D	CK	Q	$\overline{Q}$	
L	H	X	X	L	H	Clear
H	L	X	X	H	L	Preset
L	L	X	X	H	H	
H	H	L	↑	L	H	
H	H	H	↑	H	L	
H	H	X	↓	Q_n	Q_n	No Change

Absolute Maximum Ratings (Note 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	
(Note 3)	−0.5V to V_{CC} + 0.5V
(Note 4)	−0.5V to 7.0V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	
(Note 5)	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC}/GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L)	
Soldering (10 seconds)	260°C

Recommended Operating Conditions (Note 6)

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	
(Note 3)	0V to V_{CC}
(Note 4)	0V to 5.5V
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
V_{CC} = 5.0V ± 0.5V	0 ns/V ~ 20 ns/V

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading varaibles. Fairchild does not recommend operation outside databook specifications.

Note 3: HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

Note 4: V_{CC} = 0V.

Note 5: V_{OUT} < GND, V_{OUT} > V_{CC}.(Outputs Active)

Note 6: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = 25°C			T_A = −40°C to +85°C		Units	Conditions	
			Min	Typ	Max	Min	Max			
V_{IH}	HIGH Level Input Voltage	4.5	2.0			2.0		V		
		5.5	2.0			2.0				
V_{IL}	LOW Level Input Voltage	4.5			0.8		0.8	V		
		5.5			0.8		0.8			
V_{OH}	HIGH Level Output Voltage	4.5	4.40	4.50		4.40		V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA
		4.5	3.94			3.80				I_{OH} = −8 mA
V_{OL}	LOW Level Output Voltage	4.5		0.0	0.1		0.1	V	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA
		4.5			0.36		0.44			I_{OL} = 8 mA
I_{IN}	Input Leakage Current	0–5.5			±0.1		±1.0	μA	V_{IN} = 5.5V or GND	
I_{CC}	Quiescent Supply Current	5.5			2.0		20.0	μA	V_{IN} = V_{CC} or GND	
I_{CCT}	Maximum I_{CC}/Input	5.5			1.35		1.50	mA	V_{IN} = 3.4V Other Inputs = V_{CC} or GND	
I_{OFF}	Output Leakage Current (Power Down State)	0.0			+0.5		+5.0	μA	V_{OUT} = 5.5V	

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 7)	$T_A = 25°C$			$T_A = -40°C$ to $+85°C$		Units	Conditions
			Min	Typ	Max	Min	Max		
f_{MAX}	Maximum Clock Frequency	5.0	100	160		80		MHz	$C_L = 15$ pF
		5.0	80	140		65			$C_L = 50$ pF
t_{PLH} t_{PHL}	Propagation Delay Time (CK-Q, $\overline{Q}$)	5.0		5.8	7.8	1.0	9.0	ns	$C_L = 15$ pF
		5.0		6.3	8.8	1.0	10.0		$C_L = 50$ pF
t_{PLH} t_{PHL}	Propagation Delay time ($\overline{CLR}$, $\overline{PR}$ -Q, $\overline{Q}$)	5.0		7.6	10.4	1.0	12.0	ns	$C_L = 15$ pF
		5.0		8.1	11.4	1.0	13.0		$C_L = 50$ pF
C_{IN}	Input Capacitance			4	10		10	pF	V_{CC} = Open
C_{PD}	Power Dissipation Capacitance			24				pF	(Note 8)

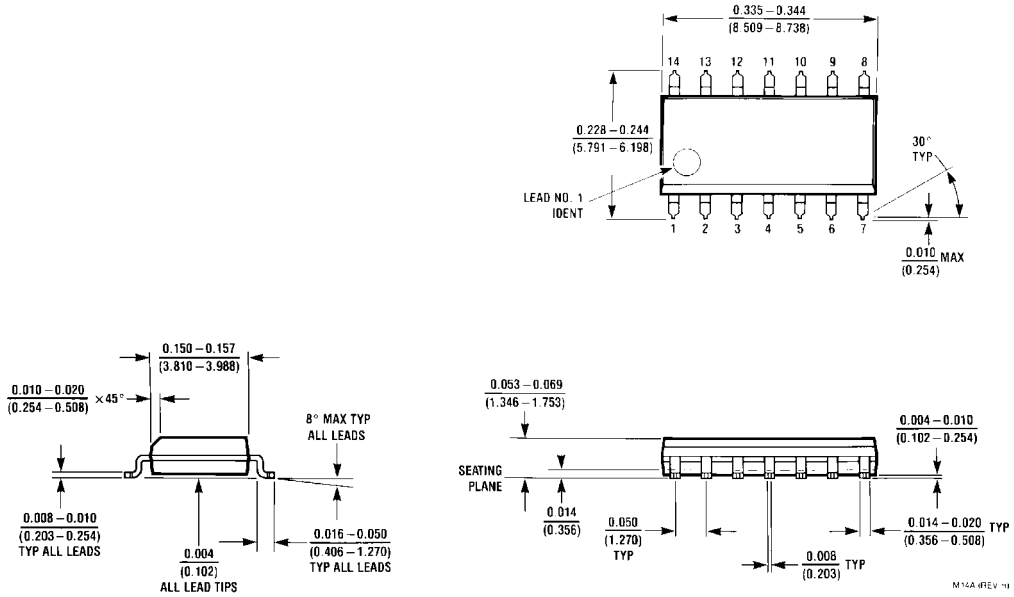
Note 7: V_{CC} is 5.0 ± 0.5V

Note 8: C_{PD} is defined as the value of internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr) = $C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per flip-flop).

AC Operating Requirements

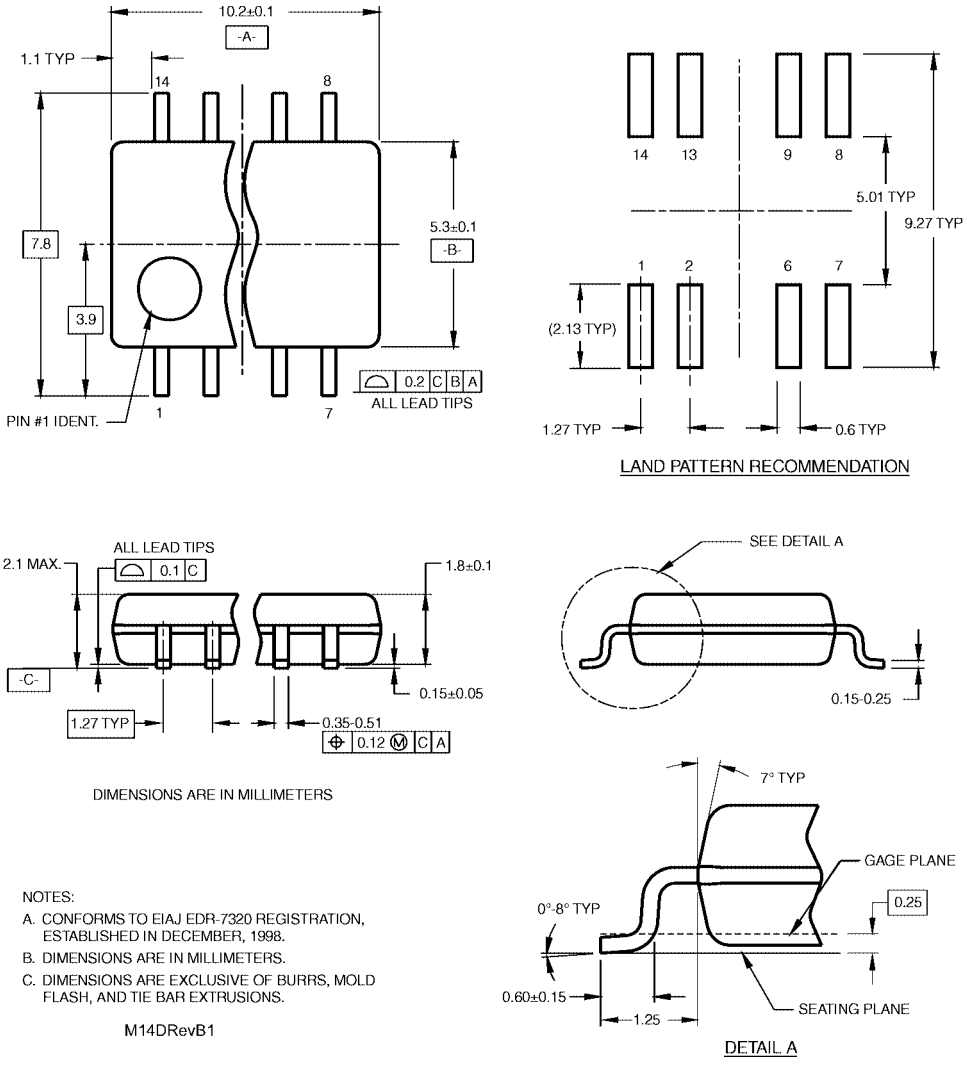
Symbol	Parameter	V_{CC} (V)	$T_A = 25°C$	$T_A = -40°C$ to $+85°C$	Units
			Typ	Guaranteed Minimum	
$t_W(L)$ $t_W(H)$	Minimum Pulse Width (CK)	5.0 ± 0.5		5.0	5.0	ns
$t_W(L)$	Minimum Pulse Width ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		5.0	5.0	ns
t_S	Minimum Setup Time	5.0 ± 0.5		5.0	5.0	ns
t_H	Minimum Hold Time	5.0 ± 0.5		0	0	ns
t_{REM}	Minimum Removal Time ($\overline{CLR}$, $\overline{PR}$)	5.0 ± 0.5		3.5	3.5	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.

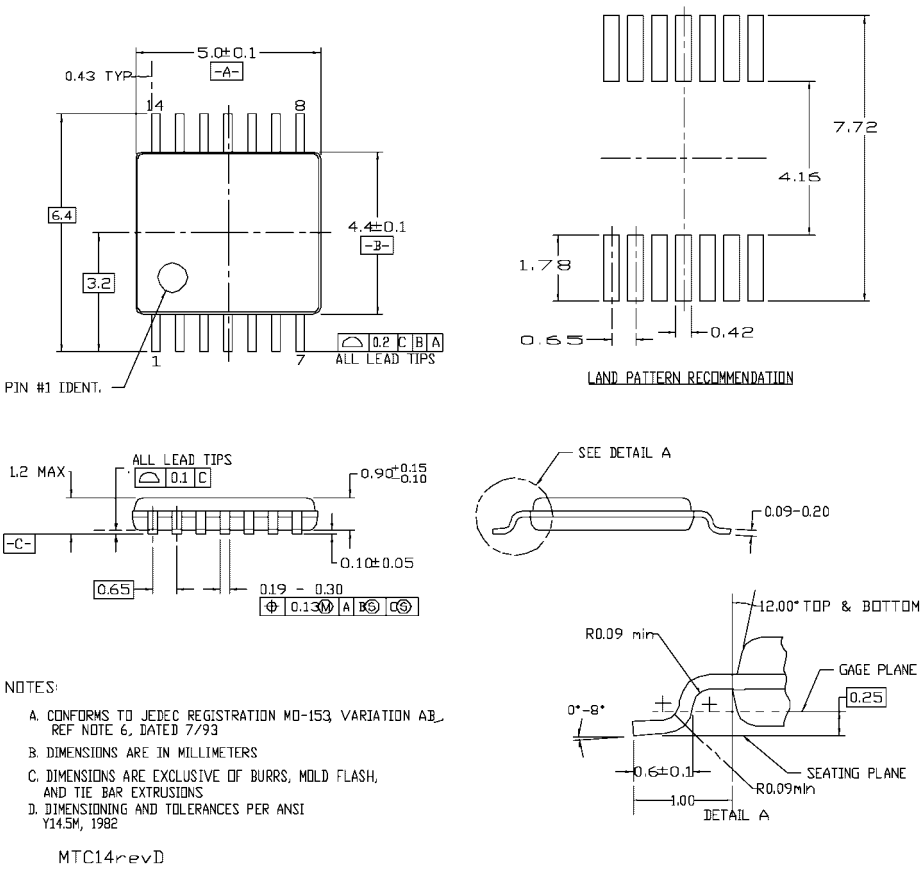
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATED 7/93

B. DIMENSIONS ARE IN MILLIMETERS

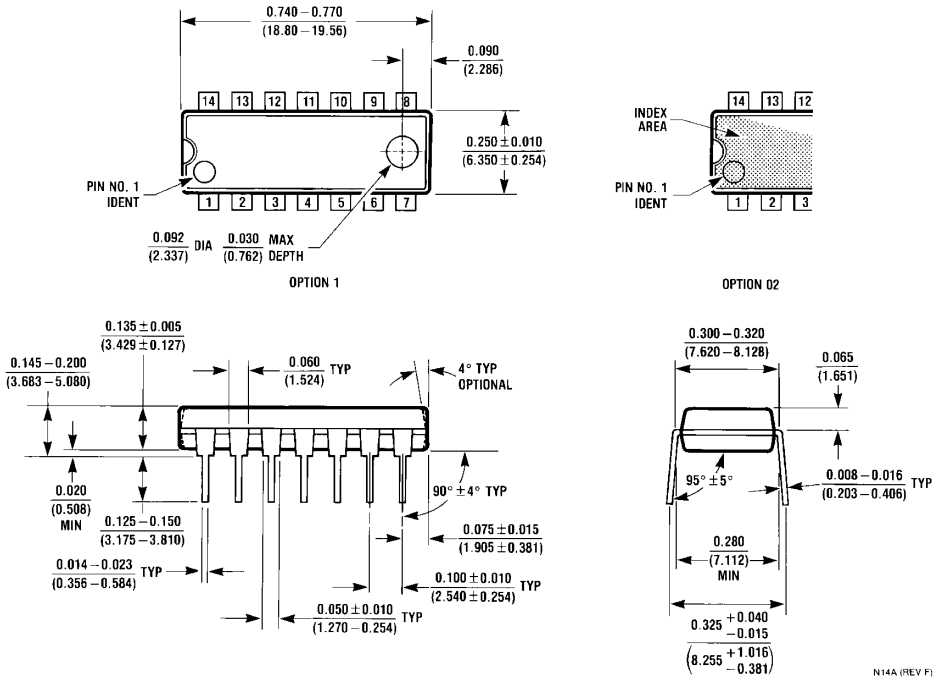
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS

D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982

MTC14revD

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A