

IRFF130, IRFF131, IRFF132, IRFF133

File Number 1564

Power MOS Field-Effect Transistors

N-Channel Enhancement-Mode
Power Field-Effect Transistors

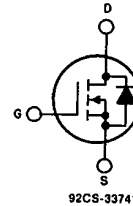
7.0A and 8.0A, 60V-100V

 $r_{DS(on)} = 0.18 \Omega$ and 0.25Ω

Features:

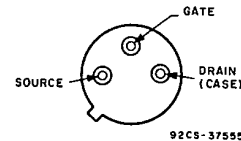
- SOA is power-dissipation limited
- Nanosecond switching speeds
- Linear transfer characteristics
- High input impedance
- Majority carrier device

N-CHANNEL ENHANCEMENT MODE



TERMINAL DIAGRAM

TERMINAL DESIGNATION



JEDEC TO-205AF

The IRFF130, IRFF131, IRFF132 and IRFF133 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFF-types are supplied in the JEDEC TO-205AF (LOW-PROFILE TO-39) metal package.

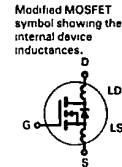
Absolute Maximum Ratings

Parameter	IRFF130	IRFF131	IRFF132	IRFF133	Units
V_{DS} Drain - Source Voltage (1)	100	60	100	60	V
V_{DGR} Drain - Gate Voltage ($R_{GS} = 20 \text{ k}\Omega$) (1)	100	60	100	60	V
$I_D @ T_C = 25^\circ\text{C}$ Continuous Drain Current	8.0	8.0	7.0	7.0	A
I_{DM} Pulsed Drain Current (2)	32	32	28	28	A
V_{GS} Gate - Source Voltage	± 20				V
$P_D @ T_C = 25^\circ\text{C}$ Max. Power Dissipation	25 (See Fig 14)				W
Linear Derating Factor	0.2 (See Fig 14)				W/ $^\circ\text{C}$
I_{LM} Inductive Current, Clamped	(See Fig 15 and 16) $L = 100 \mu\text{H}$				A
T_J Operating Junction and Storage Temperature Range	-55 to 150				$^\circ\text{C}$
Lead Temperature	300 (0.063 in. (1.6mm) from case for 10s)				$^\circ\text{C}$

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Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	IRFF130 IRFF132	100	—	—	V	$V_{GS} = 0V$
	IRFF131 IRFF133	60	—	—	V	$I_D = 250\mu A$
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{GSS} Gate-Source Leakage Forward	ALL	—	—	100	nA	$V_{GS} = 20V$
I_{GSS} Gate-Source Leakage Reverse	ALL	—	—	-100	nA	$V_{GS} = -20V$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	—	250	μA	$V_{DS} = \text{Max. Rating}, V_{GS} = 0V$
		—	—	1000	μA	$V_{DS} = \text{Max. Rating} \times 0.8, V_{GS} = 0V, T_C = 125^\circ\text{C}$
$I_{D(on)}$ On-State Drain Current ②	IRFF130 IRFF131	8.0	—	—	A	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, V_{GS} = 10V$
	IRFF132 IRFF133	7.0	—	—	A	
$R_{DS(on)}$ Static Drain-Source On State Resistance ②	IRFF130 IRFF131	—	0.14	0.18	Ω	$V_{GS} = 10V, I_D = 4.0A$
	IRFF132 IRFF133	—	0.20	0.25	Ω	
g_{fs} Forward Transconductance ②	ALL	4.0	5.5	—	S (③)	$V_{DS} > I_{D(on)} \times R_{DS(on)} \text{ max.}, I_D = 4.0A$
C_{iss} Input Capacitance	ALL	—	600	800	pF	$V_{GS} = 0V, V_{DS} = 25V, f = 1.0 \text{ MHz}$
C_{oss} Output Capacitance	ALL	—	300	500	pF	See Fig. 10
C_{rss} Reverse Transfer Capacitance	ALL	—	100	150	pF	
$t_{d(on)}$ Turn On Delay Time	ALL	—	30	50	ns	$V_{DD} = 0.5 BV_{DSS}, I_D = 4.0A, Z_\theta = 50^\circ\text{C/W}$
t_r Rise Time	ALL	—	80	150	ns	See Fig. 17
$t_{d(off)}$ Turn Off Delay Time	ALL	—	50	100	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	ALL	—	80	150	ns	
Q_g Total Gate Charge (Gate Source Plus Gate-Drain)	ALL	—	18	30	nC	$V_{GS} = 10V, I_D = 18A, V_{DS} = 0.8 \text{ Max. Rating}$. See Fig. 18 for test circuit. (Gate charge is essentially independent of operating temperature.)
Q_{gs} Gate-Source Charge	ALL	—	9.0	—	nC	
Q_{gd} Gate-Drain ("Miller") Charge	ALL	—	9.0	—	nC	
L_D Internal Drain Inductance	ALL	—	5.0	—	nH	Measured from the drain lead, 5mm (0.2 in.) from header to center of die.
L_S Internal Source Inductance	ALL	—	15	—	nH	Measured from the source lead, 5mm (0.2 in.) from header to source bonding pad.



Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	5.0	$^\circ\text{C/W}$	
R_{thJA} Junction-to-Ambient	ALL	—	—	175	$^\circ\text{C/W}$	Free Air Operation

Source-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	IRFF130 IRFF131	—	—	8.0	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
	IRFF132 IRFF133	—	—	7.0	A	
I_{SM} Pulse Source Current (Body Diode) ③	IRFF130 IRFF131	—	—	32	A	
	IRFF132 IRFF133	—	—	28	A	
V_{SD} Diode Forward Voltage ②	IRFF130 IRFF131	—	—	2.5	V	$T_C = 25^\circ\text{C}, I_S = 8.0A, V_{GS} = 0V$
	IRFF132 IRFF133	—	—	2.3	V	$T_C = 25^\circ\text{C}, I_S = 7.0A, V_{GS} = 0V$
t_{rr} Reverse Recovery Time	ALL	—	300	—	ns	$T_J = 150^\circ\text{C}, I_F = 8.0A, dI_F/dt = 100A/\mu s$
Q_{RR} Reverse Recovered Charge	ALL	—	1.5	—	μC	$T_J = 150^\circ\text{C}, I_F = 8.0A, dI_F/dt = 100A/\mu s$
t_{on} Forward Turn on Time	ALL	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

① $T_J = 25^\circ\text{C}$ to 150°C .② Pulse Test: Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

③ Repetitive Rating: Pulse width limited by max. junction temperature.

See Transient Thermal Impedance Curve (Fig. 5).

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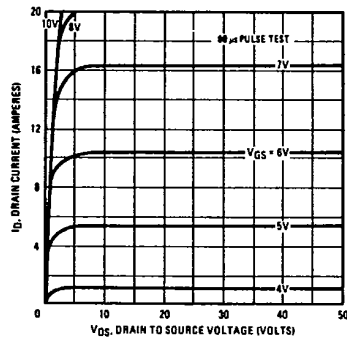


Fig. 1 - Typical Output Characteristics

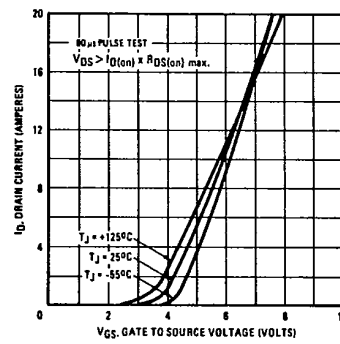


Fig. 2 - Typical Transfer Characteristics

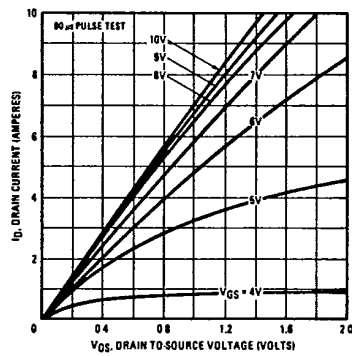


Fig. 3 - Typical Saturation Characteristics

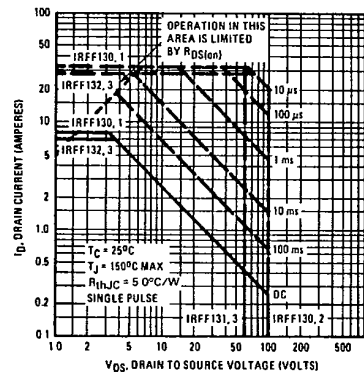


Fig. 4 - Maximum Safe Operating Area

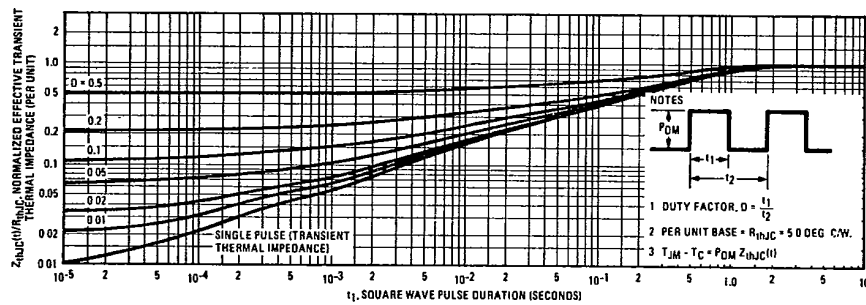


Fig. 5 - Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

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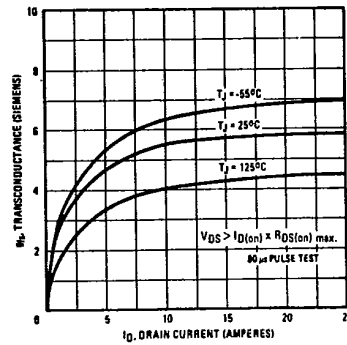


Fig. 6 - Typical Transconductance Vs. Drain Current

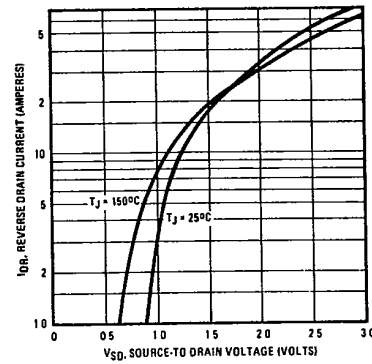


Fig. 7 - Typical Source-Drain Diode Forward Voltage

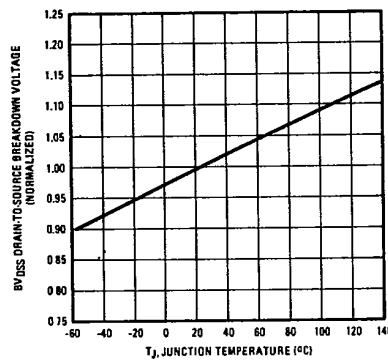


Fig. 8 - Breakdown Voltage Vs. Temperature

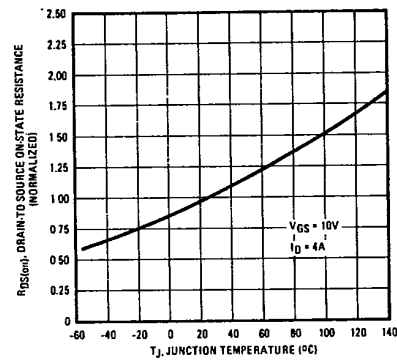


Fig. 9 - Normalized On-Resistance Vs. Temperature

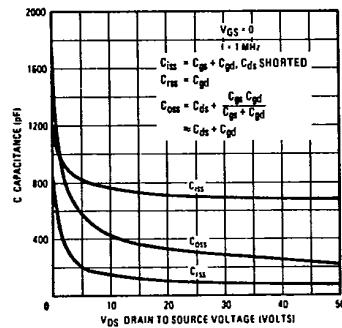


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

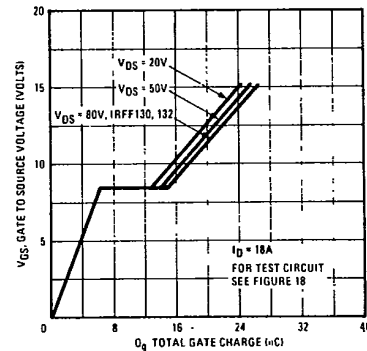


Fig. 11 - Typical Gate Charge Vs. Gate-to-Source Voltage

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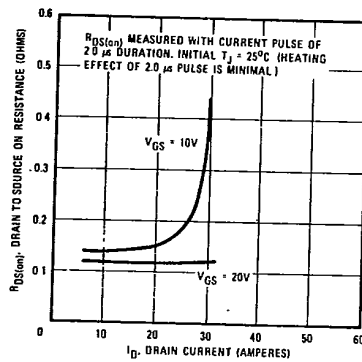


Fig. 12 - Typical On-Resistance Vs. Drain Current

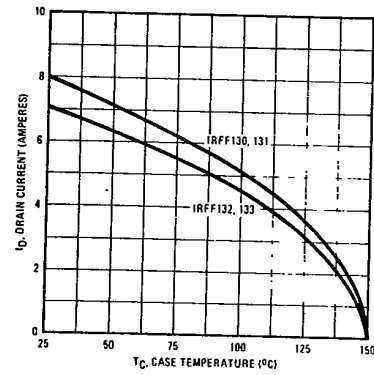


Fig. 13 - Maximum Drain Current Vs. Case Temperature

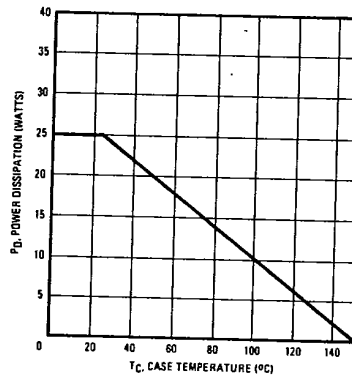


Fig. 14 - Power Vs. Temperature Derating Curve

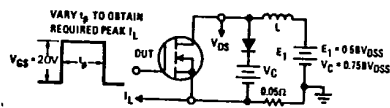


Fig. 15 - Clamped Inductive Test Circuit

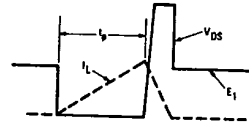


Fig. 16 - Clamped Inductive Waveforms

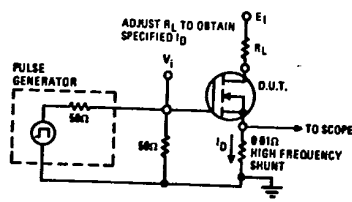


Fig. 17 - Switching Time Test Circuit

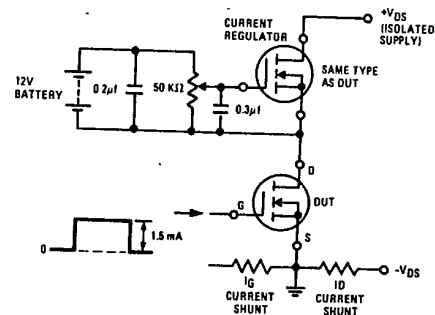


Fig. 18 - Gate Charge Test Circuit