MAXIM

Programmable Gain Amplifier

General Description

The PGA100 is a precision, digitally-programmable gain amplifier (PGA) combined with an 8 channel ±35V protected input multiplexer. The user can select any one of eight analog input channels to be amplified by one of the eight noninverting binarily weighted gain steps from 1 to 128. The digital gain and channel select are internally latched for easy microprocessor interface. The fast 5μsec settling time allows the PGA100 to be used in rapid channel scanning data acquisition systems.

Applications

Data Acquisition Amplifier

Software Error Correction

Digitally-Controlled Autoranging

Test Equipment

Remote Instrumentation System

System Dynamic Range and Resolution Improvement

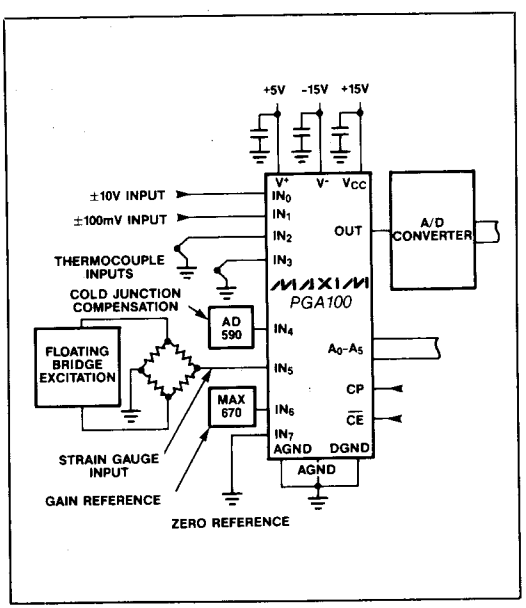
Features

- **High Gain Accuracy ±0.02% max (B Grade)**
- **Input protection, ±20V above ±15V supplies**
- **High Input Impedance: $10^{11}\Omega$**
- **Fast Settling, 5μsec to 0.01%**
- **Low Channel to Channel Crosstalk, -90dB**
- **Low nonlinearity ±0.005% max (B Grade)**
- **8 analog input channels**
- **8 Selectable Gains, 1, 2, 4, 8, 16, 32, 64, 128 V/V**
- **Fully microprocessor-compatible**

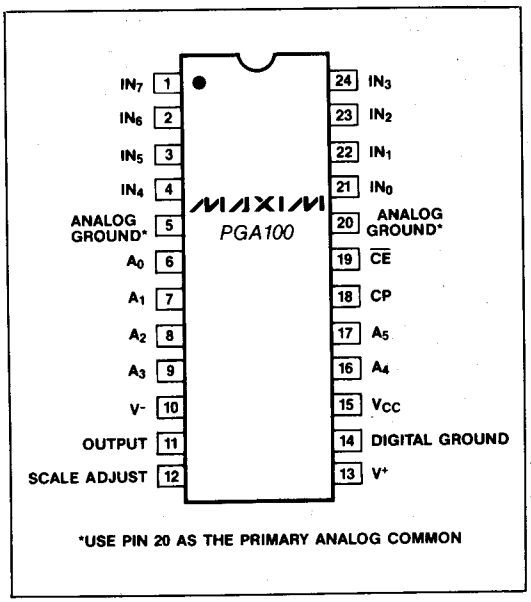
Ordering Information

PART	TEMP. RANGE	PACKAGE
PGA100AG	-25°C to +85°C	24 Pin Ceramic Side Braze
PGA100BG	-25°C to +85°C	24 Pin Ceramic Side Braze

Typical Operating Circuit



Pin Configuration



*USE PIN 20 AS THE PRIMARY ANALOG COMMON

5

Programmable Gain Amplifier

ABSOLUTE MAXIMUM RATINGS

Analog Supply (V^+, V^-) ..... ±18V
Digital Supply (V_{CC}) ..... +7V
Input Voltage Range Analog ..... V^-–20V≤V_{IN}≤V^++20V
Input Voltage Range Digital ..... –0.3≤V_{IN}≤+7V
Storage Temperature Range ..... –65°C to +160°C
Lead Temperature (soldering 10 seconds) ..... 300°C
Output Short-Circuit Duration .... Continuous to Ground
Junction Temperature ..... 175°C
Power Dissipation 1W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute Maximum ratings conditions for extended periods may affect the device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V, V^+ = +15V, V^- = –15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	PGA100AG			PGA100BG			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Gain Accuracy (Note 1) vs Temperature (Note 2) vs Time		G = 1 to 128, I_O = 1mA –25°C ≤ T_A ≤ +85°C		±.01 ±5 ±.001	±.05 ±10		±.005 ±5 ±.001	±.02 ±10	% ppm/°C %/1000 Hrs.
Nonlinearity (Note 3) vs Temperature (Note 2) vs Time		G = 1 to 128, I_O = 1mA –25°C ≤ T_A ≤ +85°C		±.004 ±2 ±.001	±.01 ±5		±.002 ±2 ±.001	±.005 ±5	% of FS ppm/°C %/1000 Hrs.
Rated Output Voltage		I_{OUT} = ±2mA	±10			±10			V
Rated Output Current		V_{OUT} = ±10V	±2			±2			mA
Output Resistance		Gain ≤ 128		0.05			0.05		Ω
Short Circuit Current				±15			±15		mA
Capacitive Load		Phase margin ≥ 25°		1000			1000		pF
Offset Voltage vs Temperature vs Supply vs Time		T_A = 25°C –25°C ≤ T_A ≤ +85°C 8V ≤ |V| ≤ 18V		±0.1 ±6 ±10 ±15	±1 ±80 		±.05 ±6 ±10 ±15	±.5 ±80 	mV µV/°C µV/V µV/month
Input Bias Current "Off" Channel "On" Channel vs Temperature				 ±10 ±0.1 Note 4			 ±10 ±0.1 Note 4	 1 	 pA nA
Input Difference Current, between Channels: "Off" Channel "On" Channel vs Temperature				 ±20 ±0.2 Note 4			 ±20 ±0.2 Note 4	 ±2 	 pA nA
Analog Input Characteristics: Input Voltage Range Input Impedance "Off" Channel "On" Channel		Linear Operation		 ±10 10^{12}||15 10^{11}||25			 ±10 10^{12}||15 10^{11}||25		 V Ω||pF Ω||pF
Input Voltage Noise Density		f_O = 1Hz f_O = 10Hz f_O = 100Hz f_O = 1kHz f_O = 10kHz f_O = 100kHz		200 60 25 18 18 18			200 60 25 18 18 18		nV/√Hz nV/√Hz nV/√Hz nV/√Hz nV/√Hz nV/√Hz

ELECTRICAL CHARACTERISTICS (Continued)

(V_{CC} = 5V, V^+ = +15V, V^- = -15V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	PGA100AG			PGA100BG			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Noise		f_{BW} = 0.1Hz to 10Hz		2.6			2.6		μV_{P-P}
Current Noise Density		f_O = 0.1Hz thru 8kHz		6			6		$fA/\sqrt{Hz}$
Current Noise		f_{BW} = 0.1Hz to 10Hz		115			115		fA_{P-P}
Gain Bandwidth Product				5			5		MHz
Full Power Bandwidth		G=1, V_O=20V_{P-P}, R_L=5kΩ		220		80	220		kHz
Slew Rate		G=1, V_O=±10V, R_L=5kΩ		14		5	14		V/μsec
Settling Time (Note 5) to 1% to 0.1% to 0.01%		G=1, V_O=±10V, R_L=5kΩ		 2.5 3 5			 2.5 3 5		 μsec μsec μsec
Rise Time		10% to 90%, 100mV		70			70		nsec
Phase Margin		G = 1, R_L = 5kΩ		60			60		°
Overload Recovery (Note 6)		G = 1, 50% overdrive		2			2		μsec
Crosstalk, RTI (Note 5, 7)		20V_{P-P}, 1kHz sine, R_S = 1kΩ on all OFF channels		±0.003			±0.003		%
Digital Inputs (Note 8): Input "LOW" Threshold					0.8			0.8	V
Input "HIGH" Threshold			2.0			2.0			V
Clock Pulse Width (low)	t_{WL}		20			20			nsec
Setup Time (CP to data)	t_{S1}		20			20			nsec
Hold Time (CP to data)	t_{H1}		5			5			nsec
Setup Time ($\overline{CE}$ to CP)	t_{S2}		25			25			nsec
Hold Time ($\overline{CE}$ to CP)	t_{H2}		5			5			nsec
V^+/V^- Range		Derated performance	±8		±18	±8		±18	V
V^+ Current				20	27		15	20	mA
V^- Current				10	16		7.5	12	mA
V_{CC} Range		Full performance	4.75		5.25	4.75		5.25	V
V_{CC} Current		V_{CC} = +5.25V		15	27		15	27	mA

Note 1: Inaccuracy is the percent error between the actual and ideal gain selected measured after temperature stabilization. It may be externally adjusted to zero.

Note 2: Parameter is untested and is not guaranteed.

Note 3: Nonlinearity is the maximum peak deviation from a "best straight line" (curve fitting on input-output graph) expressed as a percent of the full scale peak-to-peak output. Gain constant, V_{OUT} ranges from -10V to +10V.

Note 4: Doubles approximately every 10°C.

Note 5: See Typical Performance Curves.

Note 6: Time required for the output to return from saturation to linear operation following the removal of an input overdrive signal.

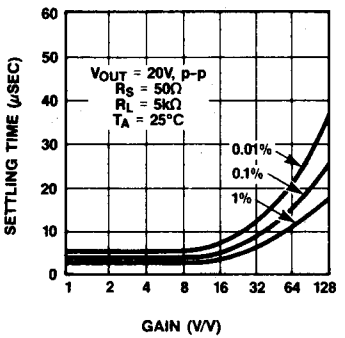
Note 7: Crosstalk is the amount of signal feedthrough from all OFF channels that appears at the output of the input multiplexer. It is express as a percent of the signal applied to all OFF channels.

Note 8: All digital inputs are one 74LSTTL load. Timing specifications not tested; guaranteed by design.

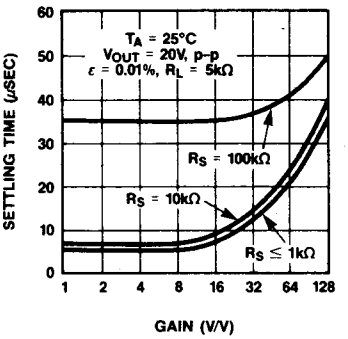
Programmable Gain Amplifier

Typical Performance Curves

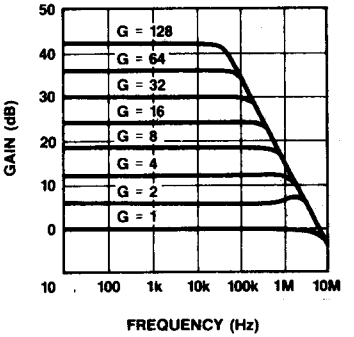
SETTLING TIME vs GAIN



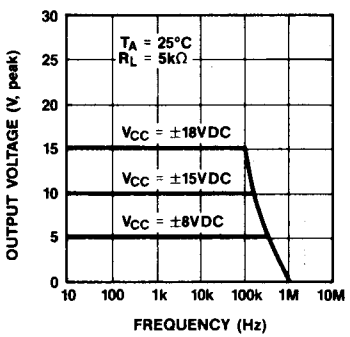
SETTLING TIME vs GAIN AND SOURCE RESISTANCE



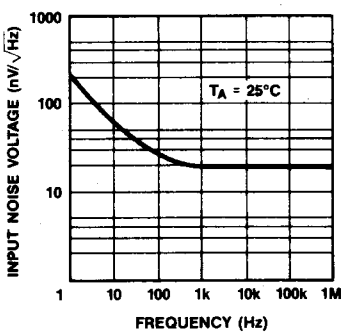
SMALL SIGNAL FREQUENCY RESPONSE



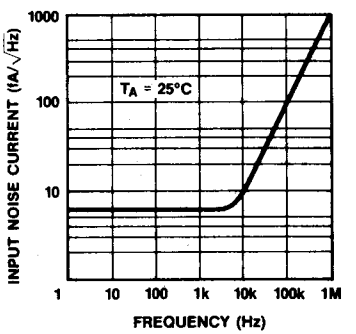
LARGE SIGNAL OUTPUT VOLTAGE vs FREQUENCY



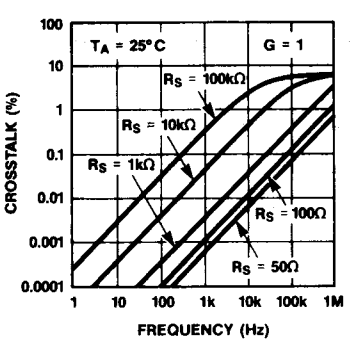
INPUT NOISE VOLTAGE vs FREQUENCY



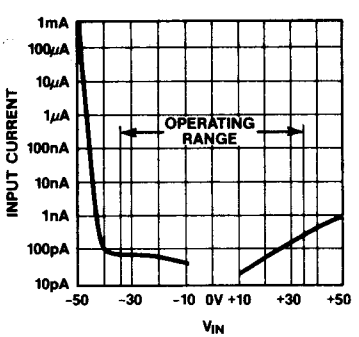
INPUT NOISE CURRENT vs FREQUENCY



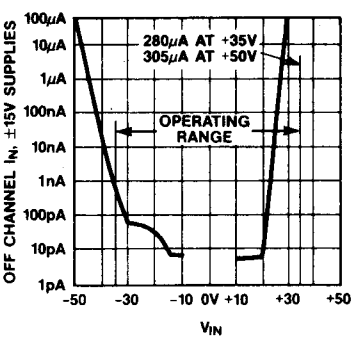
CHANNEL-TO-CHANNEL CROSSTALK vs FREQUENCY



OFF CHANNEL LEAKAGE CURRENT vs INPUT VOLTAGE WITH ±15V SUPPLIES



INPUT LEAKAGE vs INPUT VOLTAGE WITH V⁺ = V⁻ = 0V



Description

The PGA100 consists of an 8 channel ±35V protected input multiplexer followed by a non-inverting operational amplifier whose gain may be set using another multiplexer selecting outputs on a resistive feedback network (see Figure 1). Both multiplexers are fed from a TTL 6 bit latch similar to a 74LS378. The digital inputs are latched by the positive transition of the clock pulse, pin 18, when the clock enable, pin 19, is low. The relative set up and hold times specified in the Electrical Specifications are shown in Figure 3.

Layout Considerations

The PGA100 has dual analog ground pins and a separate digital ground. These must be connected at some single point in the system. The resistance seen by the analog ground is critical and must be kept below 5 milliohms to meet the accuracy specifications. Pin 20 is the primary analog ground, so should be used as the system reference point.

Input Overvoltage Protection

The PGA100 can withstand input overvoltage of up to ±35V, or 20V greater than ±15V analog supply voltages. In normal operation, this allows inputs up to plus and minus 35V. Even with the analog supplies powered down, the inputs may still be stimulated up to plus and minus 20V without damage. This degree of protection is achieved with a Maxim proprietary circuit/process as used in the MAX358 multiplexer. Note that overdriven inputs go to a relatively high impedance state that minimizes input loading and power dissipation.

Optional Gain Scale/Adjust

Ordinarily, no connection is made to pin 12 and this results in the standard gains specified in Table 1. A slight adjustment in the gains other than unity may be made by connecting a resistor or potentiometer between pin 12 and the output and/or ground. This will allow any one gain to be adjusted exactly, but at the expense of the others. The pin 12 connection has no effect on the unity gain accuracy.

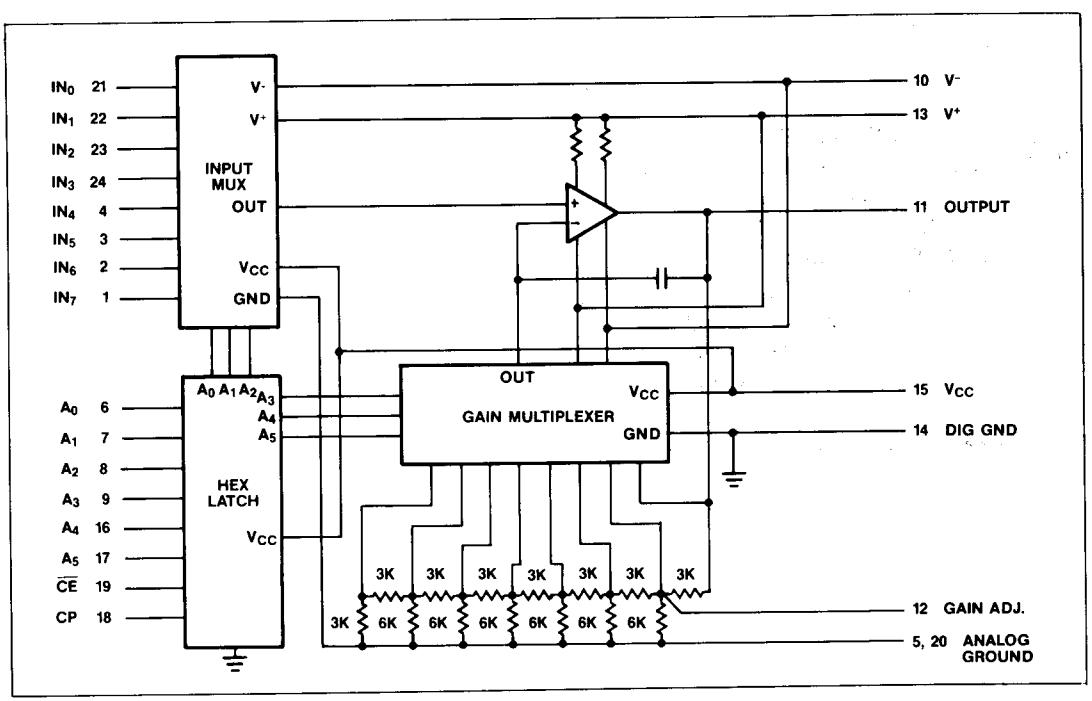


Figure 1. Equivalent Internal Schematic

Programmable Gain Amplifier

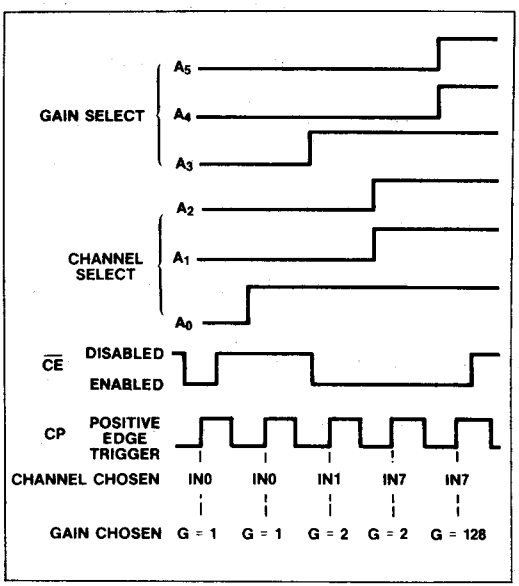


Figure 2. Timing Diagram for Selected Addresses

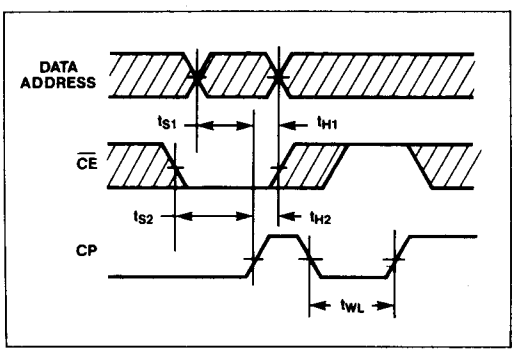


Figure 3. Data Address and Clock Enable Setup and Hold Times

Table 1: Gain and Channel Select Truth Table

Channel A0	A1	A2	Gain A3	A4	A5	
0	0	0				Channel 0
1	0	0				Channel 1
0	1	0				Channel 2
1	1	0				Channel 3
0	0	1				Channel 4
1	0	1				Channel 5
0	1	1				Channel 6
1	1	1				Channel 7
			0	0	0	Gain = 1
			1	0	0	Gain = 2
			0	1	0	Gain = 4
			1	1	0	Gain = 8
			0	0	1	Gain = 16
			1	0	1	Gain = 32
			0	1	1	Gain = 64
			1	1	1	Gain = 128

0 = Low
1 = High

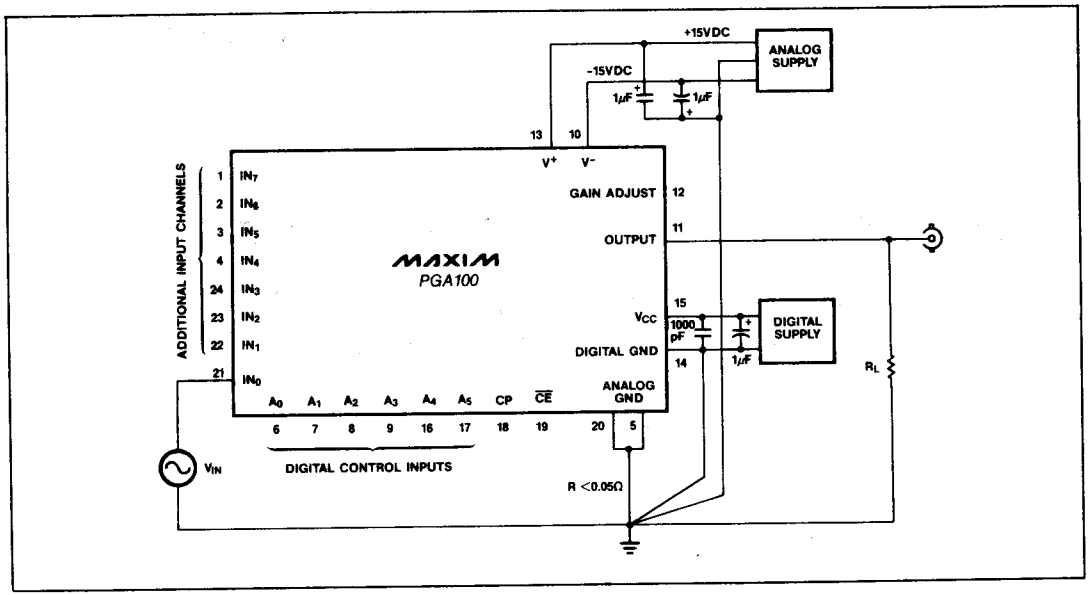


Figure 4. Basic Power Supply, Ground, and Signal Connections.

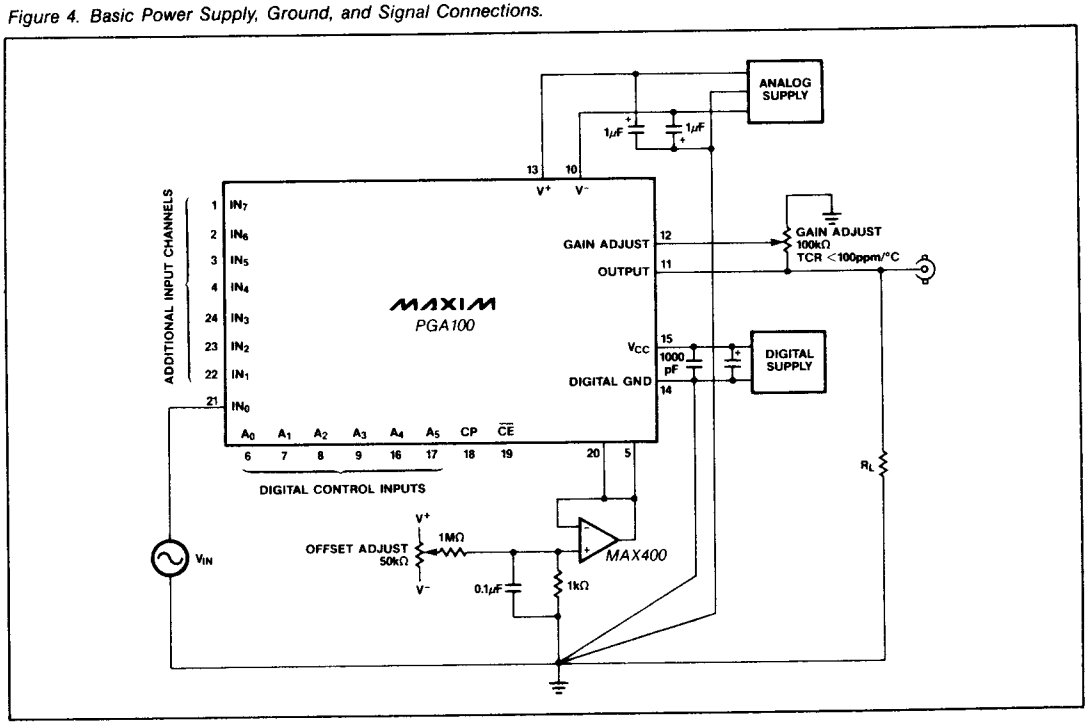


Figure 5. External Gain and Offset Adjustment

Programmable Gain Amplifier

Typical System Application

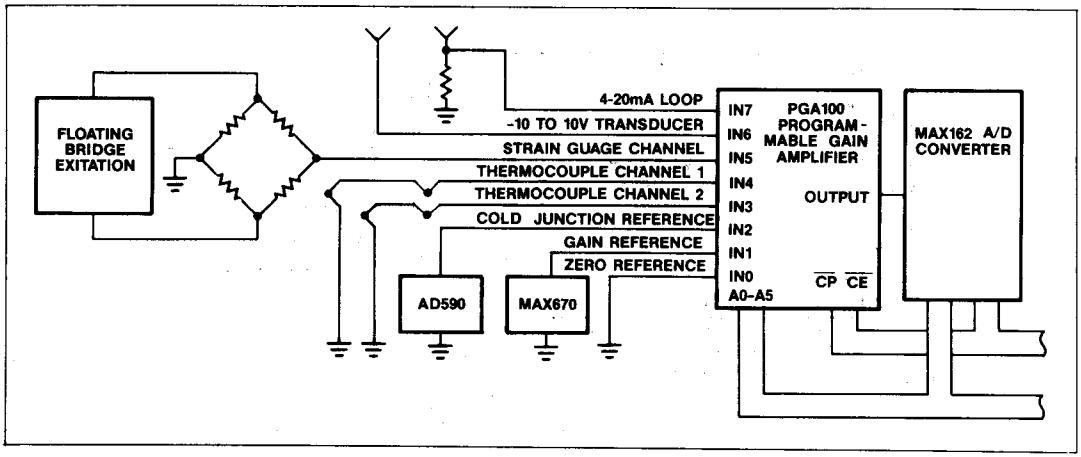


Figure 6. Multiple Channel, Variable Gain Data Acquisition System.