

SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

SDAS224B – JUNE 1982 – REVISED NOVEMBER 1995

- Compare Two 8-Bit Words
- Choice of Totem-Pole or Open-Collector Outputs
- SN74ALS518 and 'ALS520 Have 20-k Ω Pullup Resistors on Q Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

TYPE	INPUT PULLUP RESISTOR	OUTPUT FUNCTION AND CONFIGURATION
SN74ALS518	Yes	P = Q open collector
'ALS520	Yes	$\overline{P = Q}$ totem pole
SN74ALS521 [‡]	No	$\overline{P = Q}$ totem pole

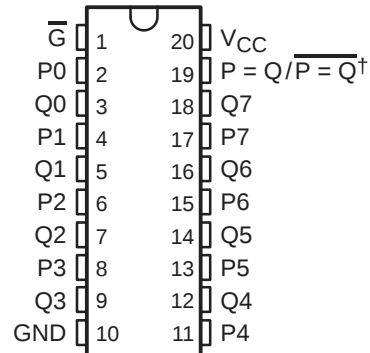
[‡] SN74ALS521 is identical to 'ALS688.

description

These identity comparators perform comparisons on two 8-bit binary or BCD words. The SN74ALS518 provides P = Q outputs, while the 'ALS520 and SN74ALS521 provide $\overline{P = Q}$ outputs. The SN74ALS518 has an open-collector output. The SN74ALS518 and 'ALS520 feature 20-k Ω pullup resistors on the Q inputs for analog or switch data.

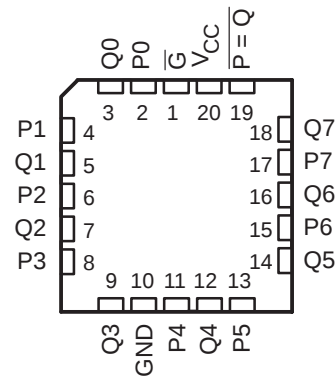
The SN54ALS520 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74ALS518, SN74ALS520, and SN74ALS521 are characterized for operation from 0°C to 70°C.

SN54ALS520 . . . J PACKAGE
SN74ALS518, SN74ALS520,
SN74ALS521 . . . DW OR N PACKAGE
(TOP VIEW)



[†] $\overline{P = Q}$ for SN74ALS518
P = Q for 'ALS520 and SN74ALS521

SN54ALS520 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE

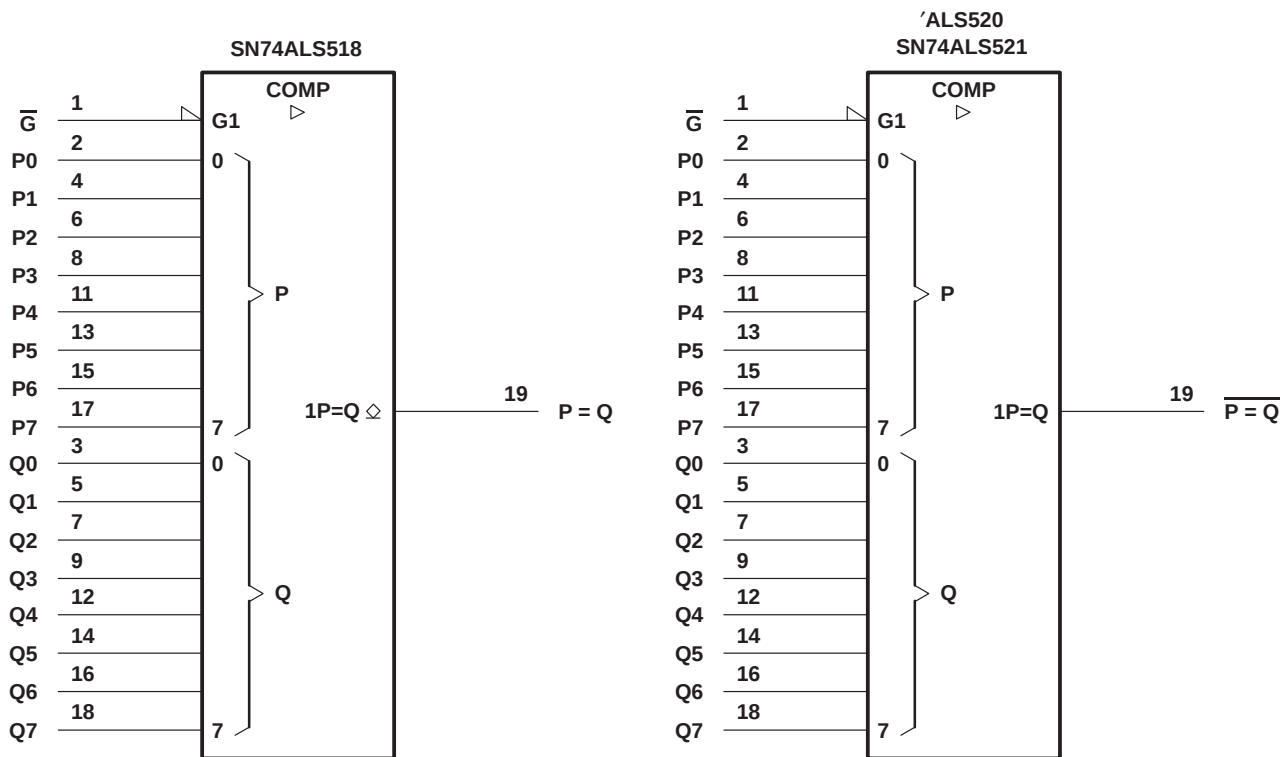
INPUTS		OUTPUTS	
DATA P, Q	ENABLE $\overline{G}$	P = Q	$\overline{P = Q}$
P = Q	L	H	L
P > Q	L	L	H
P < Q	L	L	H
X	H	L	H

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8-BIT IDENTITY COMPARATORS

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logic symbols[†]

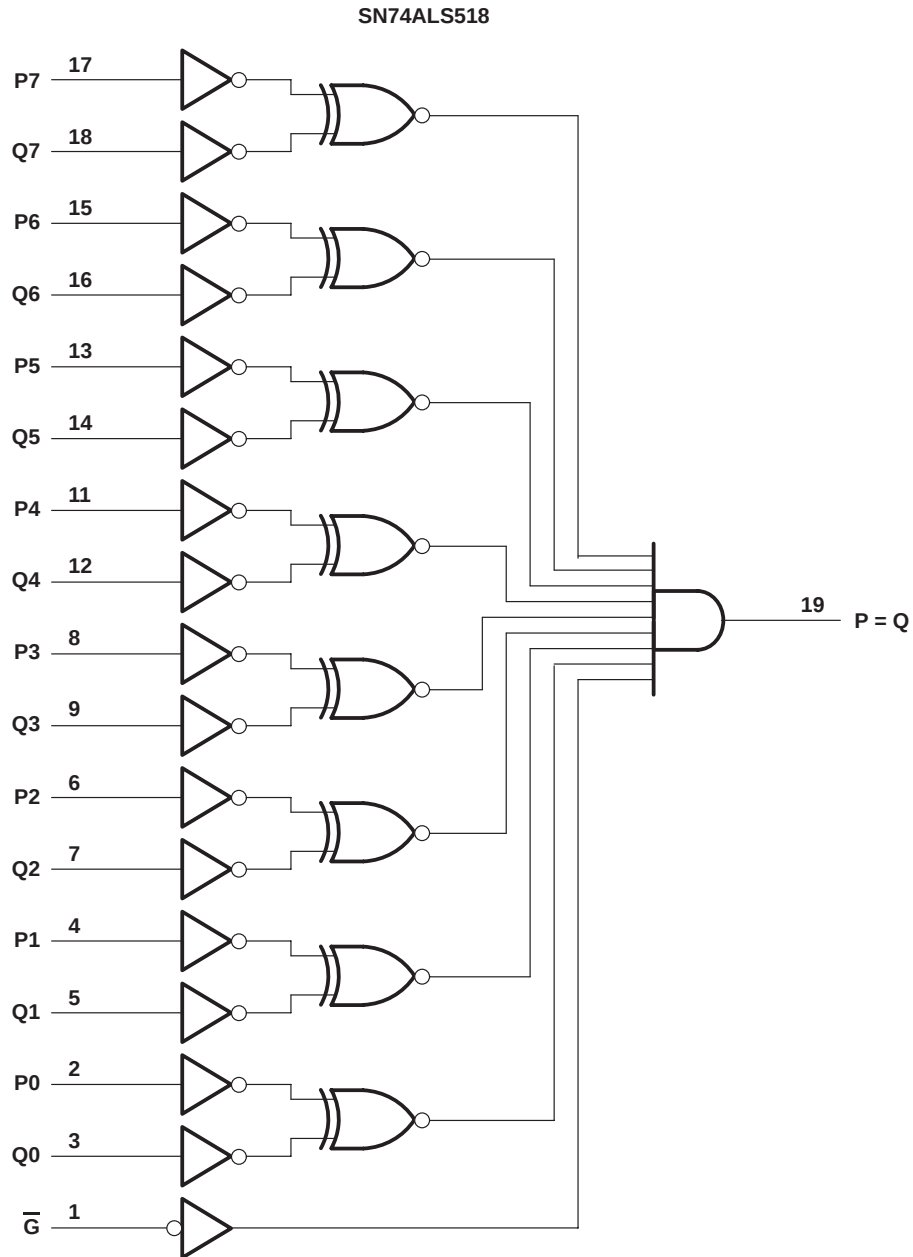


[†] These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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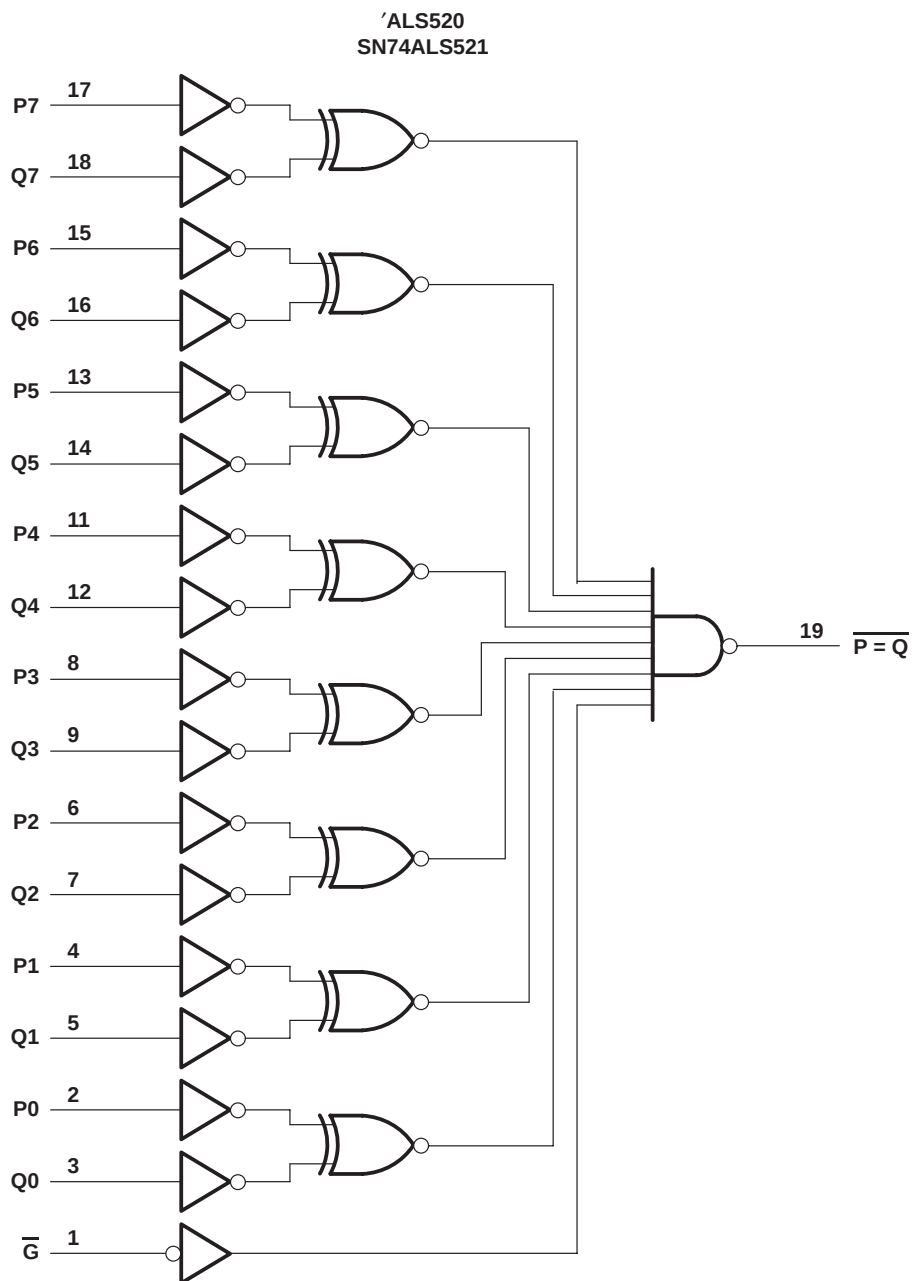
logic diagrams (positive logic)



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logic diagrams (positive logic) (continued)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V_{CC}	7 V
Input voltage, V_I : Q inputs	$V_{CC} + 0.5$ V or 5.5 V, whichever is less
All other inputs	7 V
Off-state output voltage	7 V
Operating free-air temperature range, T_A : SN74ALS518	0°C to 70°C
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN74ALS518			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage			5.5	V
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN74ALS518		UNIT
				MIN	TYP [‡]	MAX
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA			–1.5
I_{OH}		$V_{CC} = 5.5$ V,	$V_{OH} = 5.5$ V			0.1
V_{OL}		$V_{CC} = 4.5$ V	$I_{OL} = 12$ mA		0.25	0.4
			$I_{OL} = 24$ mA		0.35	0.5
I_I	Q inputs	$V_{CC} = 5.5$ V	$V_I = 5.5$ V			0.1
	All other inputs		$V_I = 7$ V			0.1
I_{IH}	Q inputs	$V_{CC} = 5.5$ V,	$V_I = 2.7$ V			–0.2
	All other inputs					20
I_{IL}	Q inputs	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V			–0.6
	All other inputs					–0.1
I_{CC}		$V_{CC} = 5.5$ V,	See Note 1		11	17

[‡] All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$.

NOTE 1: I_{CC} is measured with $\bar{G}$ grounded, and P and Q at 4.5 V.

SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX†		UNIT
			SN74ALS518		
			MIN	MAX	
t _{PLH}	P or Q	P = Q	15	33	ns
t _{PHL}			3	15	
t _{PLH}	$\overline{G}$	P = Q	15	33	ns
t _{PHL}			3	15	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, V _{CC}	7 V
Input voltage, V _I : Q inputs of 'ALS520	V _{CC} + 0.5 V or 5.5 V, whichever is less
All other inputs	7 V
Operating free-air temperature range, T _A : SN54ALS520	–55°C to 125°C
SN74ALS520, SN74ALS521	0°C to 70°C
Storage temperature range	–65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

		SN54ALS520			SN74ALS520 SN74ALS521			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			–1			–2.6	mA
I _{OL}	Low-level output current			12			24	mA
T _A	Operating free-air temperature	–55		125	0		70	°C



SN54ALS520, SN74ALS518, SN74ALS520, SN74ALS521 8-BIT IDENTITY COMPARATORS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS520			SN74ALS520 SN74ALS521			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}		V _{CC} = 4.5 V, I _I = −18 mA		−1.5			−1.5			V
V _{OH}		V _{CC} = 4.5 V to 5.5 V, I _{OH} = −0.4 mA		V _{CC} − 2			V _{CC} − 2			V
		V _{CC} = 4.5 V	I _{OH} = −1 mA	2.4 3.3						
			I _{OH} = −2.6 mA			2.4 3.2				
V _{OL}		V _{CC} = 4.5 V	I _{OL} = 12 mA	0.25 0.4		0.25 0.4			V	
			I _{OL} = 24 mA			0.35 0.5				
I _I	'ALS520 Q inputs	V _{CC} = 5.5 V	V _I = 5.5 V	0.1			0.1			mA
	All other inputs		V _I = 7 V	0.1			0.1			
I _{IH}	'ALS520 Q inputs	V _{CC} = 5.5 V, V _I = 2.7 V		−0.2			−0.2			mA
	All other inputs		20			20			μA	
I _{IL}	'ALS520 Q inputs	V _{CC} = 5.5 V, V _I = 0.4 V		−0.6			−0.6			mA
	All other inputs		−0.1			−0.1				
I _O ‡		V _{CC} = 5.5 V, V _O = 2.25 V	−20	−112		−30	−112			mA
I _{CC}	'ALS520	V _{CC} = 5.5 V, See Note 1	12 19		12 19					mA
	SN74ALS521		12 19		12 19					

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

NOTE 1: I_{CC} is measured with $\bar{G}$ grounded, and P and Q at 4.5 V.

switching characteristics (see Figure 1)

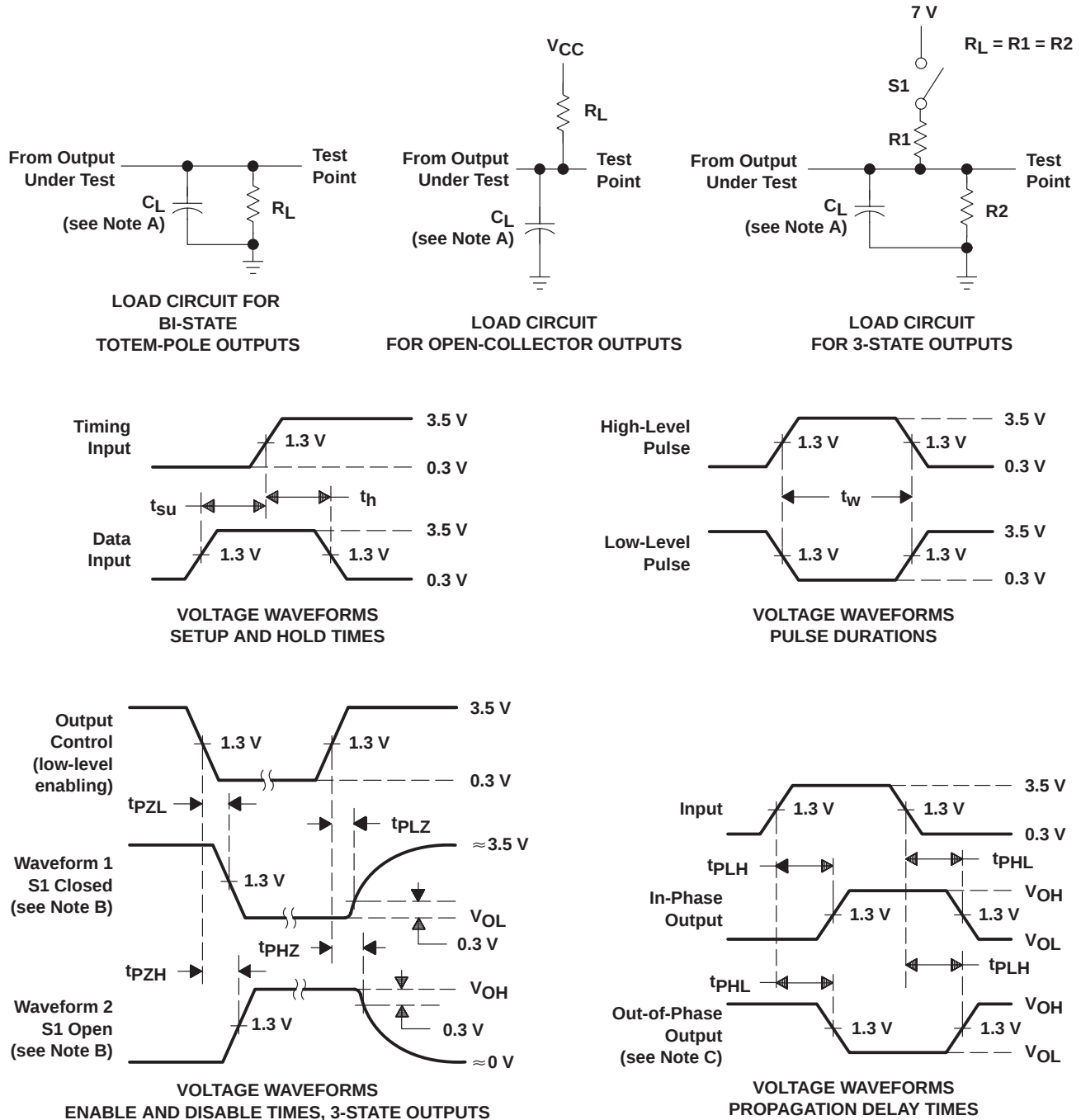
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 500 Ω, T _A = MIN to MAX§				UNIT
			SN54ALS520		SN74ALS520 SN74ALS521		
			MIN	MAX	MIN	MAX	
t _{PLH}	P or Q	$\overline{P} = \overline{Q}$	3	19	3	12	ns
t _{PHL}			3	25	5	20	
t _{PLH}	G	P = Q	2	18	2	12	ns
t _{PHL}			5	23	5	22	

^{\S} For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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PARAMETER MEASUREMENT INFORMATION SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: $PRR \leq 1 \text{ MHz}$, $t_r = t_f = 2 \text{ ns}$, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-88691012A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
5962-8869101RA	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN54ALS520J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC
SN74ALS518DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS518DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS518N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS518NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS518NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS518NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS520DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS520DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS520DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS520DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS520N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS520NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS520NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS520NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS521DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS521DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS521DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS521DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS521N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS521NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS521NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS521NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SNJ54ALS520FK	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Level-NC-NC-NC
SNJ54ALS520J	ACTIVE	CDIP	J	20	1	TBD	Call TI	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-4/F 06/2004

- NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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