IS42S81600A, IS42LS81600A
IS42S16800A, IS42LS16800A
IS42S32400A, IS42LS32400A

ISSI®

16Meg x 8, 8Meg x16 & 4Meg x 32
128-MBIT SYNCHRONOUS DRAM

ADVANCED INFORMATION
AUGUST 2002

FEATURES

- Clock frequency: 133 100, MHz
- Fully synchronous; all signals referenced to a positive clock edge
- Internal bank for hiding row access/precharge
- Power supply

	V_{DD}	V_{DDQ}
IS42LS81600A	2.5V	1.8V (2.5V tolerant)
IS42LS16800A	2.5V	1.8V (2.5V tolerant)
IS42LS32400A	2.5V	1.8V (2.5V tolerant)
IS42S81600A	3.3V	3.3V
IS42S16800A	3.3V	3.3V
IS42S32400A	3.3V	3.3V

- LVTTL interface
- Programmable burst length
  – (1, 2, 4, 8, full page)
- Programmable burst sequence: Sequential/Interleave
- Extended Mode Register
- Programmable Power Reduction Feature by partial array activation during Self-Refresh
- Auto Refresh (CBR)
- Temp. Compensated Self Refresh.
- Self Refresh with programmable refresh periods
- 4096 refresh cycles every 64 ms
- Random column address every clock cycle
- Programmable $\overline{CAS}$ latency (2, 3 clocks)
- Burst read/write and burst read/single write operations capability
- Burst termination by burst stop and precharge command
- Industrial Temperature Availability

OVERVIEW

ISSI's 128Mb Synchronous DRAM achieves high-speed data transfer using pipeline architecture. All inputs and outputs signals refer to the rising edge of the clock input.The 128Mb SDARM is organized as follows.

IS42LS81600A	IS42LS16800A	IS42LS32400A
IS42S81600A	IS42S16800A	IS42S32400A
4M x8x4 Banks	2M x16x4 Banks	2M x16x4 Banks
54pin TSOPII	54ball FBGA	90ball FBGA
	54 pin TSOPII	86pin TSOPII

KEY TIMING PARAMETERS

Parameter	-7	-10	Unit
Clk Cycle Time			
$\overline{CAS}$ Latency = 3	7	10	ns
$\overline{CAS}$ Latency = 2	10	10	ns
Clk Frequency			
$\overline{CAS}$ Latency = 3	133	100	Mhz
$\overline{CAS}$ Latency = 2	100	100	Mhz
Access Time from Clock			
$\overline{CAS}$ Latency = 3	5.4	7	ns
$\overline{CAS}$ Latency = 2	6	9	ns
Row to Column Delay Time (t_{RCD})	15	18	ns
Row Precharge Tim (t_{RP})	15	18	ns

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DEVICE OVERVIEW

The 128Mb SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 2.5V V_{DD} and 1.8V V_{DDQ} or 3.3V_{DD} and 3.3V V_{DDQ} memory systems containing 134,217 ,728 bits. Internally configured as a quad-bank DRAM with a synchronous interface. Each 16,777,216-bit bank is organized as 4,096 rows by 256 columns by 16 bits.

The 128Mb SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK. All inputs and outputs are LVTTL compatible.

Only partials of the memory array can be selected for Self-Refresh and the refresh period during Self-Refresh is progammable in 4 steps which drastically reduces the self refresh current, depending on the case temperature of the components in the system application.

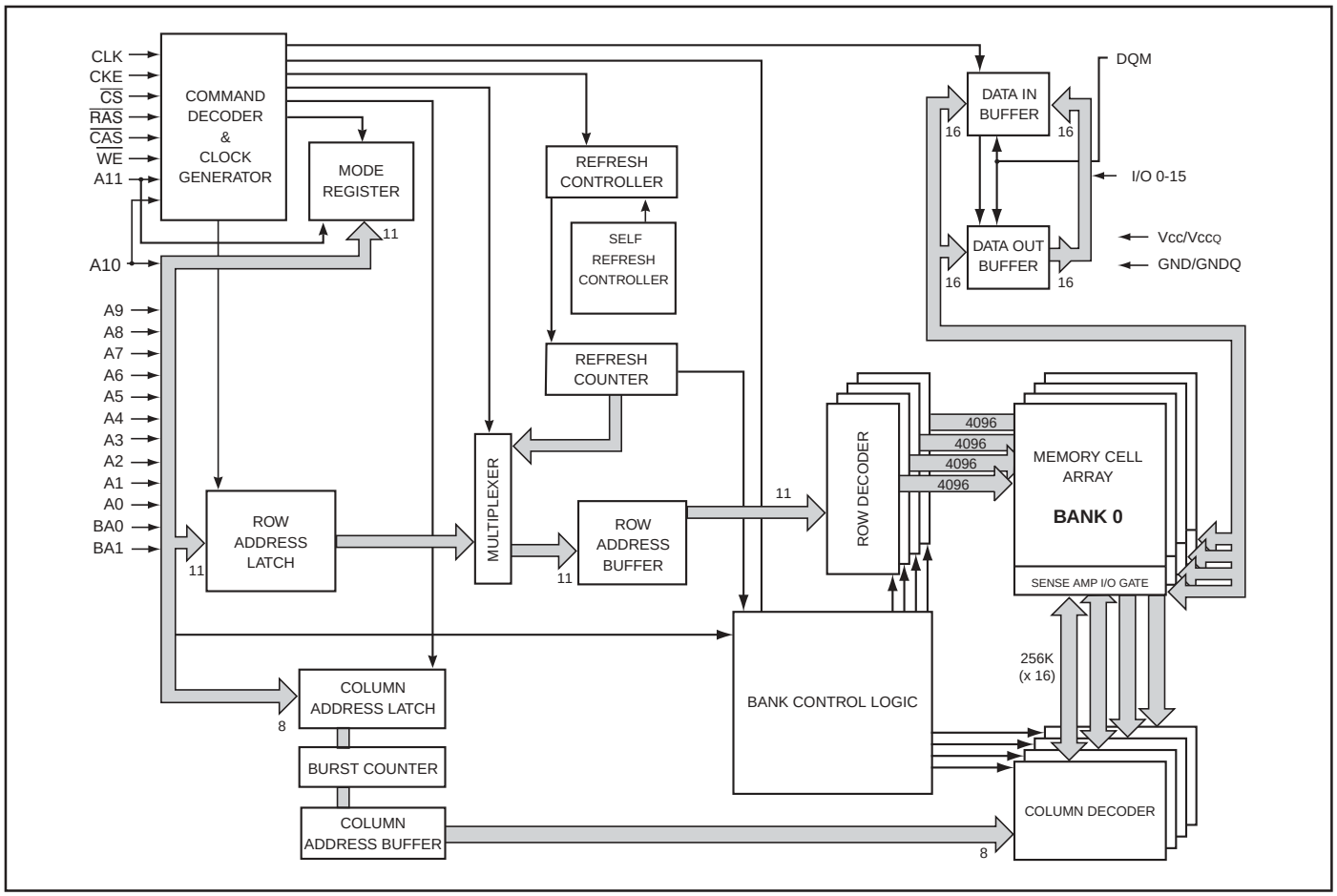
The 128Mb SDRAM has the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks to hide precharge time and the capability to randomly change column addresses on each clock cycle during burst access.

A self-timed row precharge initiated at the end of the burst sequence is available with the AUTO PRECHARGE function enabled. Precharge one bank while accessing one of the other three banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

SDRAM read and write accesses are burst oriented starting at a selected location and continuing for a programmed number of locations in a programmed sequence. The registration of an ACTIVE command begins accesses, followed by a READ or WRITE command. The ACTIVE command in conjunction with address bits registered are used to select the bank and row to be accessed (BA0, BA1 select the bank; A0-A11 select the row). The READ or WRITE commands in conjunction with address bits registered are used to select the starting column location for the burst access.

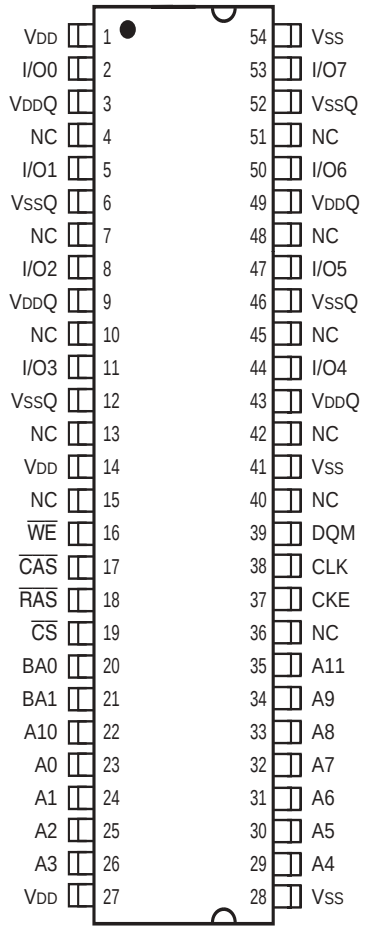
Programmable READ or WRITE burst lengths consist of 1, 2, 4 and 8 locations or full page, with a burst terminate option.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

54 pin TSOP - Type II for x8



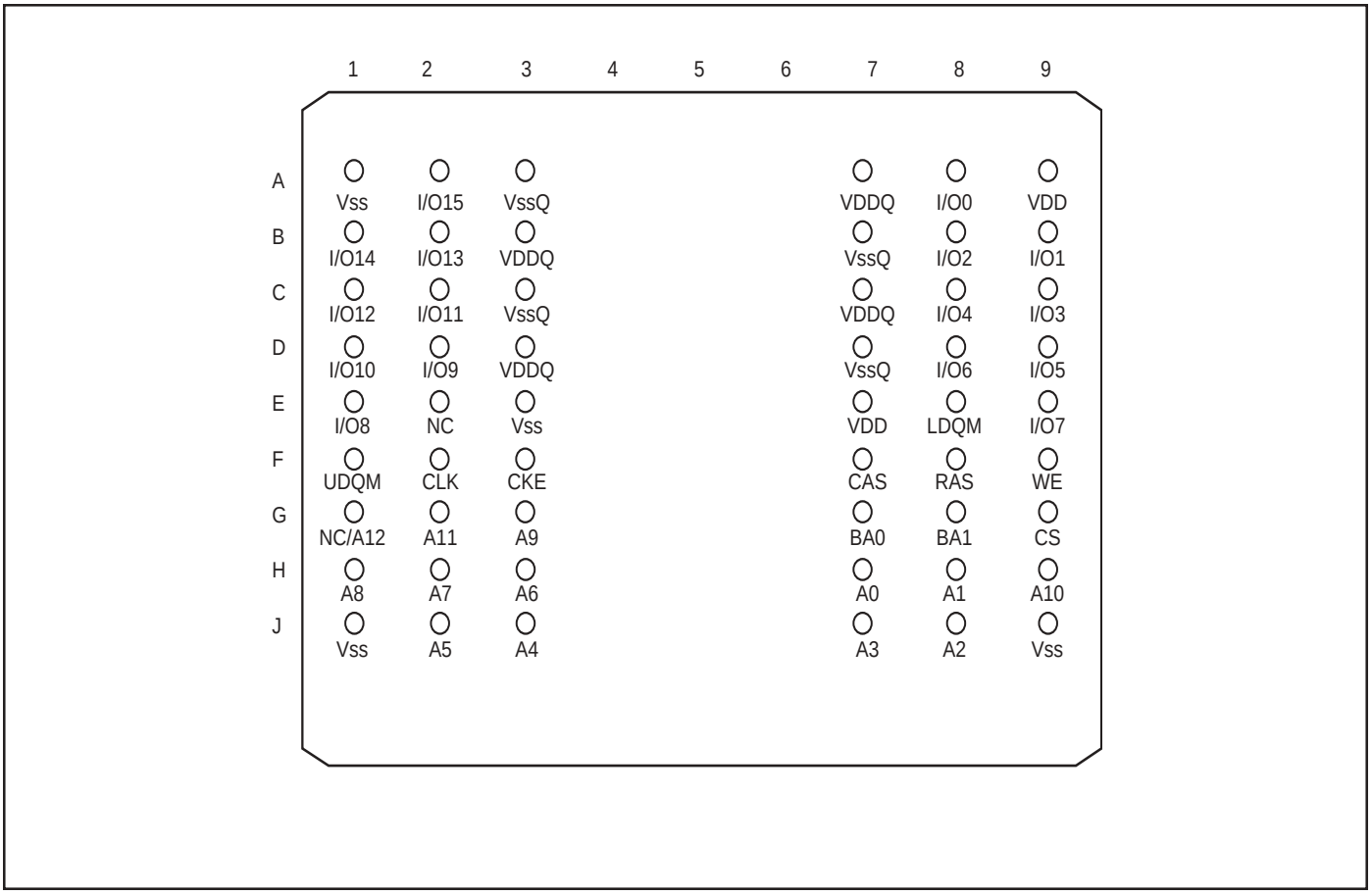
PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A8, A10	Column Address Input
BA0, BA1	Bank Select Address
I/O0 to I/O7	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
DQM	x 8 Lower Bye, Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

54-Ball FBGA for x16



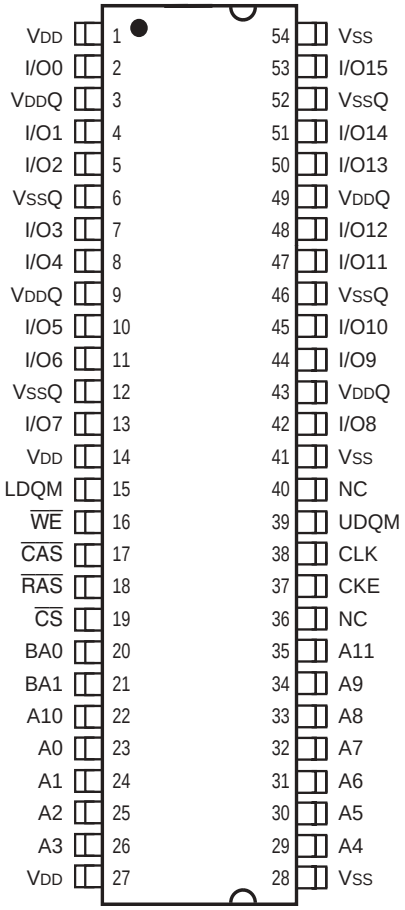
PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A8, A10	Column Address Input
BA0, BA1	Bank Select Address
DQ0 to DQ15	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
LDQM	x16 Lower Bye, Input/Output Mask
UDQM	x16 Upper Bye, Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

54 pin TSOP - Type II for x16



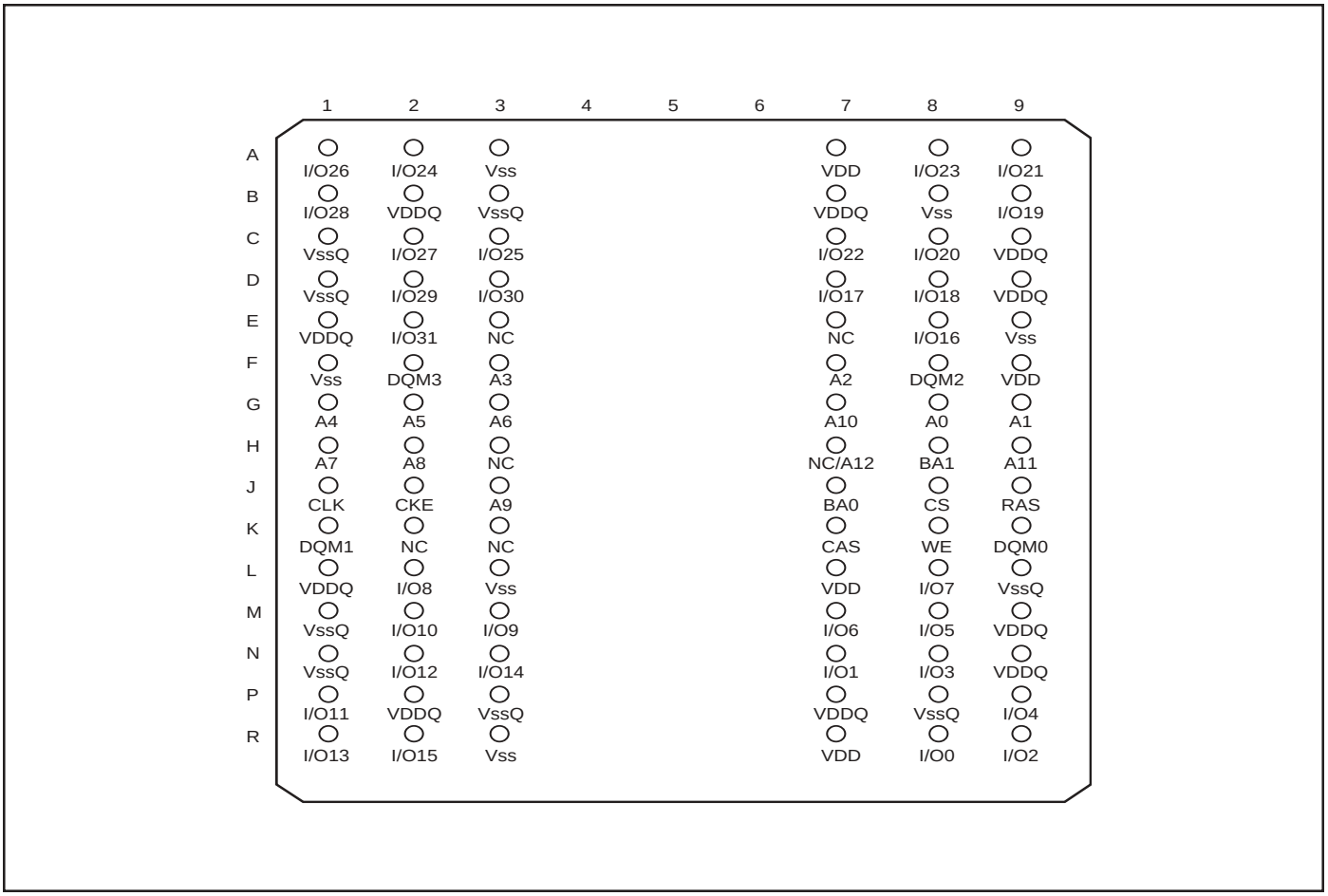
PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A8, A10	Column Address Input
BA0, BA1	Bank Select Address
I/O0 to I/O15	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
LDQM	x16 Lower Bye, Input/Output Mask
UDQM	x16 Upper Bye, Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

90-Ball FBGA for x32



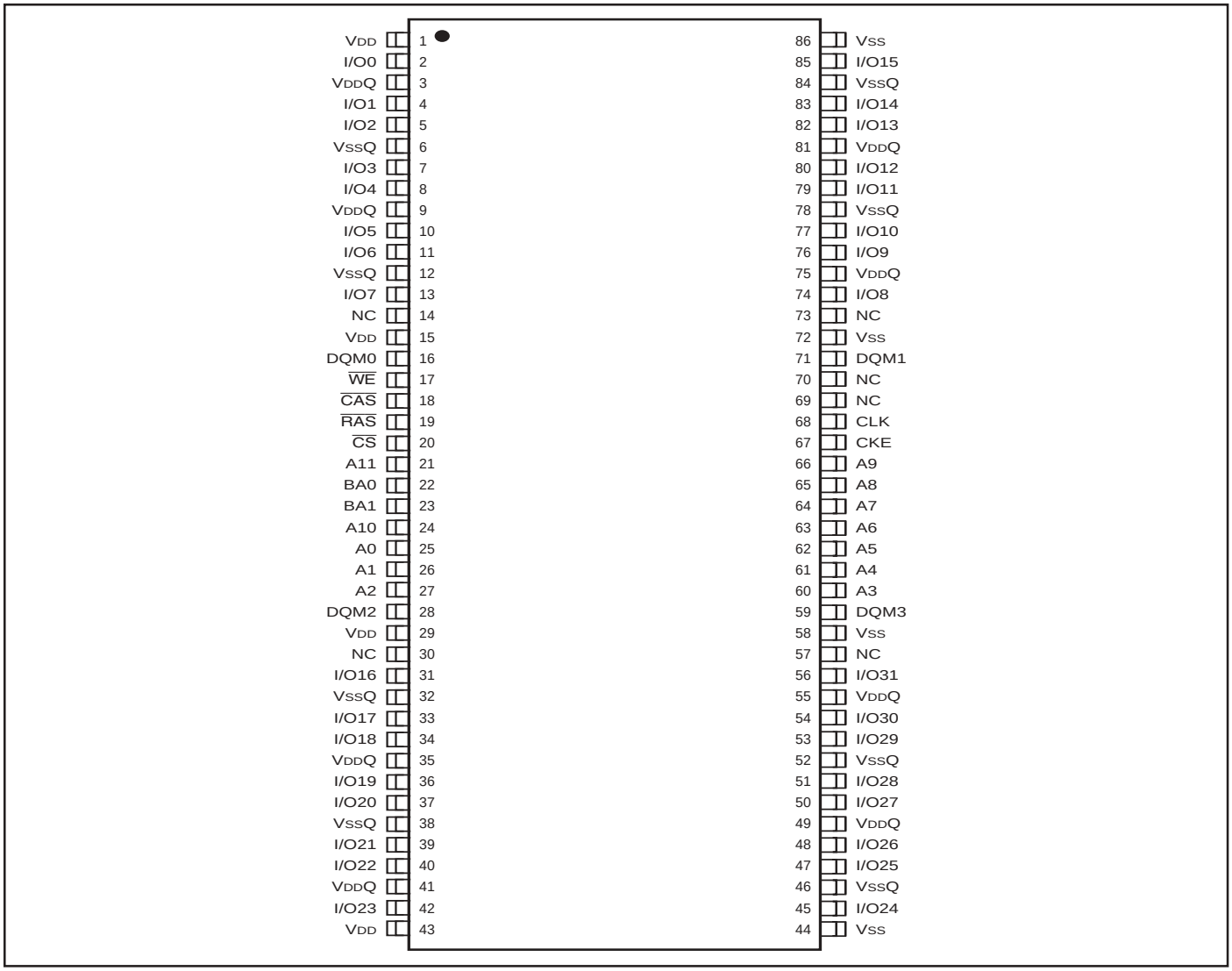
PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A8, A10	Column Address Input
BA0, BA1	Bank Select Address
I/O0 to I/O31	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
DQM0-DQM3	x32 Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN CONFIGURATIONS

86 pin TSOP - Type II for x32



PIN DESCRIPTIONS

A0-A11	Row Address Input
A0-A8, A10	Column Address Input
BA0, BA1	Bank Select Address
I/O0 to I/O31	Data I/O
CLK	System Clock Input
CKE	Clock Enable
$\overline{CS}$	Chip Select
$\overline{RAS}$	Row Address Strobe Command
$\overline{CAS}$	Column Address Strobe Command

$\overline{WE}$	Write Enable
DQM0-DQM3	x32 Input/Output Mask
V_{DD}	Power
Vss	Ground
V_{DDQ}	Power Supply for I/O Pin
V_{SSQ}	Ground for I/O Pin
NC	No Connection

PIN FUNCTIONS

Symbol	Type	Function (In Detail)
A0-A11	Input Pin	Address Inputs: A0-A11 are sampled during the ACTIVE command (row-address A0-A11) and READ/WRITE command (A0-A7 with A10 defining auto precharge) to select one location out of the memory array in the respective bank. A10 is sampled during a PRECHARGE command to determine if all banks are to be precharged (A10 HIGH) or bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
BA0, BA1	Input Pin	Bank Select Address: BA0 and BA1 defines which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied.
$\overline{CAS}$	Input Pin	$\overline{CAS}$, in conjunction with the $\overline{RAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" for details on device commands.
CKE	Input Pin	The CKE input determines whether the CLK input is enabled. The next rising edge of the CLK signal will be valid when is CKE HIGH and invalid when LOW. When CKE is LOW, the device will be in either power-down mode, clock suspend mode, or self refresh mode. CKE is an asynchronous input.
CLK	Input Pin	CLK is the master clock input for this device. Except for CKE, all inputs to this device are acquired in synchronization with the rising edge of this pin.
$\overline{CS}$	Input Pin	The $\overline{CS}$ input determines whether command input is enabled within the device. Command input is enabled when $\overline{CS}$ is LOW, and disabled with $\overline{CS}$ is HIGH. The device remains in the previous state when $\overline{CS}$ is HIGH.
I/O0 to I/O32	I/O Pin	I/O0 to I/O32 are I/O pins. I/O through these pins can be controlled in byte units using the LDQM and UDQM pins.
LDQM, UDQM	Input Pin	LDQM and UDQM control the lower and upper bytes of the I/O buffers. In read mode, LDQM and UDQM control the output buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and when HIGH, disabled. The outputs go to the HIGH impedance state when LDQM/UDQM is HIGH. This function corresponds to $\overline{OE}$ in conventional DRAMs. In write mode, LDQM and UDQM control the input buffer. When LDQM or UDQM is LOW, the corresponding buffer byte is enabled, and data can be written to the device. When LDQM or UDQM is HIGH, input data is masked and cannot be written to the device.
DQM0-DQM3	Input Pin	
DQM	Input Pin	
$\overline{RAS}$	Input Pin	$\overline{RAS}$, in conjunction with $\overline{CAS}$ and $\overline{WE}$, forms the device command. See the "Command Truth Table" item for details on device commands.
$\overline{WE}$	Input Pin	$\overline{WE}$, in conjunction with $\overline{RAS}$ and $\overline{CAS}$, forms the device command. See the "Command Truth Table" item for details on device commands.
V_{DDQ}	Power Supply Pin	V_{DDQ} is the output buffer power supply.
V_{DD}	Power Supply Pin	V_{DD} is the device internal power supply.
V_{SSQ}	Power Supply Pin	V_{SSQ} is the output buffer ground.
V_{SS}	Power Supply Pin	V_{SS} is the device internal ground.

GENERAL DESCRIPTION

READ

The READ command selects the bank from BA0, BA1 inputs and starts a burst read access to an active row. Inputs A0-A7 provides the starting column location. When A10 is HIGH, this command functions as an AUTO PRECHARGE command. When the auto precharge is selected, the row being accessed will be precharged at the end of the READ burst. The row will remain open for subsequent accesses when AUTO PRECHARGE is not selected. DQ's read data is subject to the logic level on the DQM inputs two clocks earlier. When a given DQM signal was registered HIGH, the corresponding DQ's will be High-Z two clocks later. DQ's will provide valid data when the DQM signal was registered LOW.

WRITE

A burst write access to an active row is initiated with the WRITE command. BA0, BA1 inputs selects the bank, and the starting column location is provided by inputs A0-A7. Whether or not AUTO-PRECHARGE is used is determined by A10.

The row being accessed will be precharged at the end of the WRITE burst, if AUTO PRECHARGE is selected. If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses.

A memory array is written with corresponding input data on DQ's and DQM input logic level appearing at the same time. Data will be written to memory when DQM signal is LOW. When DQM is HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. BA0, BA1 can be used to select which bank is precharged or they are treated as "Don't Care". A10 determined whether one or all banks are precharged. After executing this command, the next command for the selected banks(s) is executed after passage of the period t_{RP}, which is the period required for bank precharging. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

AUTO PRECHARGE

The AUTO PRECHARGE function ensures that the precharge is initiated at the earliest valid stage within a burst. This function allows for individual-bank precharge without requiring an explicit command. A10 to enables the AUTO PRECHARGE function in conjunction with a specific READ or WRITE command. For each individual READ or WRITE command, auto precharge is either enabled or disabled. AUTO PRECHARGE does not apply except in full-page burst mode. Upon completion of the READ or WRITE burst, a precharge of the bank/row that is addressed is automatically performed.

AUTO REFRESH COMMAND

This command executes the AUTO REFRESH operation. The row address and bank to be refreshed are automatically generated during this operation. The stipulated period (t_{RC}) is required for a single refresh operation, and no other commands can be executed during this period. This command is executed at least 4096 times for every 64ms. During an AUTO REFRESH command, address bits are "Don't Care". This command corresponds to CBR Auto-refresh.

BURST TERMINATE

The BURST TERMINATE command forcibly terminates the burst read and write operations by truncating either fixed-length or full-page bursts and the most recently registered READ or WRITE command prior to the BURST TERMINATE.

COMMAND INHIBIT

COMMAND INHIBIT prevents new commands from being executed. Operations in progress are not affected, apart from whether the CLK signal is enabled

NO OPERATION

When $\overline{CS}$ is low, the NOP command prevents unwanted commands from being registered during idle or wait states.

LOAD MODE REGISTER

During the LOAD MODE REGISTER command the mode register is loaded from A0-A11. This command can only be issued when all banks are idle.

EXTENDED MODE REGISTER

The extended mode register defines low power functions. During this command A0-A11 are data input pins. After power on, the extended mode register set command must be executed to fix low power functions. During tRSC following this command, they can not accept any other command.

GENERAL DESCRIPTION Continued:

The extended mode register has four fields:

Options: A11-A7

Drive Strength: A6-A5

Temperature Compensated self Refresh: A4-A3

Partial Array Self Refresh: A2-A0

Following extended mode register programming, no command can be issued before at least 2 CLK have elapsed.

ACTIVE COMMAND

When the ACTIVE COMMAND is activated, BA0, BA1 inputs selects a bank to be accessed, and the address inputs on A0-A11 selects the row. Until a PRECHARGE command is issued to the bank, the row remains open for accesses.

COMMAND TRUTH TABLE

Function Symbol	CKE n – 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA1	BA0	A10	A11 A9 - A0
Device deselect	H	×	H	×	×	×	×	×	×	×
No operation H	×	L	H	H	H	×	×	×		
Burst stop	H	H	L	H	H	L	×	×	×	×
Read	H	×	L	H	L	H	V	V	L	V
Read with auto precharge	H	×	L	H	L	H	V	V	H	V
Write	H	×	L	H	L	L	V	V	L	V
Write with auto precharge	H	×	L	H	L	L	V	V	H	V
Bank activate	H	×	L	L	H	H	V	V	V	V
Precharge select bank	H	×	L	L	H	L	V	V	L	×
Precharge all banks	H	×	L	L	H	L	×	×	H	×
Mode register set	H	×	L	L	L	L	L	L	L	V
Extended mode reg set	H	×	L	L	L	L	H	L	L	V

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

DQM TRUTH TABLE

Function Symbol	CKE n-1	CKE n	DQM U	DQM L
Data write / output enable	H	×	L	L
Data mask / output disable	H	×	H	H
Upper byte write enable / output enable	H	×	L	×
Lower byte write enable / output enable	H	×	×	L
Upper byte write inhibit / output disable	H	×	H	×
Lower byte write inhibit / output disable	H	×	×	H

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

CKE TRUTH TABLE

Current State /Function	CKE n – 1	CKE n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address
Activating Clock suspend mode entry	H	L	×	×	×	×	×
Any Clock suspend mode	L	L	×	×	×	×	×
Clock suspend mode exit	L	H	×	×	×	×	×
Auto refresh command Idle	H	H	L	L	L	H	×
Self refresh entry Idle	H	L	L	L	L	H	×
Power down entry Idle	H	L	L	H	H	H	×
	H	L	H	×	×	×	×
Deep power down entry	H	L	L	H	H	L	×
Self refresh exit	L	H	L	H	H	H	×
	L	H	H	×	×	×	×
Power down exit	L	H	L	H	H	H	×
	L	H	H	×	×	×	×
Deep power down exit	L	H	×	×	×	×	×

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data.

FUNCTIONAL TRUTH TABLE

	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Idle	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	Nop
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (2)
	L	H	L	L	A, CA, A10	WRIT/WRITA	ILLEGAL(2)
	L	L	H	H	BA, RA	ACT	Row activating
	L	L	H	L	A, A10	PRE/PALL	Nop
	L	L	L	H	X	REF	Auto refresh
	L	L	L	L	OC, BA1=L	MRS	Mode register set
	L	L	L	L	OC, BA1=H	EMRS	Extended mode register set
Row Active	H	X	X	X	X	DESL	Nop
	L	H	H	H	X	NOP	Nop
	L	H	H	L	X	BST	Nop
	L	H	L	H	BA, CA, A10	READ/READA	Begin read (3)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin write (3)
	L	L	H	H	BA, RA	ACT	ILLEGAL (2)
	L	L	H	L	BA, A10	PRE/PALL	Precharge/Precharge all banks(
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Read	H	X	X	X	X	DESL	Continue burst to end to Row active
	L	H	H	H	X	NOP	Continue burst to end Row Row active
	L	H	H	L	X	BST	Burst stop Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, begin new read (5)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, begin write (5, 6)
	L	L	H	H	BA, RA	ACT	ILLEGAL (2)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Write	H	X	X	X	X	DESL	Continue burst to end Write recovering
	L	H	H	H	X	NOP	Continue burst to end Write recovering
	L	H	H	L	X	BST	Burst stop Row active
	L	H	L	H	BA, CA, A10	READ/READA	Terminate burst, start read : Determine AP (5, 6)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Terminate burst, new write : Determine AP (5)
	L	L	H	H	BA,	RA ACT	ILLEGAL (2)
	L	L	H	L	BA, A10	PRE/PALL	Terminate burst Precharging (7)
	L	L	L	H	X	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Read with auto Precharging	H	×	×	×	×	DESL	Continue burst to end -
Precharge Precharging	L	H	H	H	x	NOP	Continue burst to end -
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (2)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (2)
	L	L	H	H	BA, RA	ACT	ILLEGAL (2)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (2)
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Write with Auto Precharge	H	×	×	×	×	DESL	Continue burst to end -Write recovering with auto precharge
	L	H	H	H	×	NOP	Continue burst to end -Write recoveringwith auto precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL(2)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (2)
	L	L	H	H	BA, RA		
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (2)
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Precharging	H	×	×	×	×	DESL	Nop Enter idle after tRP
	L	H	H	H	×	NOP	Nop Enter idle after tRP
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (2)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (2)
	L	L	H	H	BA, RA	ACT I	LLEGAL(2)
	L	L	H	L	BA, A10	PRE/PALL	Nop Enter idle after tRP
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Row Activating	H	×	×	×	×	DESL	Nop Enter bank active after tRCD
	L	H	H	H	×	NOP	Nop Enter bank active after tRCD
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL (2)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (2)
	L	L	H	H	BA, RA	ACT	ILLEGAL (2,8)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (2)
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

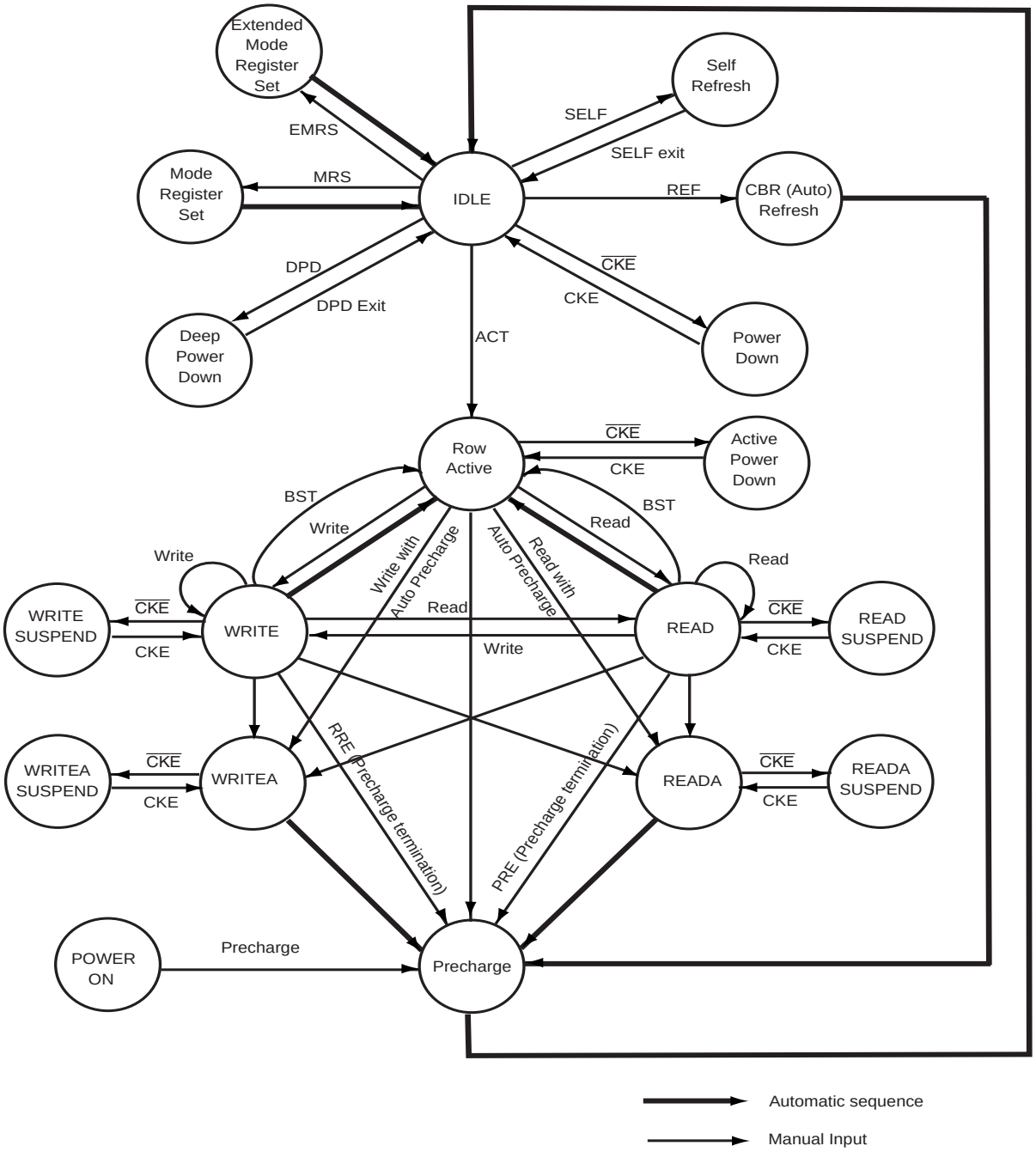
	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action
Write Recovering	H	×	×	×	×	DESL	Nop Enter row active after tDPL
	L	H	H	H	×	NOP	Nop Enter row active after tDPL
	L	H	H	L	×	BST	Nop Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	Begin read (6)
	L	H	L	L	BA, CA, A10	WRIT/WRITA	Begin new write
	L	L	H	H	BA, RA	ACT	ILLEGAL (2)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (2)
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Write Recovering	H	×	×	×	×	DESL	Nop Enter precharge after tDPL
with Auto	L	H	H	H	×	NOP	Nop Enter precharge after tDPL
Precharge	L	H	H	L	×	BST	Nop Enter row active after tDPL
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL (2, 6)
	L	L	H	H	BA, RA	ACT	ILLEGAL (2)
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL (2)
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Refresh	H	×	×	×	×	DESL	Enter idle after tRC1
	L	H	H	H	×	NOP	Nop Enter idle after tRC1
	L	H	H	L	×	BST	Nop Enter idle after tRC1
	L	H	L	H	BA, CA, A10	EAD/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL
Mode Register	H	×	×	×	×	DESL	Nop Enter idle after tRSC
Accessing	L	H	H	H	×	NOP	Nop Enter idle after tRSC
	L	H	H	L	×	BST	Nop Enter idle after tRSC
	L	H	L	H	BA, CA, A10	READ/READA	ILLEGAL
	L	H	L	L	BA, CA, A10	WRIT/WRITA	ILLEGAL
	L	L	H	H	BA, RA	ACT	ILLEGAL
	L	L	H	L	BA, A10	PRE/PALL	ILLEGAL
	L	L	L	H	×	REF	ILLEGAL
	L	L	L	L	OC, BA	MRS/EMRS	ILLEGAL

Note: H=V_{IH}, L=V_{IL} x= V_{IH} or V_{IL}, V = Valid Data, BA= Bank Address, CA+Column Address, RA=Row Address, OC= Op-Code

FUNCTIONAL TRUTH TABLE Continued:

Notes:
1. All entries assume that CKE is active (CKEn-1=CKEn=H).
2. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
3. Illegal if tRCD is not satisfied.
4. Illegal if tRAS is not satisfied.
5. Must satisfy burst interrupt condition.
6. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
7. Must mask preceding data which don't satisfy tDPL.
8. Illegal if tRRD is not satisfied.

STATE DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters		Rating		Unit
$V_{DD\ MAX}$	Maximum Supply Voltage		–0.5 to +3.6	–0.5 to +4.6	V
$V_{DDQ\ MAX}$	Maximum Supply Voltage for Output Buffer			–0.5 to +3.6	–0.5 to +4.6 V
V_{IN}	Input Voltage		–0.5 to +3.6	–0.5 to +4.6	V
V_{OUT}	Output Voltage		–0.5 to +3.6	–0.5 to +4.6	V
$P_{D\ MAX}$	Allowable Power Dissipation		1	1	W
I_{CS}	Output Shorted Current		50	50	mA
T_{OPR}	Operating Temperature	Com. Ind.	0 to +70 –40 to +85	0 to +70 –40 to +85	°C
T_{STG}	Storage Temperature		–55 to +125	–55 to +125	°C

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. All voltages are referenced to Vss.

DC RECOMMENDED OPERATING CONDITIONS(2) (At T_A = 0 to +70°C)

		42LSxxxxxx			42Sxxxxxx			
Symbol	Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	2.3	2.5	2.7	3.0	3.3	3.6	V
V_{DDQ}	I/O Supply Voltage	1.65	2.0	2.5	3.0	3.3	3.6	V
V_{IH}(1)	Input High Voltage	0.8xV_{DDQ}	—	V_{DDQ} + 0.3	2.0	—	V_{DDQ} + 0.3	V
V_{IL}(2)	Input Low Voltage	-0.3	—	+0.3	-0.3	—	+0.8	V

Note:

1. V_{IH} (max) = V_{DDQ} +1.5V (PULSE WIDTH ≤ 5NS).
2. V_{IL} (min) = -1.5V (PULSE WIDTH ≤ 5NS).

CAPACITANCE CHARACTERISTICS(1,2) (At T_A = 0 to +25°C, Vdd = Vdd_Q= 3.3 ± 0.3V, f = 1 MHz)

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Input Capacitance: A0-A11, BA0, BA1	—	3.5	pF
C_{IN2}	Input Capacitance: (CLK, CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, LDQM, UDQM)	—	3.8	pF
CI/O	Data Input/Output Capacitance: I/O0-I/O15	—	6.5	pss.

DC ELECTRICAL CHARACTERISTICS (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition			Speed	Min.	Max.	Unit
I_{IL}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{DD}, with pins other than the tested pin at 0V				–5	5	µA
I_{OL}	Output Leakage Current	Output is disabled, 0V ≤ V_{OUT} ≤ V_{DD}				–5	5	µA
V_{OH}	Output High Voltage Level	I_{OUT} = –2 mA				2.4	—	V
V_{OL}	Output Low Voltage Level	I_{OUT} = +2 mA				—	0.4	V
I_{DD1}	Operating Current[1,2]	One Bank Operation,	$\overline{CAS}$ latency = 3					
		Burst Length=1		Com.	-7	—	120	mA
		$t_{RC} \geq t_{RC}$ (min.)		Ind.	-7	—	140	mA
		I_{OUT} = 0mA		Com.	-10	—	110	mA
				Ind.	-10	—	120	mA
I_{DD2P}	Precharge Standby Current	CKE ≤ V_{IL} (MAX)	$t_{CK} = t_{CK}$ (MIN)	Com.	—	—	1	mA
				Ind.	—	—	1	mA
I_{DD2PS}	(In Power-Down Mode)		$t_{CK} = \infty$	Com.	—	—	.6	mA
				Ind.	—	—	.6	mA
I_{DD2N}	Precharge Standby Current	CKE ≥ V_{IH} (MIN)	$t_{CK} = t_{CK}$ (MIN)		—	—	11	mA
I_{DD2NS}	(In Non Power-Down Mode)		$t_{CK} = \infty$	Com.	—	—	5	mA
				Ind.	—	—	7	mA
I_{DD3P}	Active Standby Current	CKE ≤ V_{IL} (MAX)	$t_{CK} = t_{CK}$ (MIN)	Com.	—	—	4	mA
			Ind.	Ind.	—	—	6	mA
I_{DD3PS}	(In Power-Down Mode)		$t_{CK} = \infty$	Com.	—	—	3	mA
				Ind.	—	—	5	mA
I_{DD3N}	Active Standby Current	CKE ≥ V_{IH} (MIN)	$t_{CK} = t_{CK}$ (MIN)		—	—	28	mA
I_{DD3NS}	(In Non Power-Down Mode)		$t_{CK} = \infty$	Com.	—	—	17	mA
				Ind.	—	—	20	mA
I_{DD4}	Operating Current	$t_{CK} = t_{CK}$ (MIN)	$\overline{CAS}$ latency = 3					
	(In Burst Mode)[1]	I_{OUT} = 0mA		Com.	-7	—	120	mA
				Ind.	-7	—	140	mA
				Com.	-10	—	110	mA
				Ind.	-10	—	120	mA
			$\overline{CAS}$ latency = 2					
				Com.	-7	—	90	mA
				Ind.	-7	—	110	mA
				Com.	-10	—	80	mA
				Ind.	-10	—	100	mA

Notes:
1. These are the values at the minimum cycle time. Since the currents are transient, these values decrease as the cycle time increases. Also note that a bypass capacitor of at least 0.01 µF should be inserted between Vdd and Vss for each memory chip to suppress power supply voltage noise (voltage drops) due to these transient currents.
2. I_{DD1} and I_{DD4} depend on the output load. The maximum values for I_{DD1} and I_{DD4} are obtained with the output open state.

DC ELECTRICAL CHARACTERISTICS (Recommended Operation Conditions unless otherwise noted.)

Symbol	Parameter	Test Condition		Speed	Min.	Max.	Unit
I_{DD5}	Auto-Refresh Current	$t_{RC} = t_{RC}$ (MIN)	$\overline{CAS}$ latency = 3				
			Com.	-7	—	330	mA
			Ind.	-7	—	350	mA
			Com.	-10	—	300	mA
			Ind.	-10	—	330	mA
			$\overline{CAS}$ latency = 2				
			Com.	-7	—	330	mA
			Ind.	-7	—	350	mA
			Com.	-10	—	300	mA
			Ind.	-10	—	330	mA
I_{DD6}	Self-Refresh Current	CKE ≤ 0.2V, t_{CSR} = 00					
	PASR=000 (full)	ts ≤ 70°C		—	—	0.35	mA
	PASR=001 (2BK)			—	—	0.25	mA
	PASR=010 (1BK)			—	—	0.18	mA
	PASR=101 (1/2BK)			—	—	0.12	mA
	PASR=110 (1/4BK)			—	—	0.09	mA
I_{DD6}	Self-Refresh Current	CKE ≤ 0.2V, , t_{CSR} = 01					
	PASR=000 (full)	ts ≤ 45°C		—	—	0.20	mA
	PASR=001 (2BK)			—	—	0.15	mA
	PASR=010 (1BK)			—	—	0.10	mA
	PASR=101 (1/2BK)			—	—	0.08	mA
	PASR=110 (1/4BK)			—	—	0.07	mA
I_{DD6}	Self-Refresh Current	CKE ≤ 0.2V, , t_{CSR} = 11					
	PASR=000 (full)	ts ≤ 85°C		—	—	0.60	mA
	PASR=001 (2BK)			—	—	0.50	mA
	PASR=010 (1BK)			—	—	0.43	mA
	PASR=101 (1/2BK)			—	—	0.37	mA
	PASR=110 (1/4BK)			—	—	0.34	mA
I_{DD7}	Standby Current in Deep Power Down Mode	CKE ≤ 0.2V		—	—	10	µA

AC ELECTRICAL CHARACTERISTICS (1,2,3)

			-7		-10		
Symbol	Parameter		Min.	Max.	Min.	Max	Units
t_{CK3}	Clock Cycle Time	$\overline{CAS}$ Latency = 3	7	—	10	—	ns
t_{CK2}		$\overline{CAS}$ Latency = 2	10	—	10	—	ns
t_{AC3}	Access Time From CLK(4)	$\overline{CAS}$ Latency = 3	—	5.4	—	7	ns
t_{AC2}		$\overline{CAS}$ Latency = 2	—	6	—	9	ns
t_{CHI}	CLK HIGH Level Width		2.5	—	3.5	—	ns
t_{CL}	CLK LOW Level Width		2.5	—	3.5	—	ns
t_{OH3}	Output Data Hold Time	$\overline{CAS}$ Latency = 3	2.5	—	2.5	—	ns
t_{OH2}		$\overline{CAS}$ Latency = 2	2.5	—	2.5	—	ns
t_{LZ}	Output LOW Impedance Time		0	—	0	—	ns
t_{HZ3}	Output HIGH Impedance Time(5)	$\overline{CAS}$ Latency = 3	—	6	—	7	ns
t_{HZ2}		$\overline{CAS}$ Latency = 2	—	6	—	9	ns
t_{DS}	Input Data Setup Time		1.5	—	2.0	—	ns
t_{DH}	Input Data Hold Time		0.8	—	1	—	ns
t_{AS}	Address Setup Time		.5	—	2.0	—	ns
t_{AH}	Address Hold Time		0.8	—	1	—	ns
t_{CKS}	CKE Setup Time		1.5	—	2.0	—	ns
t_{CKH}	CKE Hold Time		0.8	—	1	—	ns
t_{CKA}	CKE to CLK Recovery Delay Time		1CLK+3	—	1CLK+3	—	ns
t_{CS}	Command Setup Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)		1.5	—	2.0	—	ns
t_{CH}	Command Hold Time ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM)			0.8	—	1	—
ns							
t_{RC}	Command Period (REF to REF / ACT to ACT)		63	—	70	—	ns
t_{RAS}	Command Period (ACT to PRE)		37	120,000	44	120,000	ns
t_{RP}	Command Period (PRE to ACT)		15	—	18	—	ns
t_{RCD}	Active Command To Read / Write Command Delay Time		15	—	18	—	ns
t_{RRD}	Command Period (ACT [0] to ACT[1])		14	—	15	—	ns
t_{DPL3}	Input Data To Precharge Command Delay time	$\overline{CAS}$ Latency = 3	2CLK	—	2CLK	—	ns
t_{DPL2}		$\overline{CAS}$ Latency = 2	2CLK	—	2CLK	—	ns
t_{DAL3}	Input Data To Active / Refresh Command Delay time (During Auto-Precharge)	$\overline{CAS}$ Latency = 3	CLK+t_{RP}	—	2CLK+t_{RP}	—	ns
t_{DAL2}		$\overline{CAS}$ Latency = 2	2CLK+t_{RP}	—	2CLK+t_{RP}	—	ns
t_T	Transition Time		0.5	30	0.5	30	ns
t_{REF}	Refresh Cycle Time (4096)		—	64	—	64	ms

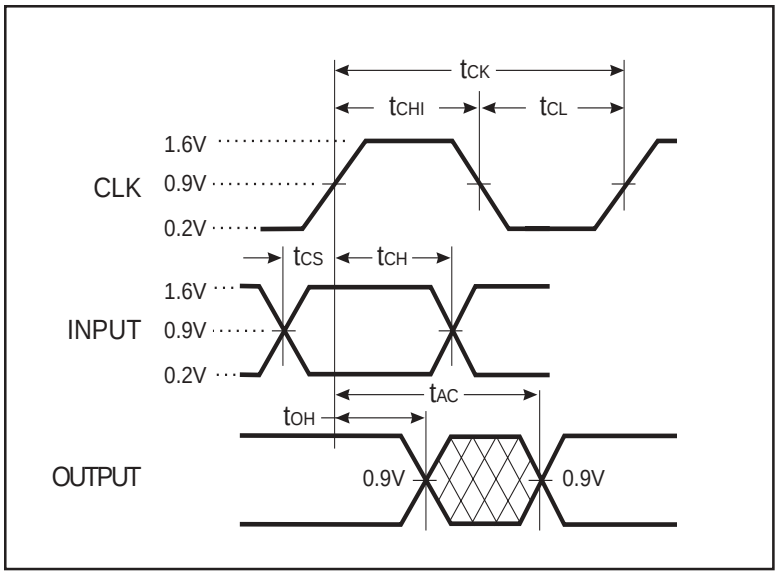
Notes:
1. When power is first applied, memory operation should be started 100 µs after Vdd and V_{DDQ} reach their stipulated voltages. Also note that the power-on sequence must be executed before starting memory operation.
2. Measured with t_T = 1 ns.
3. The reference level is 0.9V when measuring input signal timing. Rise and fall times are measured between V_{IH} (min.) and V_{IL} (max.).
4. Access time is measured at 0.9V with the load shown in the figure below.
5. The time t_{HZ} (max.) is defined as the time required for the output voltage to transition by ± 200 mV from V_{OH} (min.) or V_{OL} (max.) when the output is in the high impedance state.

OPERATING FREQUENCY / LATENCY RELATIONSHIPS

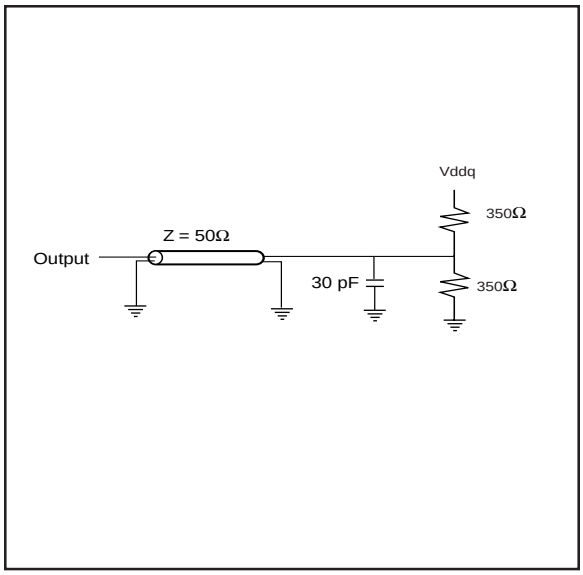
SYMBOL	PARAMETER		-7	-10.	UNITS
—	Clock Cycle Time		7	10	ns
—	Operating Frequency		133	100	MHz
t_{CCD}	READ/WRITE command to READ/WRITE command		1	1	cycle
t_{CKED}	CKE to clock disable or power-down entry mode		1	1	cycle
t_{PED}	CKE to clock enable or power-down exit setup mode		1	1	cycle
t_{DQD}	DQM to input data delay		0	0	cycle
t_{DQM}	DQM to data mask during WRITEs		0	0	cycle
t_{DQZ}	DQM to data high-impedance during READs		2	2	cycle
t_{DWD}	WRITE command to input data delay		0	0	cycle
t_{DAL}	Data-in to ACTIVE command		5	4	cycle
t_{DPL}	Data-in to PRECHARGE command		2	2	cycle
t_{BDL}	Last data-in to burst STOP command		1	1	cycle
t_{CDL}	Last data-in to new READ/WRITE command		1	1	cycle
t_{RDL}	Last data-in to PRECHARGE command		2	2	cycle
t_{MRD}	LOAD MODE REGISTER command to ACTIVE or REFRESH command		2	2	cycle
t_{ROH}	Data-out to high-impedance from PRECHARGE command	CL = 3 CL = 2	3 2	3 2	cycle

AC TEST CONDITIONS

Input Load



Output Load



AC TEST CONDITIONS

Parameter	Unit
AC High Level Input Voltage/Low Level Input Voltage	1.6V to 0.2V
Input Rise and Fall Times	1 ns
Input Timing Reference Level	0.9V
Output Timing Measurement Reference Level	0.9V

FUNCTIONAL DESCRIPTION

The 128Mb SDRAMs are quad-bank DRAMs which operate at 2.5V or 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 16,777,216-bit banks is organized as 4,096 rows by 256 columns by 16 bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 and BA1 select the bank, A0-A11 select the row). The address bits (A0-A7) registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

Initialization

SDRAMs must be powered up and initialized in a predefined manner.

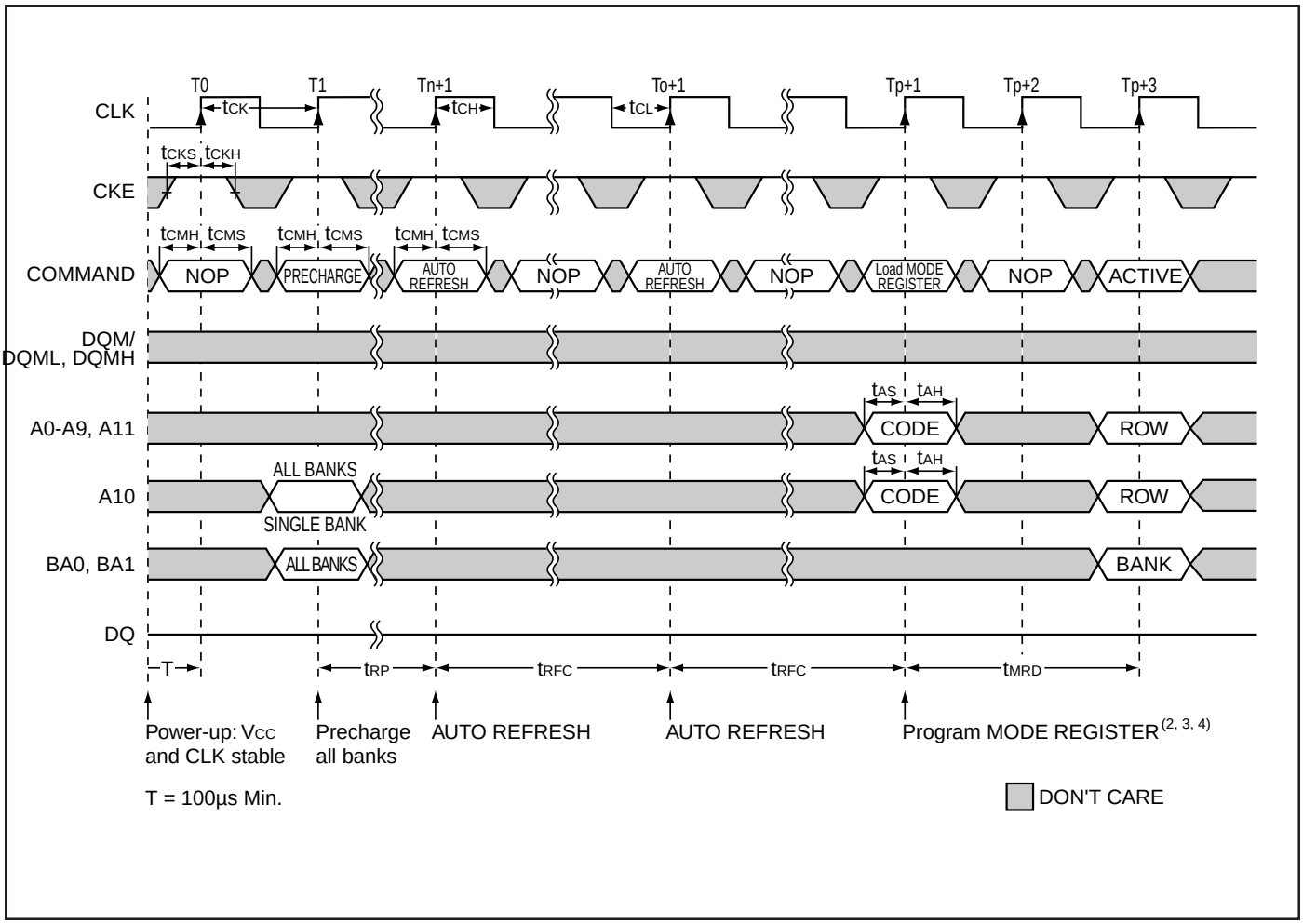
The 128M SDRAM is initialized after the power is applied to V_{DD} and Vddq (simultaneously) and the clock is stable.

A 200µs delay is required prior to issuing any command other than a COMMAND INHIBIT or a NOP. The COMMAND INHIBIT or NOP may be applied during the 100us period and should continue at least through the end of the period.

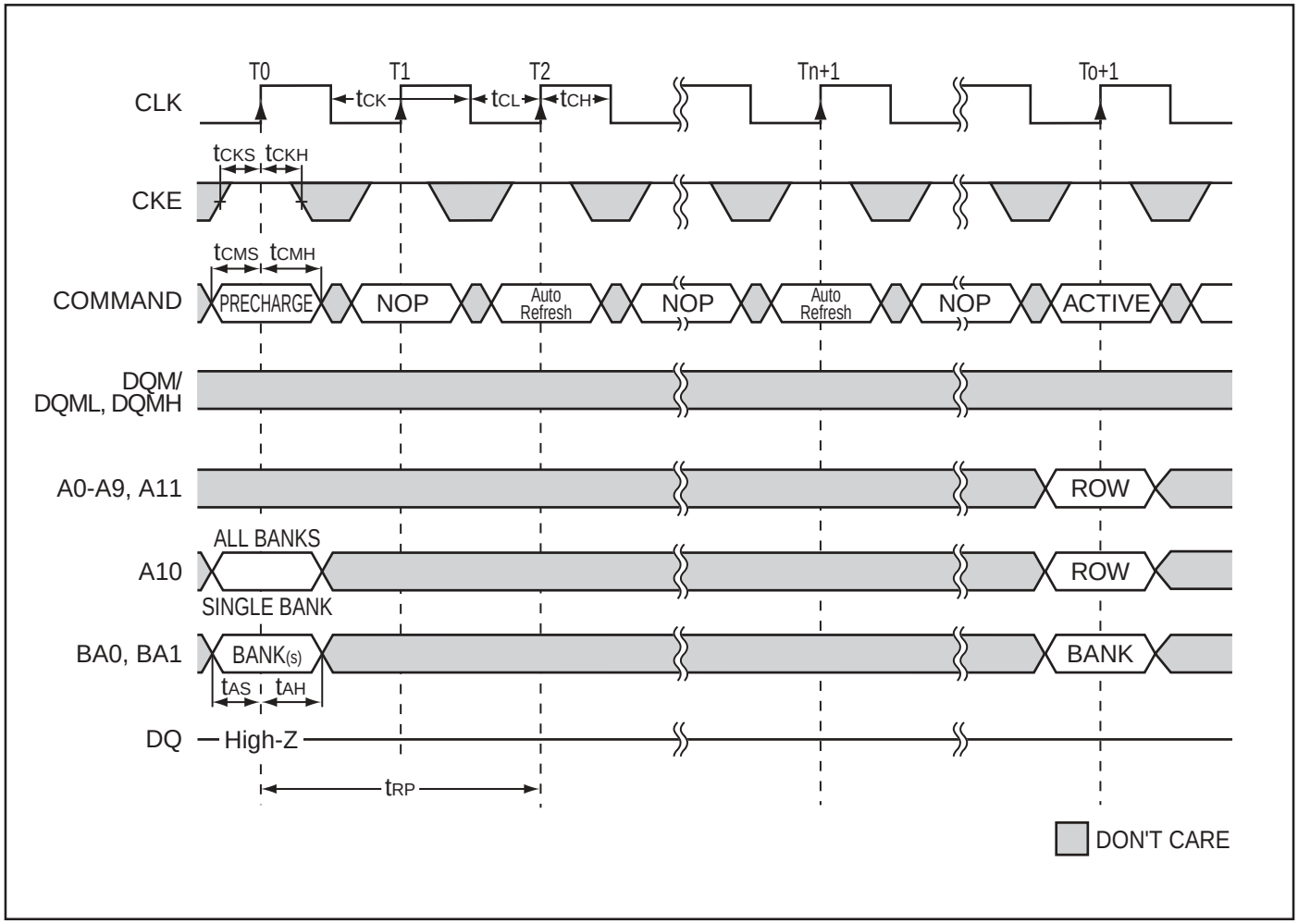
With at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied once the 100µs delay has been satisfied. All banks must be precharged. This will leave all banks in an idle state where two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SRDRAM is then ready for mode register programming.

The mode register and extended mode registers should be loaded prior to applying any operational command because it will power up in an unknown state.

INITIALIZE AND LOAD MODE REGISTER

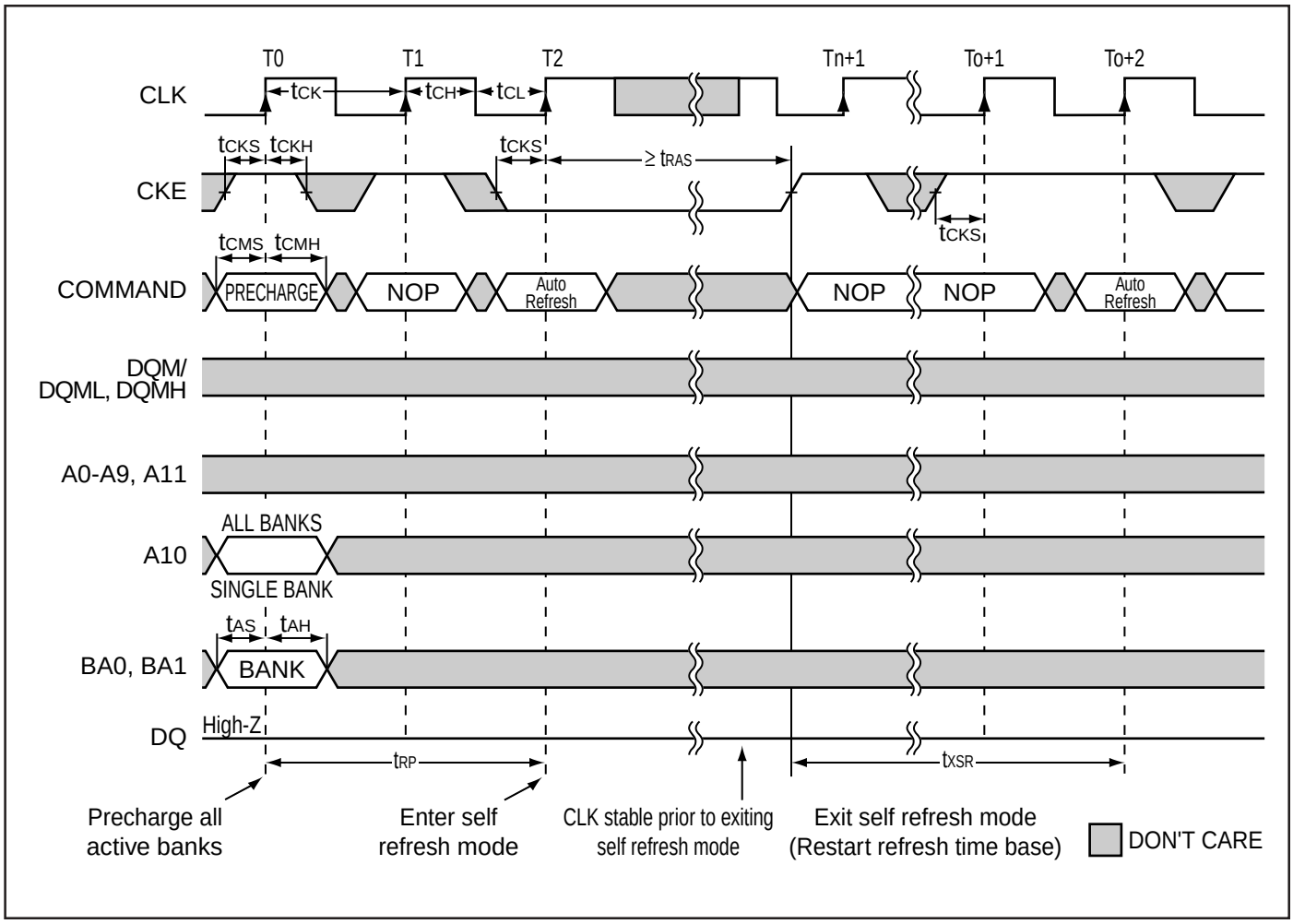


AUTO-REFRESH CYCLE



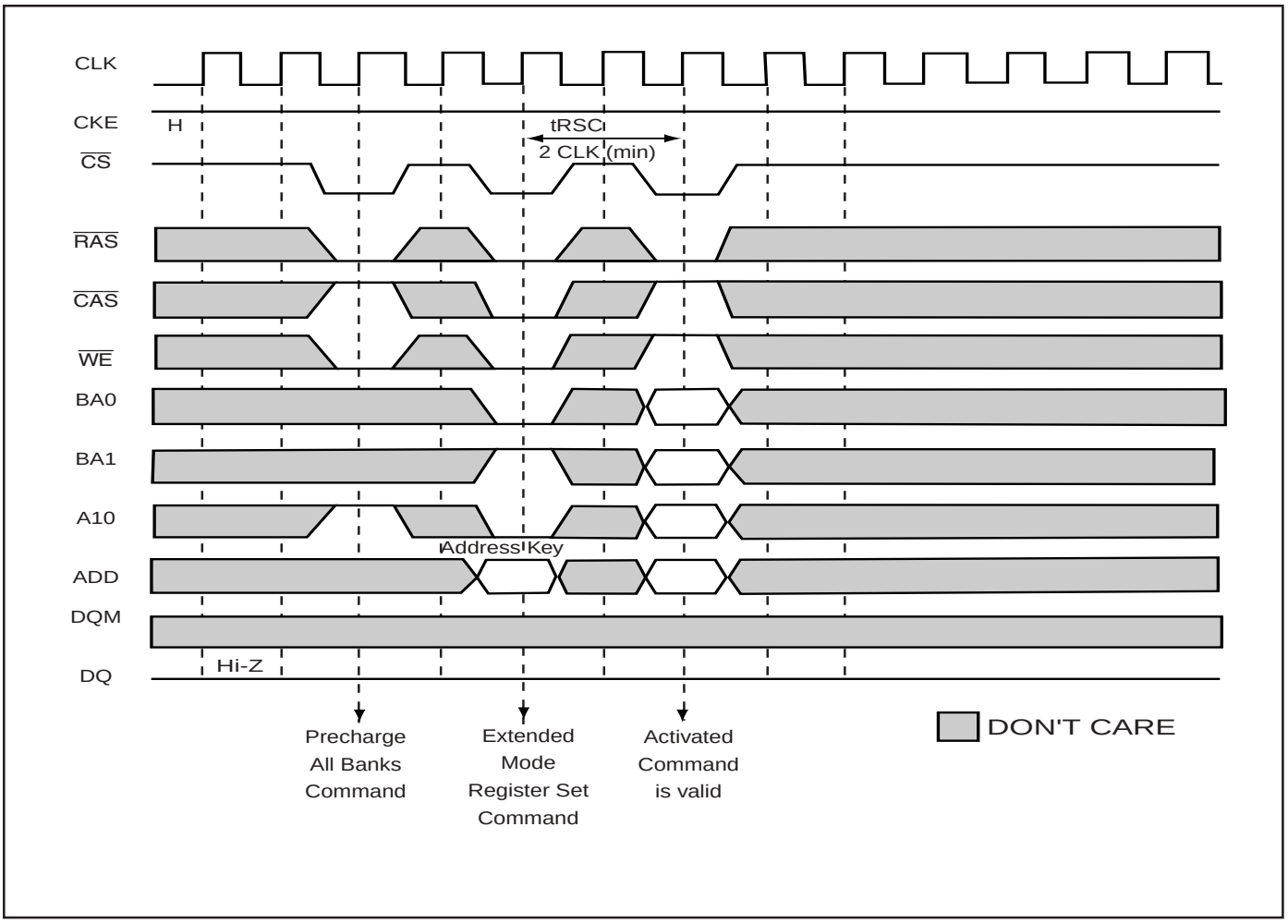
$\overline{\text{CAS}}$ latency = 2, 3

SELF-REFRESH CYCLE



$\overline{CAS}$ latency = 2, 3

EXTENDED MODE REGISTER SET



REGISTER DEFINITION

Mode Register

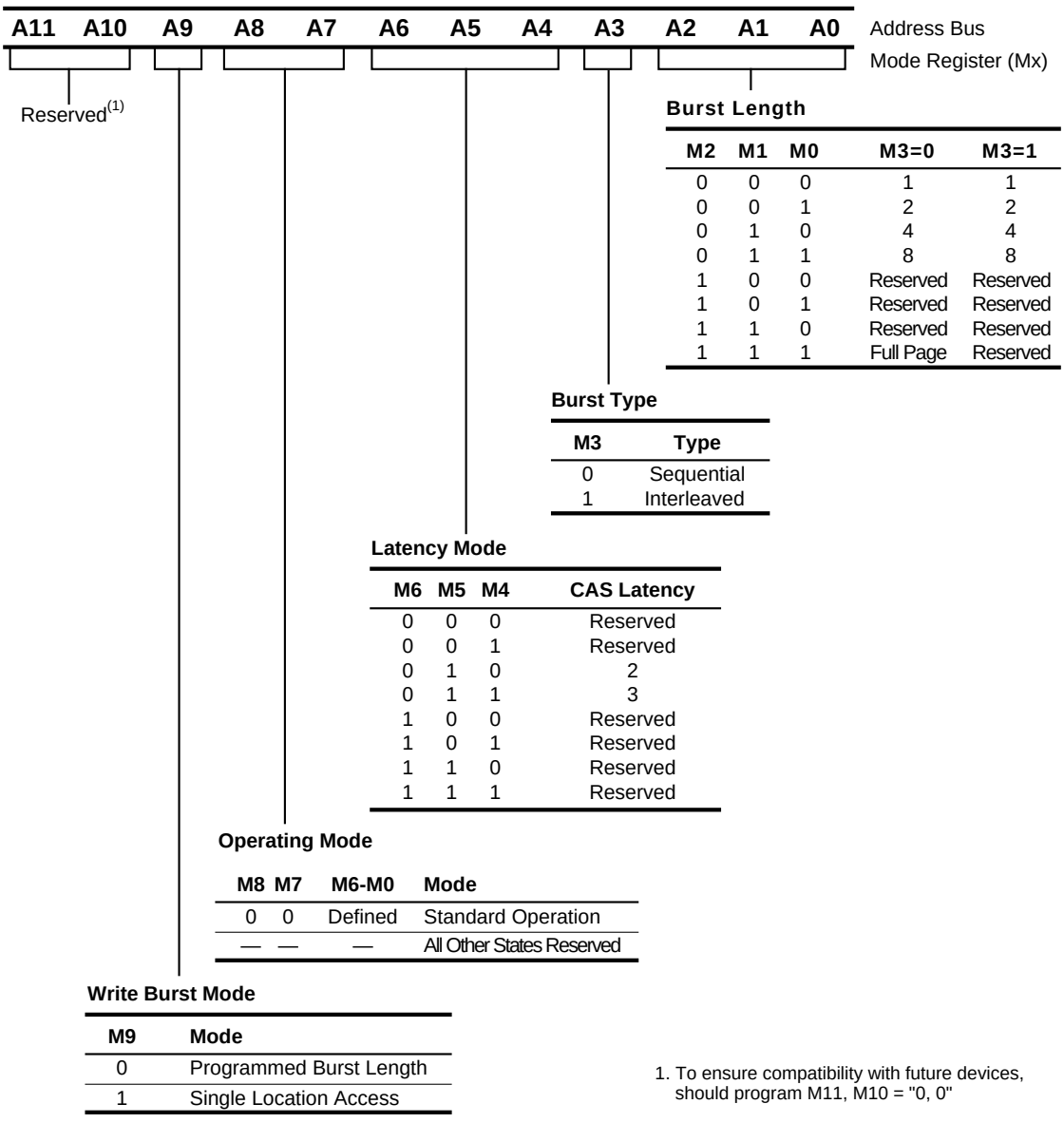
The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS\ latency, an operating mode and a write burst mode, as shown in MODE REGISTER DEFINITION.

The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0-M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4- M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the WRITE burst mode, and M10 and M11 are reserved for future use.

The mode register must be loaded when all banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

MODE REGISTER DEFINITION



Burst Length

M2	M1	M0	M3=0	M3=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Burst Type

M3	Type
0	Sequential
1	Interleaved

Latency Mode

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Operating Mode

M8	M7	M6-M0	Mode
0	0	Defined	Standard Operation
—	—	—	All Other States Reserved

Write Burst Mode

M9	Mode
0	Programmed Burst Length
1	Single Location Access

1. To ensure compatibility with future devices, should program M11, M10 = "0, 0"

BURST LENGTH

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in MODE REGISTER DEFINITION. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4 or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A1-A7 (x16) when the burst length is set to two; by A2-A7 (x16) when the burst length is set to four; and by A3-A7 (x16) when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached.

Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in BURST DEFINITION table.

BURST DEFINITION

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
				Type = Sequential	Type = Interleaved
			A0		
2			0	0-1	0-1
			1	1-0	1-0
		A1	A0		
		0	0	0-1-2-3	0-1-2-3
4		0	1	1-2-3-0	1-0-3-2
		1	0	2-3-0-1	2-3-0-1
		1	1	3-0-1-2	3-2-1-0
	A2	A1	A0		
	0	0	0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0	0	1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0	1	0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
8	0	1	1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1	0	0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1	0	1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1	1	0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1	1	1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A7 (location 0-y)			Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

CAS Latency

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge n, and the latency is *m* clocks, the data will be available by clock edge *n* + m. The DQs will start driving as a result of the clock edge one cycle earlier (*n* + *m* - 1), and provided that the relevant access times are met, the data will be valid by clock edge *n* + m. For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at T0 and the latency is programmed to two clocks, the DQs will start driving after T1 and the data will be valid by T2, as shown in CAS Latency diagrams. The Allowable Operating Frequency table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

Operating Mode

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

Write Burst Mode

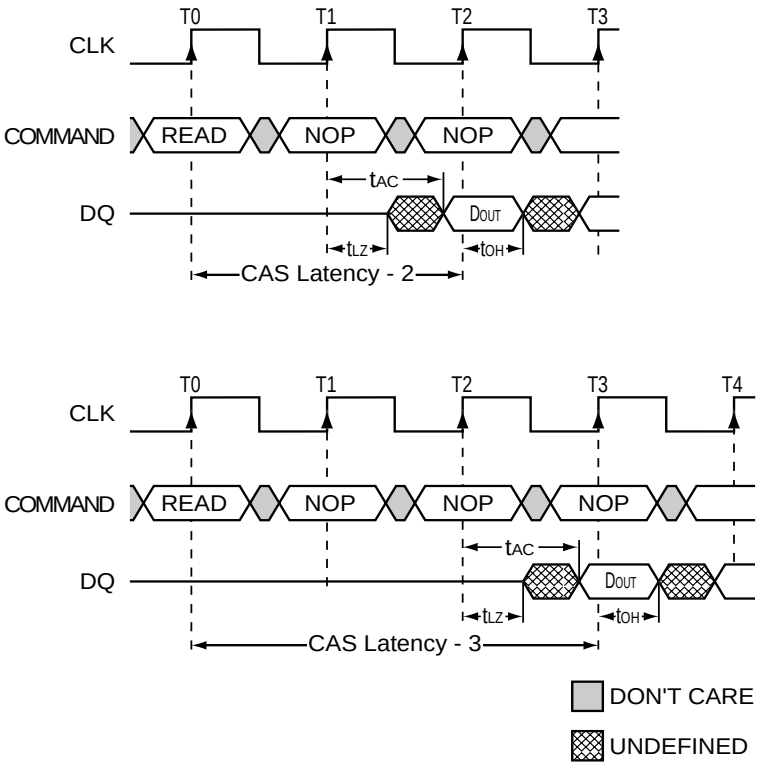
When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

CAS Latency

Allowable Operating Frequency (MHz)

Speed	CAS Latency = 2	CAS Latency = 3
7.5	100	133
10	75	100

CAS LATENCY



CHIP OPERATION

BANK/ROW ACTIVATION

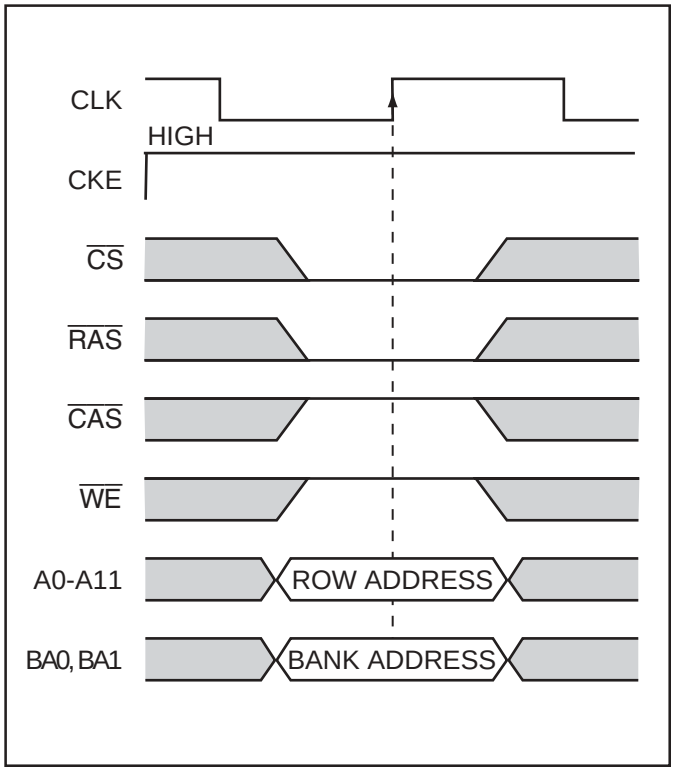
Before any READ or WRITE commands can be issued to a bank within the SDRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated (see Activating Specific Row Within Specific Bank).

After opening a row (issuing an ACTIVE command), a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. Minimum t_{RCD} should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command on which a READ or WRITE command can be entered. For example, a t_{RCD} specification of 20ns with a 125 MHz clock (8ns period) results in 2.5 clocks, rounded to 3. This is reflected in the following example, which covers any case where $2 < [t_{RCD} (MIN)/t_{CK}] \leq 3$. (The same procedure is used to convert other specification limits from time units to clock cycles).

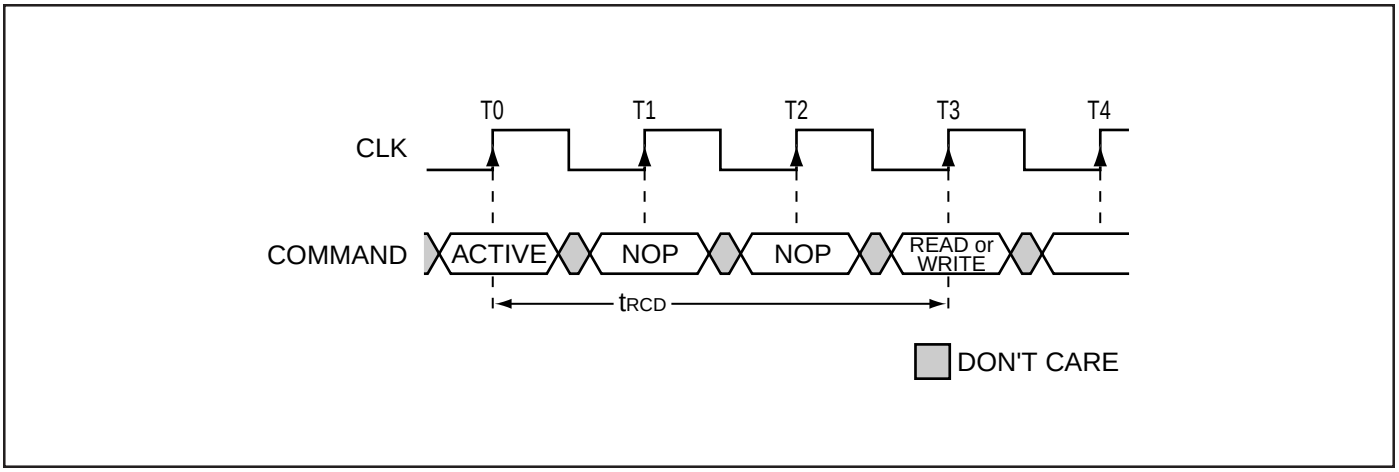
A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed" (precharged). The minimum time interval between successive ACTIVE commands to the same bank is defined by t_{RC}.

A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row-access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.

ACTIVATING SPECIFIC ROW WITHIN SPECIFIC BANK



EXAMPLE: MEETING TRCD (MIN) WHEN 2 < [TRCD (MIN)/TCK] ≤ 3



READS

READ bursts are initiated with a READ command, as shown in the READ COMMAND diagram.

The starting column and bank addresses are provided with the READ command, and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic READ commands used in the following illustrations, auto precharge is disabled.

During READ bursts, the valid data-out element from the starting column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid by the next positive clock edge. The CAS Latency diagram shows general timing for each possible CAS latency setting.

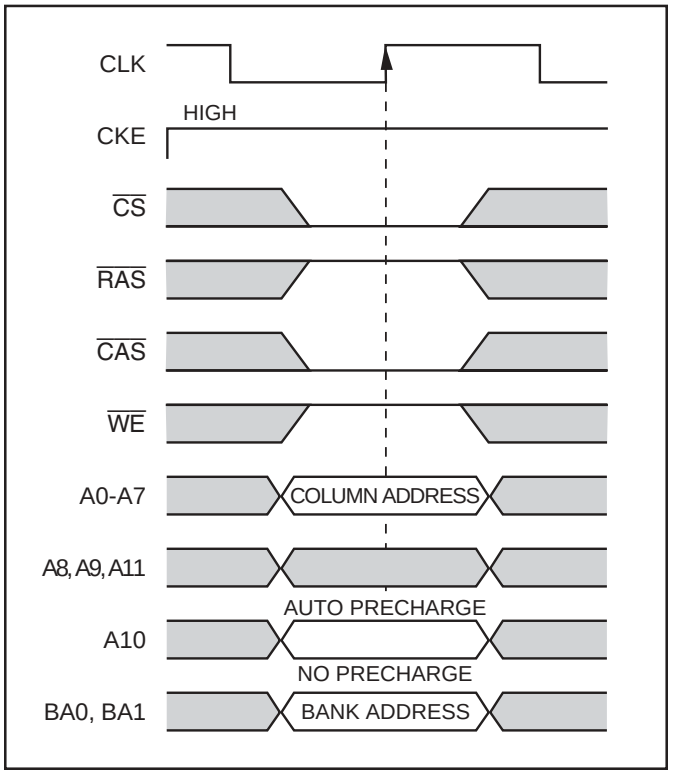
Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data from any READ burst may be truncated with a subsequent READ command, and data from a fixed-length READ burst may be immediately followed by data from a READ command. In either case, a continuous flow of data can be maintained. The first data element from the new burst follows either the last element of a completed burst or the last desired data element of a longer burst which is being truncated.

The new READ command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in Consecutive READ Bursts for CAS latencies of two and three; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. The 64Mb SDRAM uses a pipelined architecture and therefore does not require the *2n* rule associated with a prefetch architecture. A READ command can be initiated on any clock cycle following a previous READ command. Full-speed random read accesses can be performed to the same bank, as shown in Random READ Accesses, or each subsequent READ may be performed to a different bank.

Data from any READ burst may be truncated with a subsequent WRITE command, and data from a fixed-length READ burst may be immediately followed by data from a WRITE command (subject to bus turnaround limitations). The WRITE burst may be initiated on the clock edge immediately following the last (or last desired) data element from the READ burst, provided that I/O contention can be avoided. In a given system design, there may be a possibility that the device driving the input data will go Low-Z before the SDRAM DQs go High-Z. In this case, at least a single-cycle delay should occur between the last read data and the WRITE command.

READ COMMAND



The DQM input is used to avoid I/O contention, as shown in Figures RW1 and RW2. The DQM signal must be asserted (HIGH) at least two clocks prior to the WRITE command (DQM latency is two clocks for output buffers) to suppress data-out from the READ. Once the WRITE command is registered, the DQs will go High-Z (or remain High-Z), regardless of the state of the DQM signal, provided the DQM was active on the clock just prior to the WRITE command that truncated the READ command. If not, the second WRITE will be an invalid WRITE. For example, if DQM was LOW during T4 in Figure RW2, then the WRITEs at T5 and T7 would be valid, while the WRITE at T6 would be invalid.

The DQM signal must be de-asserted prior to the WRITE command (DQM latency is zero clocks for input buffers) to ensure that the written data is not masked. Figure RW1 shows the case where the clock frequency allows for bus contention to be avoided without adding a NOP cycle, and Figure RW2 shows the case where the additional NOP is needed.

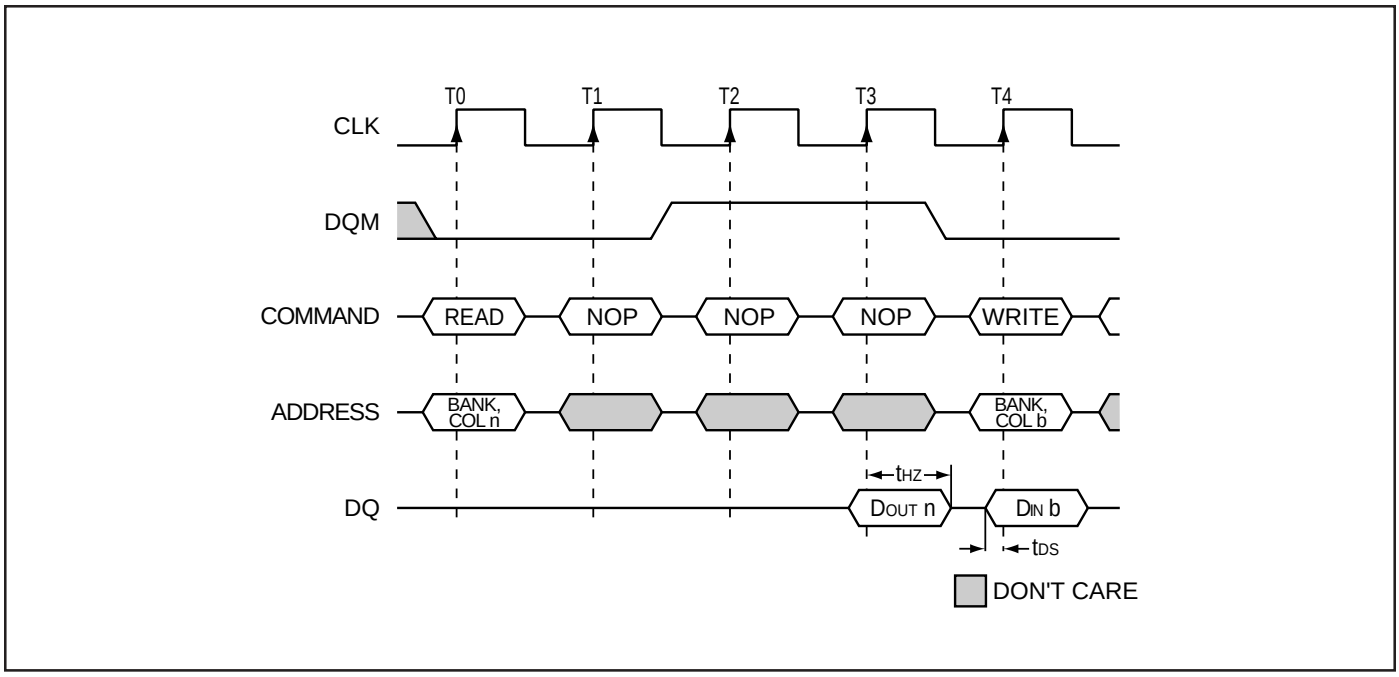
A fixed-length READ burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page burst may be truncated with a PRECHARGE command to the

same bank. The PRECHARGE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in the READ to PRECHARGE diagram for each possible CAS latency; data element *n* + 3 is either the last of a burst of four or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met. Note that part of the row precharge time is hidden during the access of the last data element(s).

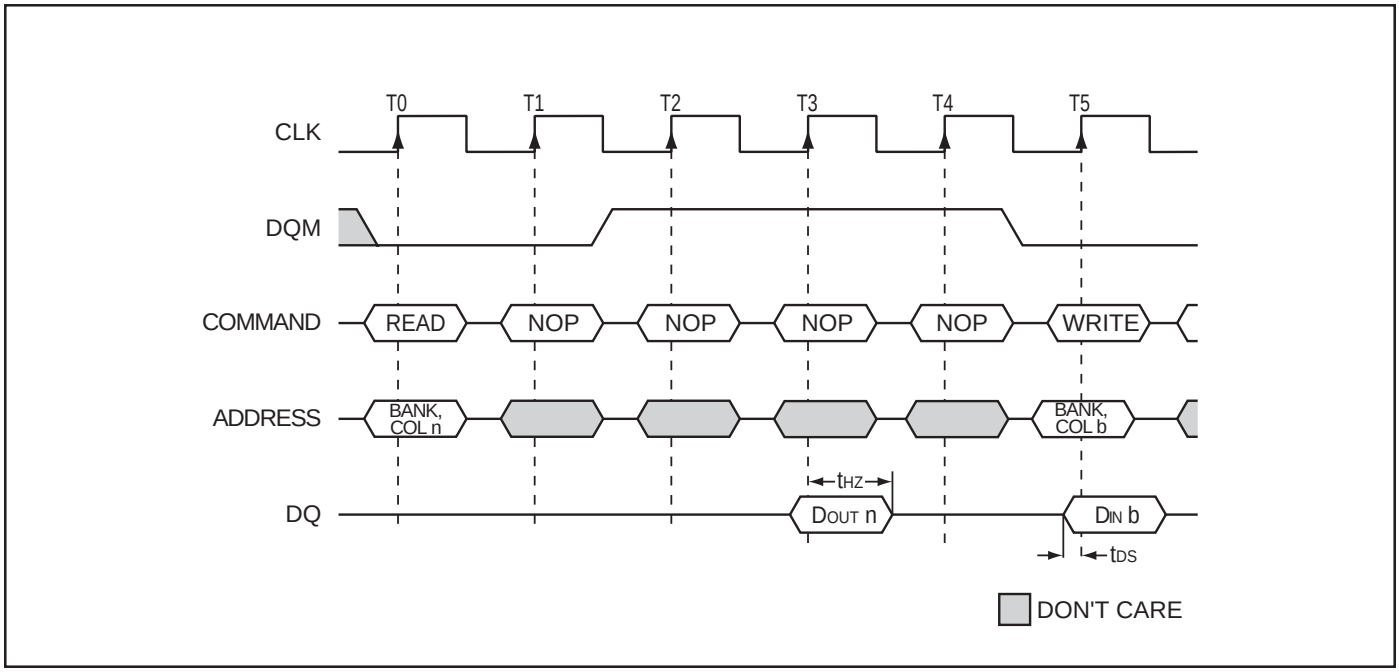
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

Full-page READ bursts can be truncated with the BURST TERMINATE command, and fixed-length READ bursts may be truncated with a BURST TERMINATE command, provided that auto precharge was not activated. The BURST TERMINATE command should be issued *x* cycles before the clock edge at which the last desired data element is valid, where *x* equals the CAS latency minus one. This is shown in the READ Burst Termination diagram for each possible CAS latency; data element *n* + 3 is the last desired data element of a longer burst.

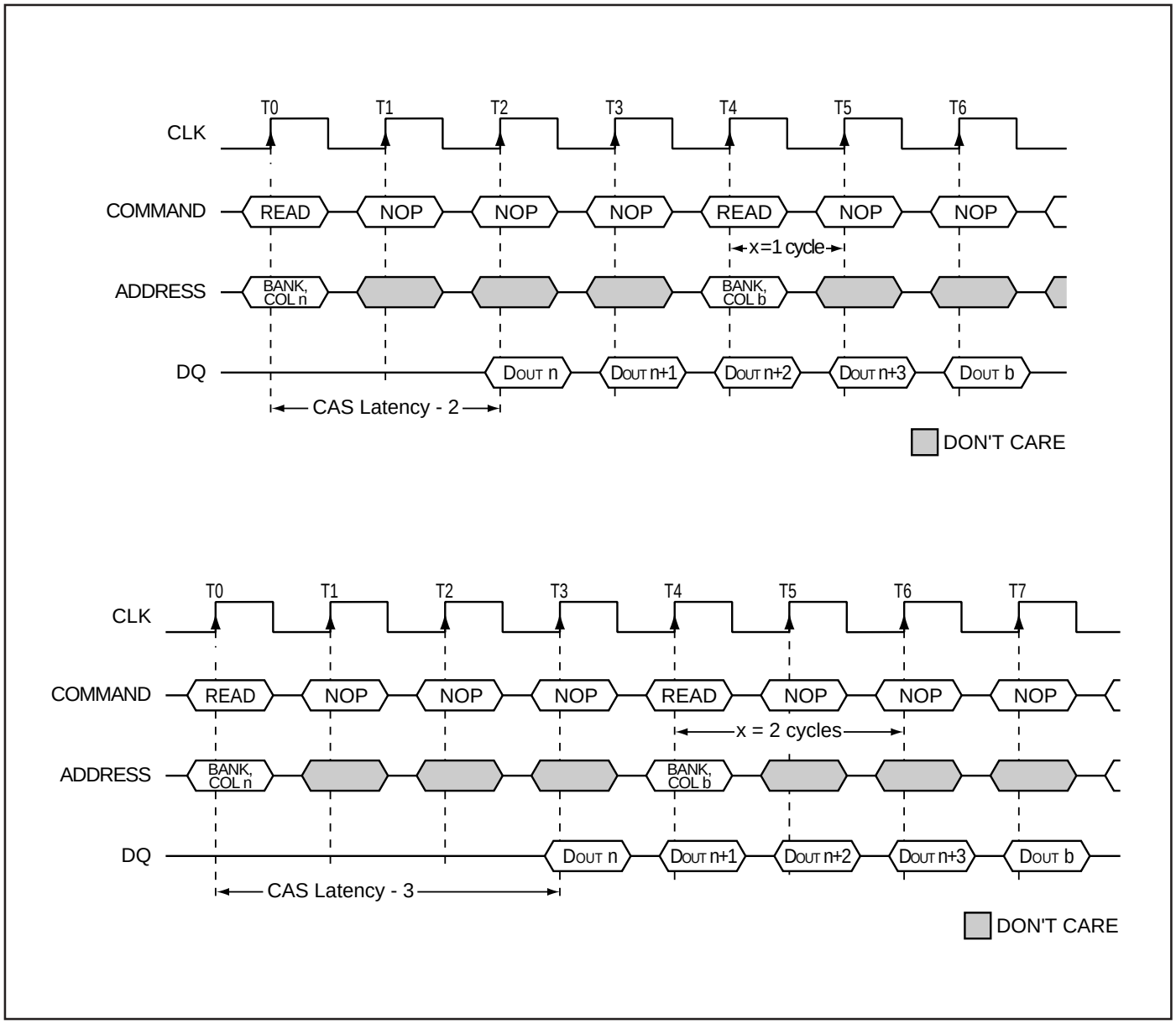
RW1 - READ TO WRITE



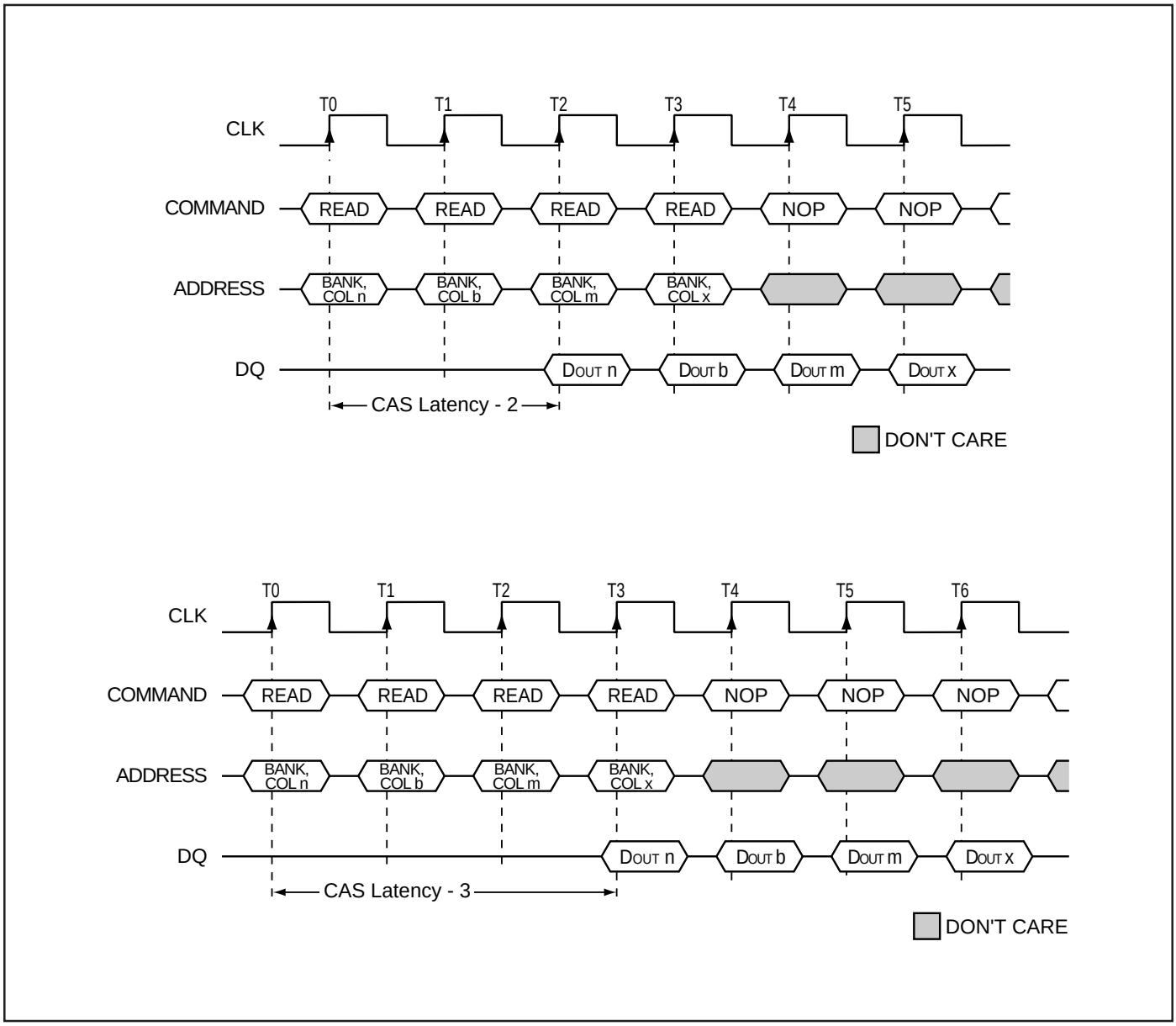
RW2 - READ TO WRITE WITH EXTRA CLOCK CYCLE



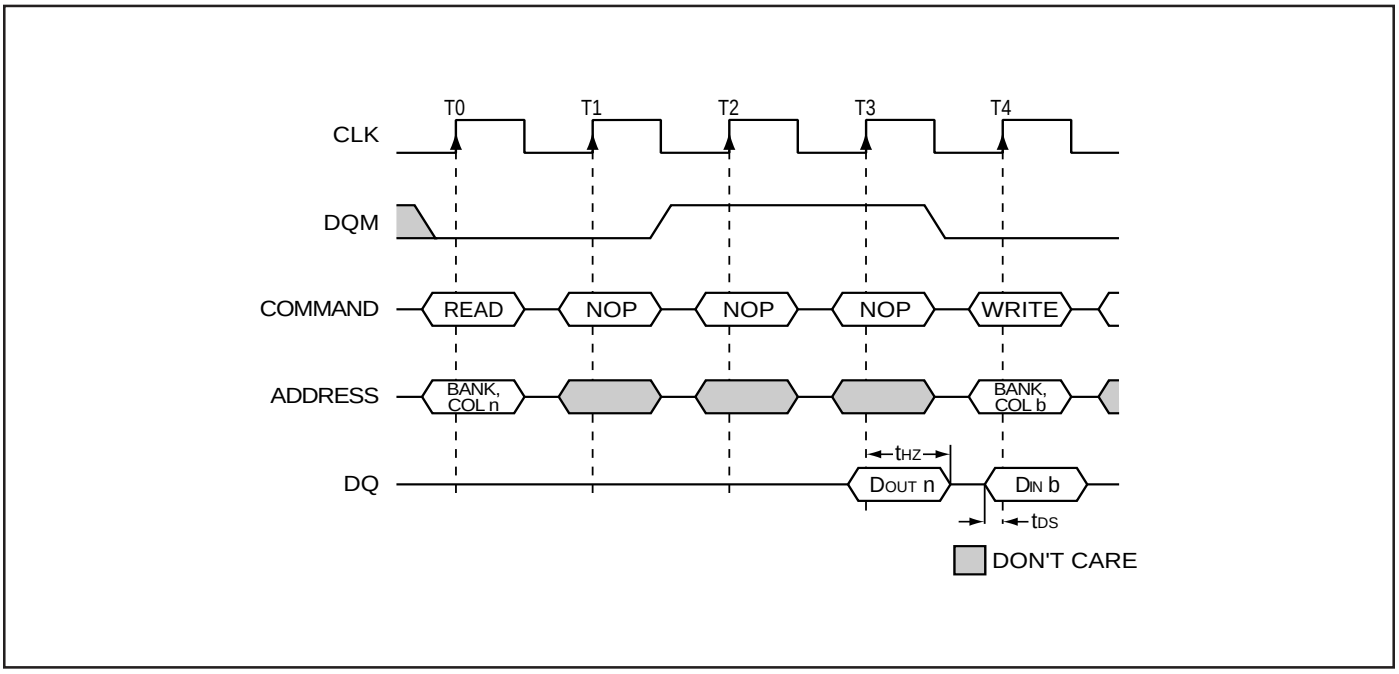
CONSECUTIVE READ BURSTS



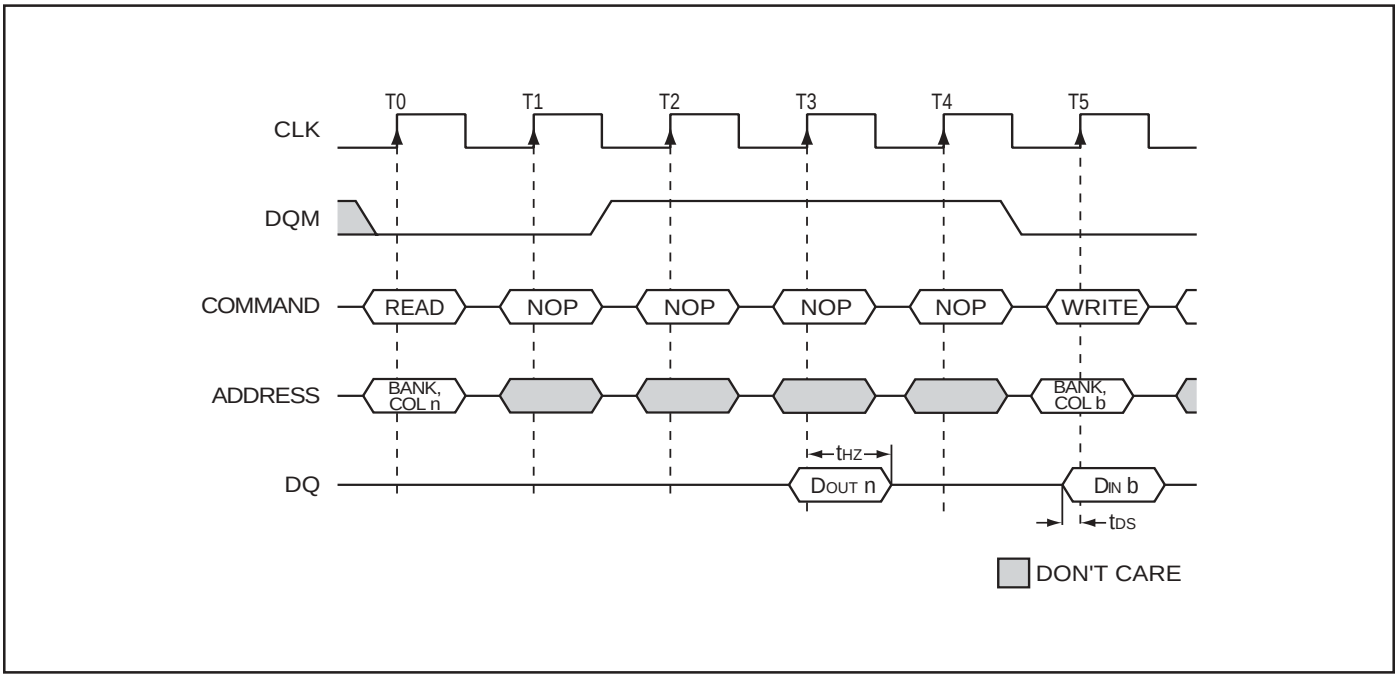
RANDOM READ ACCESSES



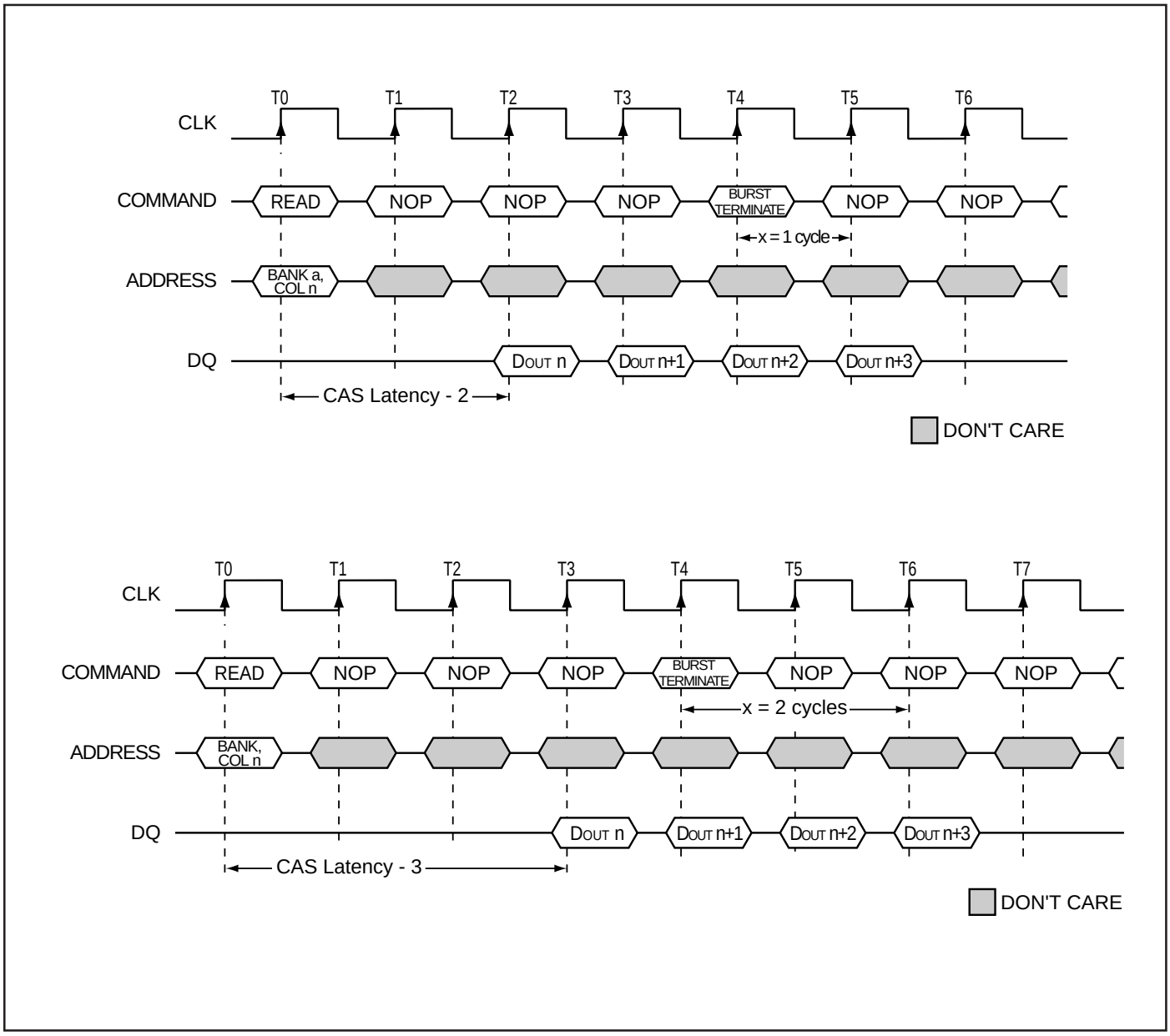
RW1 - READ TO WRITE



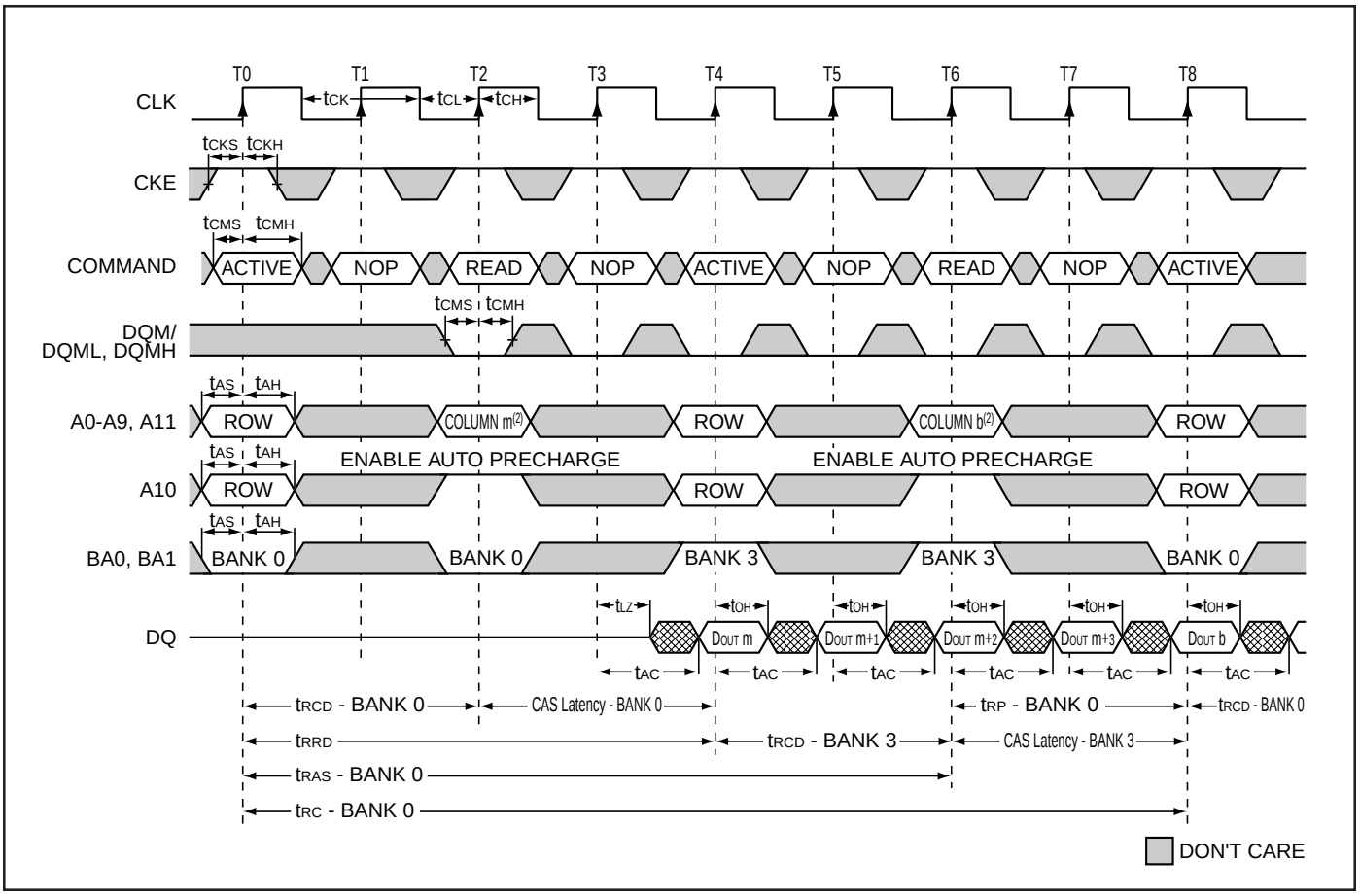
RW2 - READ TO WRITE WITH EXTRA CLOCK CYCLE



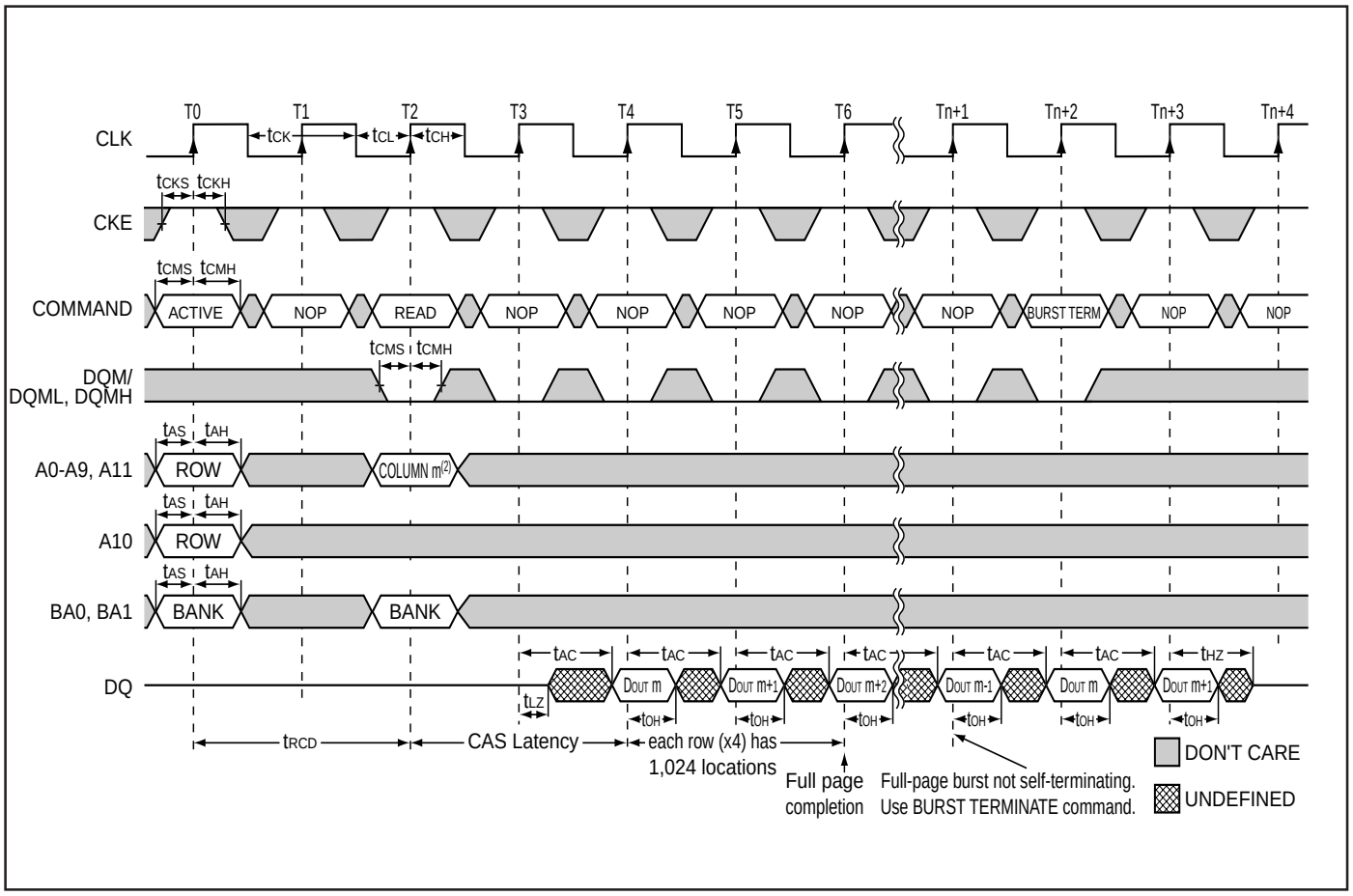
READ BURST TERMINATION



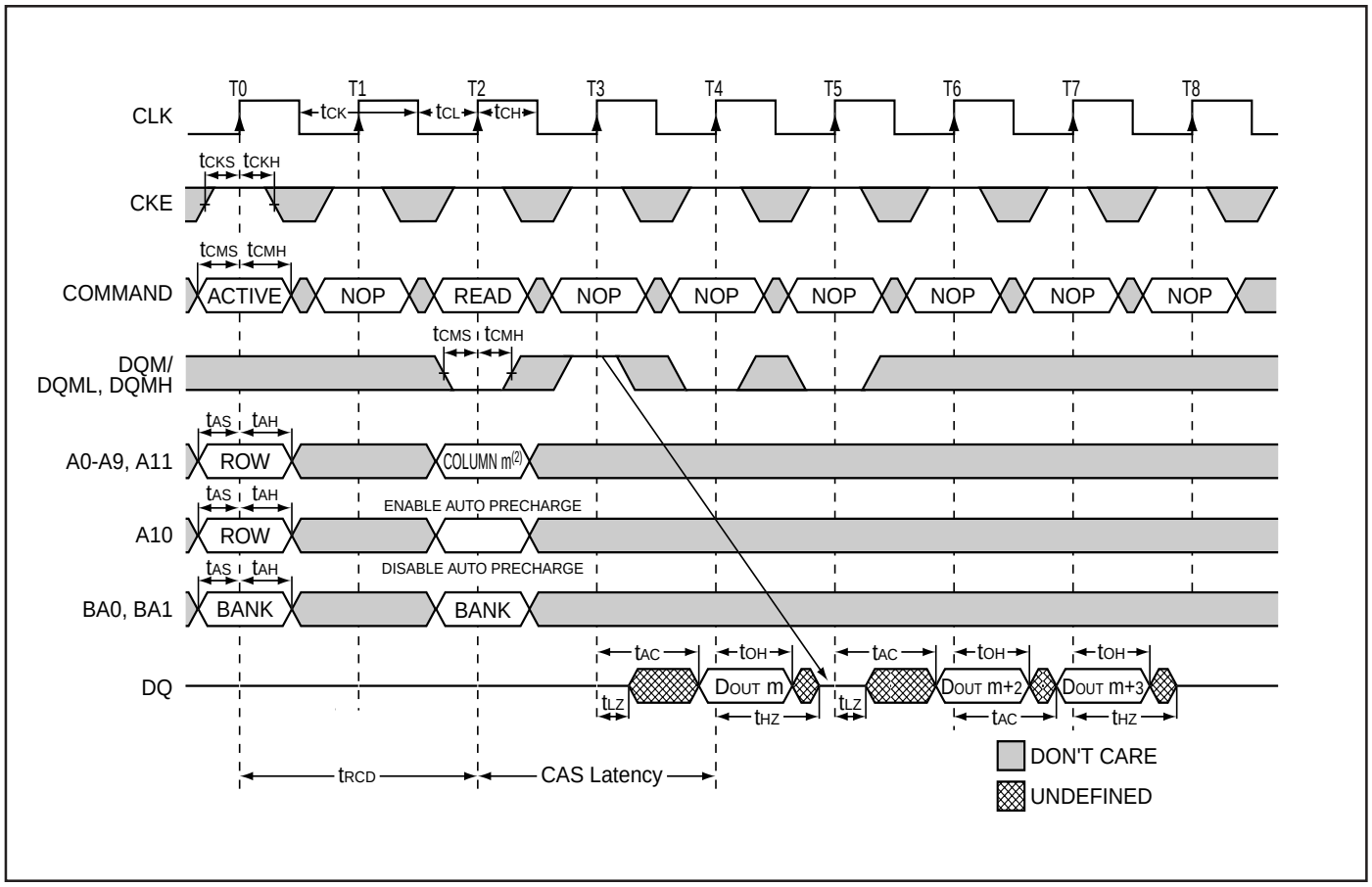
ALTERNATING BANK READ ACCESSES



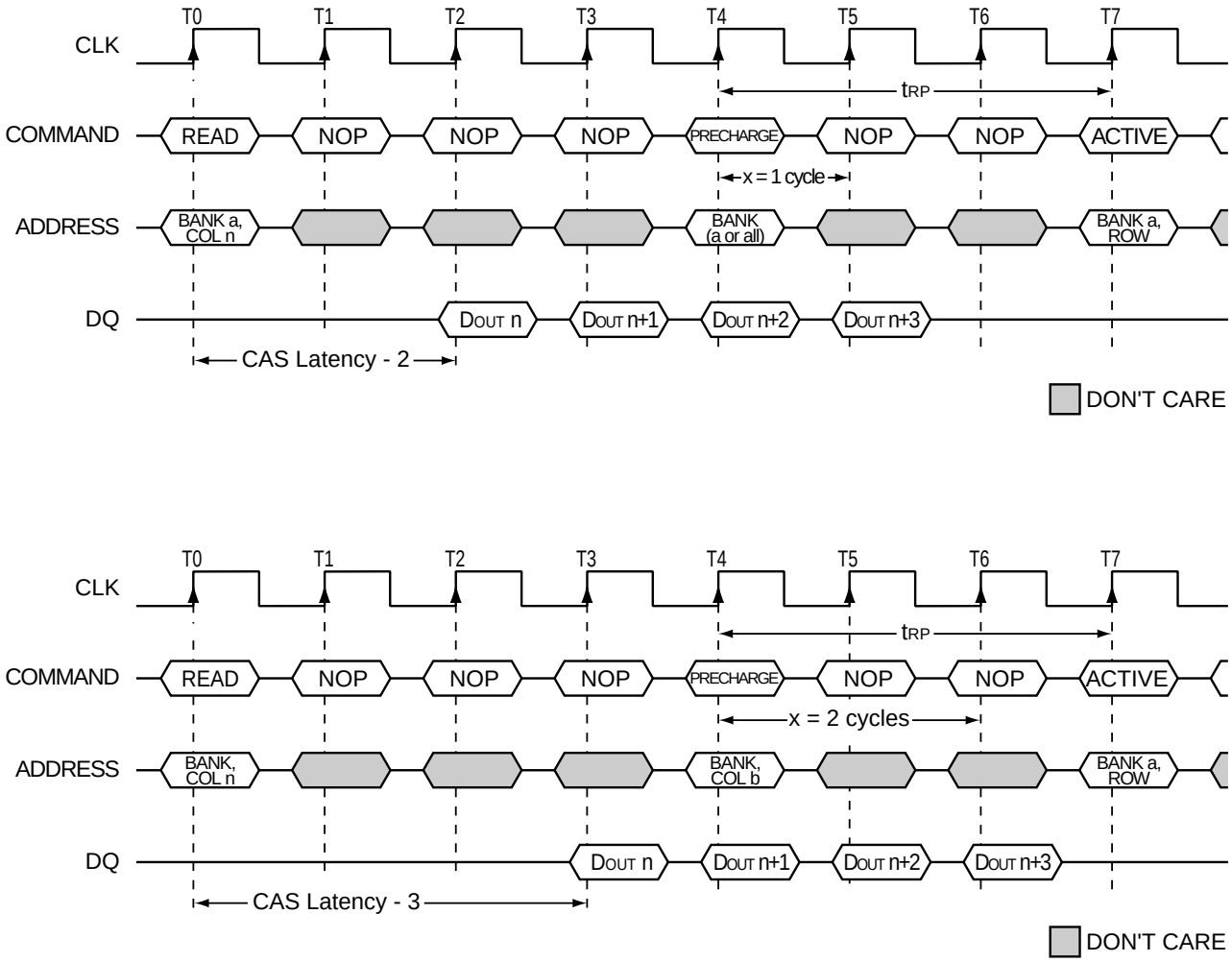
READ - FULL-PAGE BURST



READ - DQM OPERATION



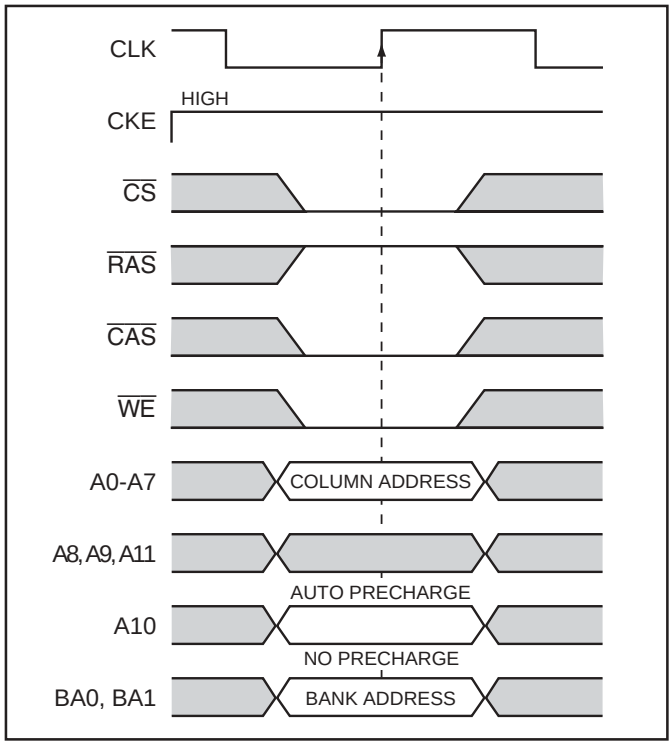
READ to PRECHARGE



WRITES

WRITE bursts are initiated with a WRITE command, as shown in WRITE Command diagram.

WRITE COMMAND



The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

During WRITE bursts, the first valid data-in element will be registered coincident with the WRITE command. Subsequent data elements will be registered on each successive positive clock edge. Upon completion of a fixed-length burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored (see WRITE Burst). A full-page burst will continue until terminated. (At the end of the page, it will wrap to column 0 and continue.)

Data for any WRITE burst may be truncated with a subsequent WRITE command, and data for a fixed-length WRITE burst may be immediately followed by data for a WRITE command. The new WRITE command can be issued on any clock following the previous WRITE command, and the data provided coincident with the new command applies to the new command.

An example is shown in WRITE to WRITE diagram. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst. The 128Mb SDRAM uses a pipelined architecture and therefore does not require the *2n* rule associated with a prefetch architecture. A WRITE command can be initiated on any clock cycle following a previous WRITE command. Full-speed random write accesses within a page can be performed to the same bank, as shown in Random WRITE Cycles, or each subsequent WRITE may be performed to a different bank.

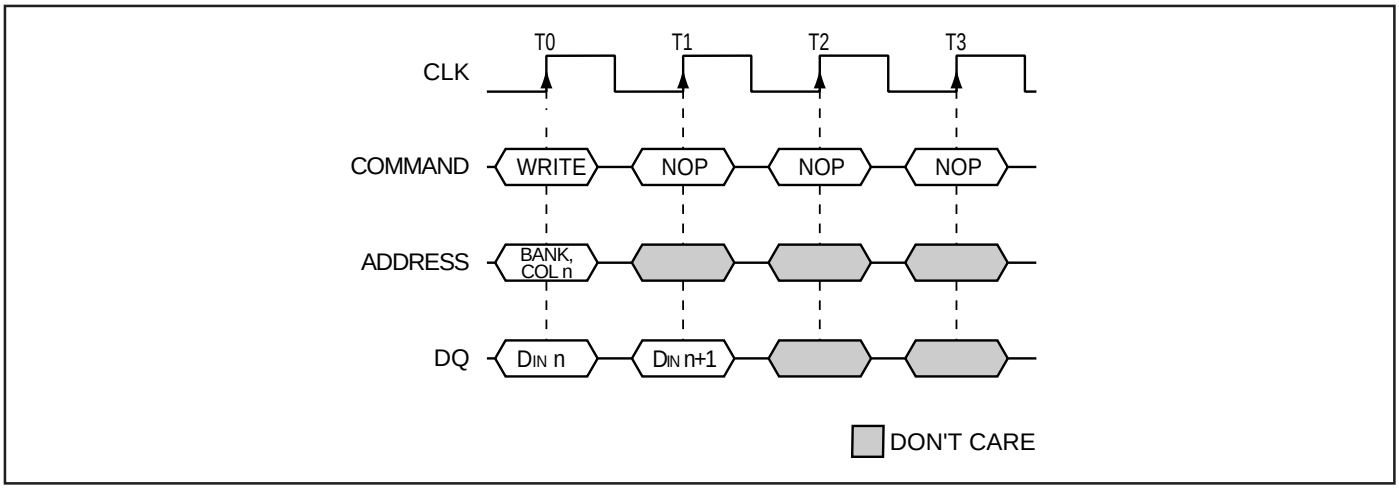
Data for any WRITE burst may be truncated with a subsequent READ command, and data for a fixed-length WRITE burst may be immediately followed by a subsequent READ command. Once the READ com mand is registered, the data inputs will be ignored, and WRITEs will not be executed. An example is shown in WRITE to READ. Data *n* + 1 is either the last of a burst of two or the last desired of a longer burst.

Data for a fixed-length WRITE burst may be followed by, or truncated with, a PRECHARGE command to the same bank (provided that auto precharge was not activated), and a full-page WRITE burst may be truncated with a PRECHARGE command to the same bank. The PRECHARGE command should be issued t_{WR} after the clock edge at which the last desired input data element is registered. The auto precharge mode requires a t_{WR} of at least one clock plus time, regardless of frequency. In addition, when truncating a WRITE burst, the DQM signal must be used to mask input data for the clock edge prior to, and the clock edge coincident with, the PRECHARGE command. An example is shown in the WRITE to PRECHARGE diagram. Data *n*+1 is either the last of a burst of two or the last desired of a longer burst. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until t_{RP} is met.

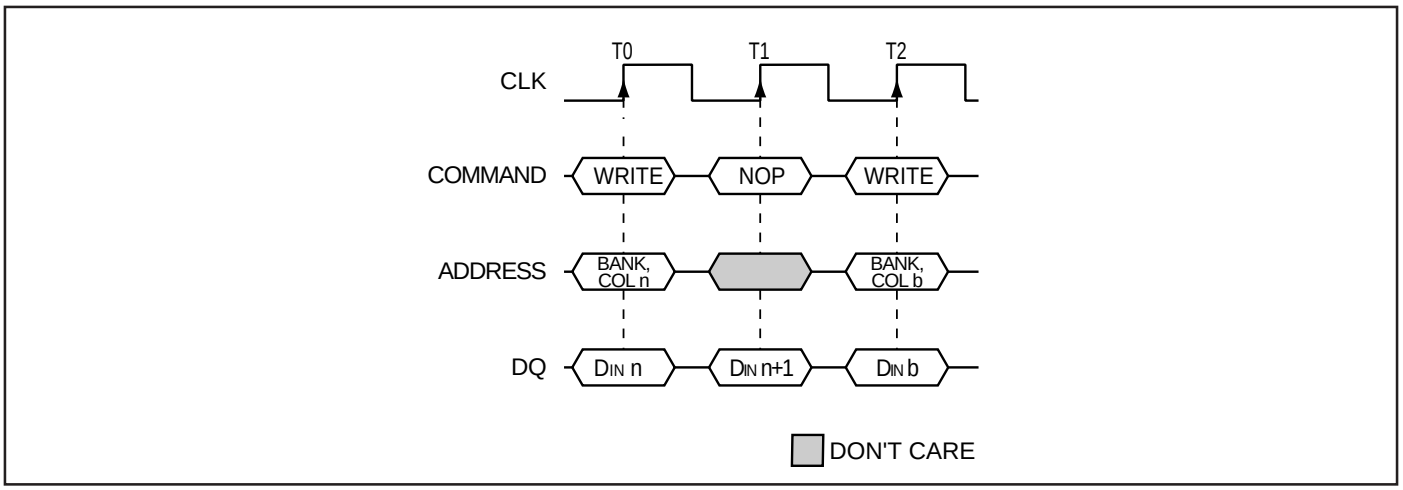
In the case of a fixed-length burst being executed to completion, a PRECHARGE command issued at the optimum time (as described above) provides the same operation that would result from the same fixed-length burst with auto precharge. The disadvantage of the PRECHARGE command is that it requires that the command and address buses be available at the appropriate time to issue the command; the advantage of the PRECHARGE command is that it can be used to truncate fixed-length or full-page bursts.

Fixed-length or full-page WRITE bursts can be truncated with the BURST TERMINATE command. When truncating a WRITE burst, the input data applied coincident with the BURST TERMINATE command will be ignored. The last data written (provided that DQM is LOW at that time) will be the input data applied one clock previous to the BURST TERMINATE command. This is shown in WRITE Burst Termination, where data *n* is the last desired data element of a longer burst.

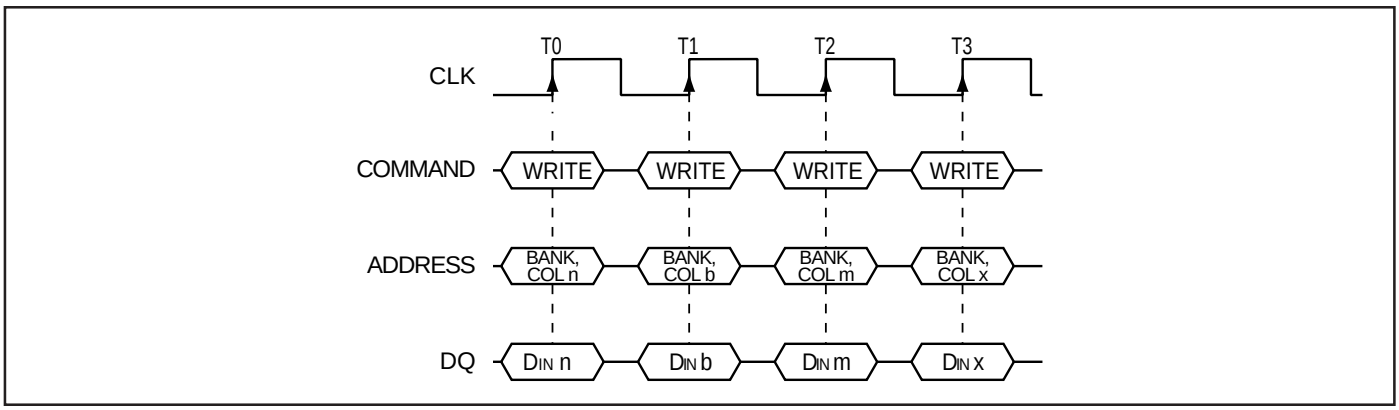
WRITE BURST



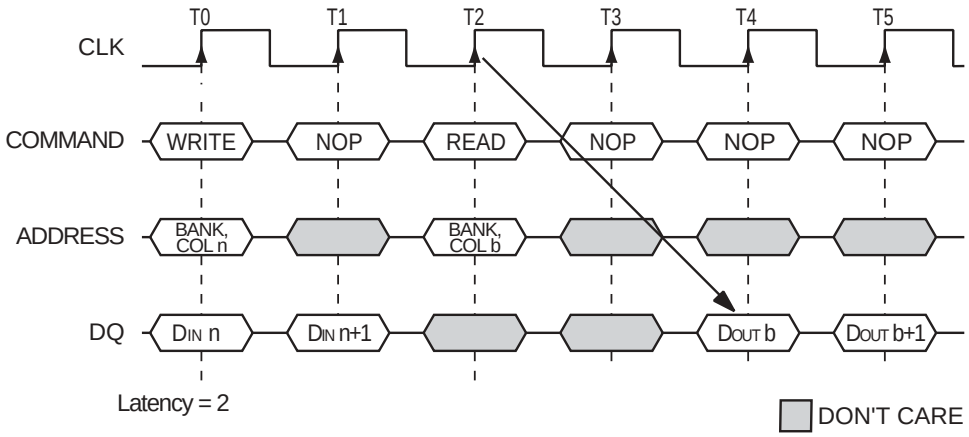
WRITE TO WRITE



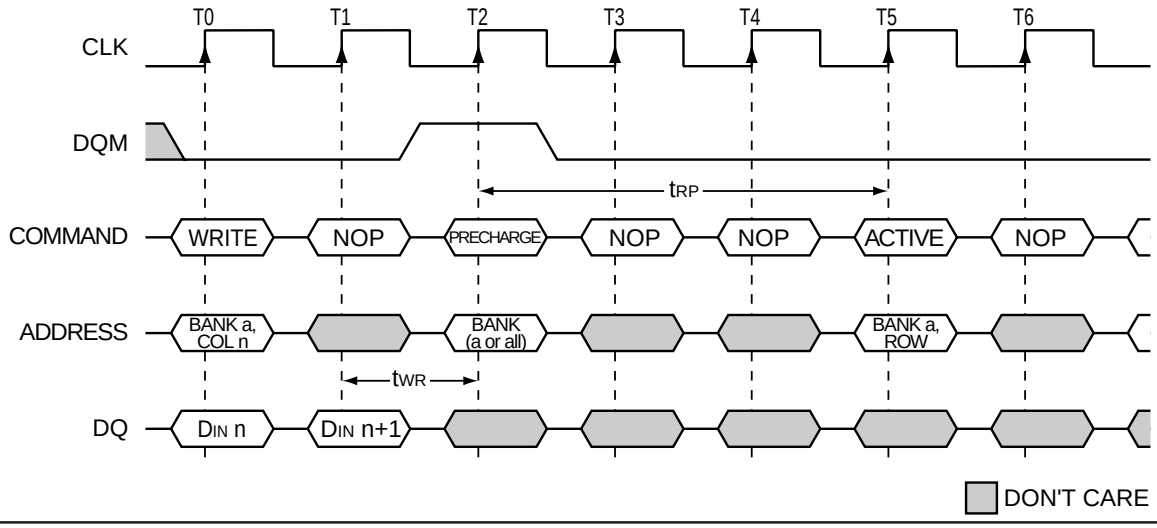
RANDOM WRITE CYCLES



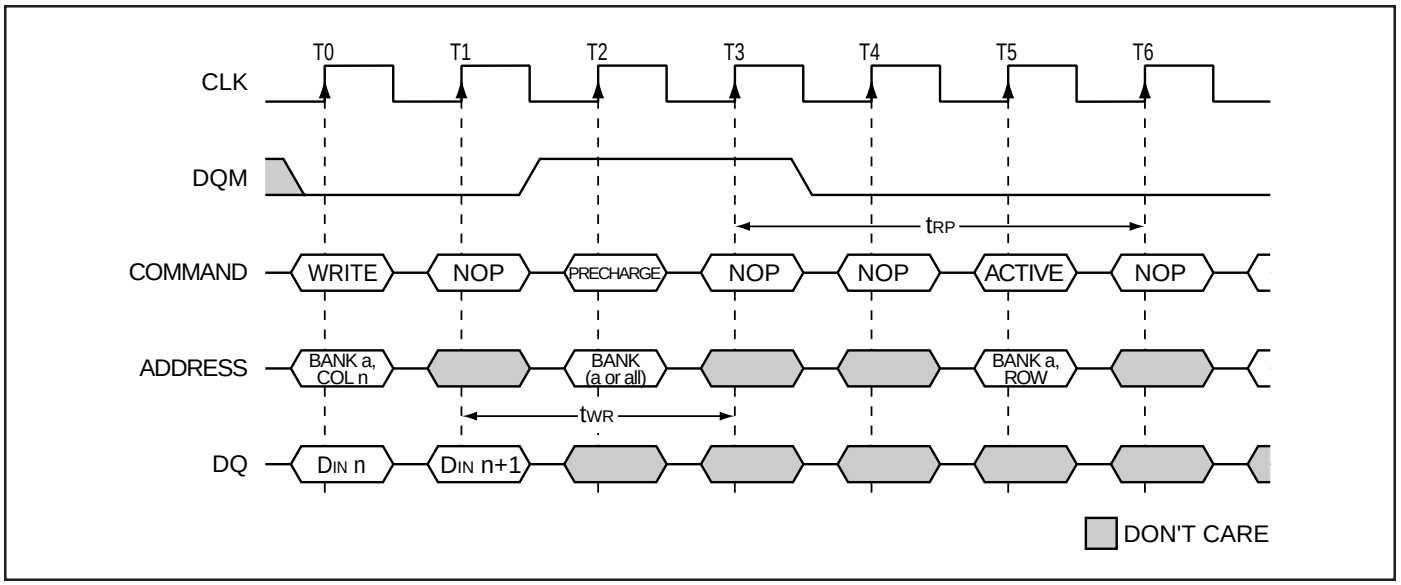
WRITE TO READ



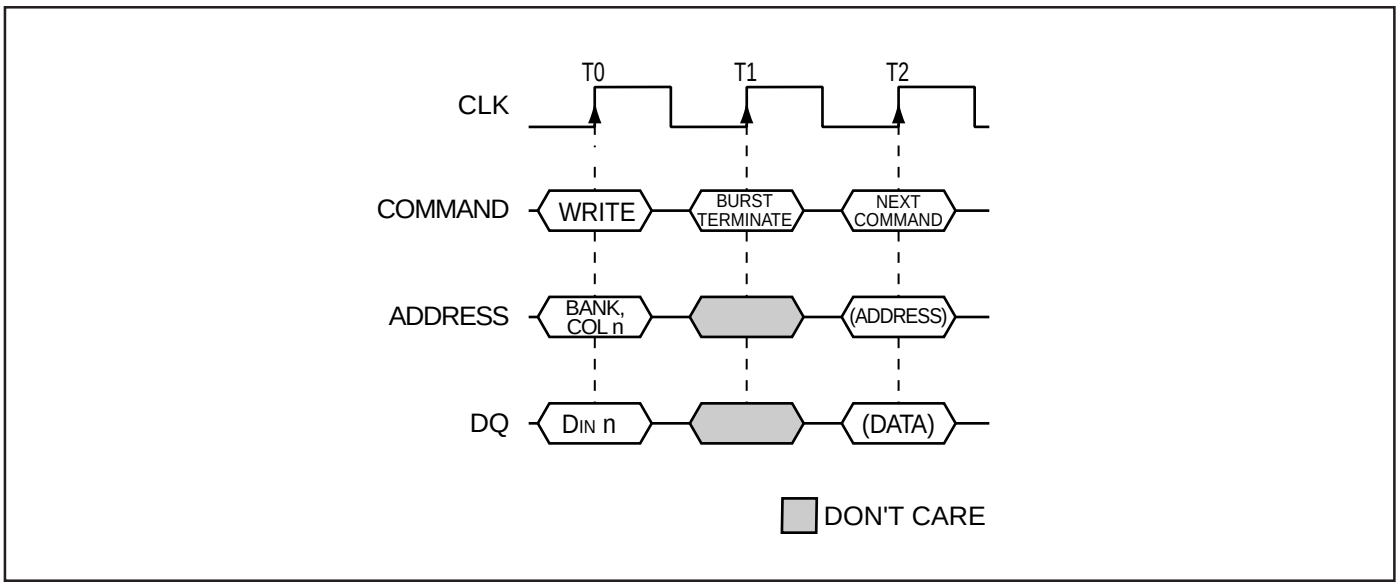
WRITE TO PRECHARGE (TWR @ TCK ≥ 15NS)



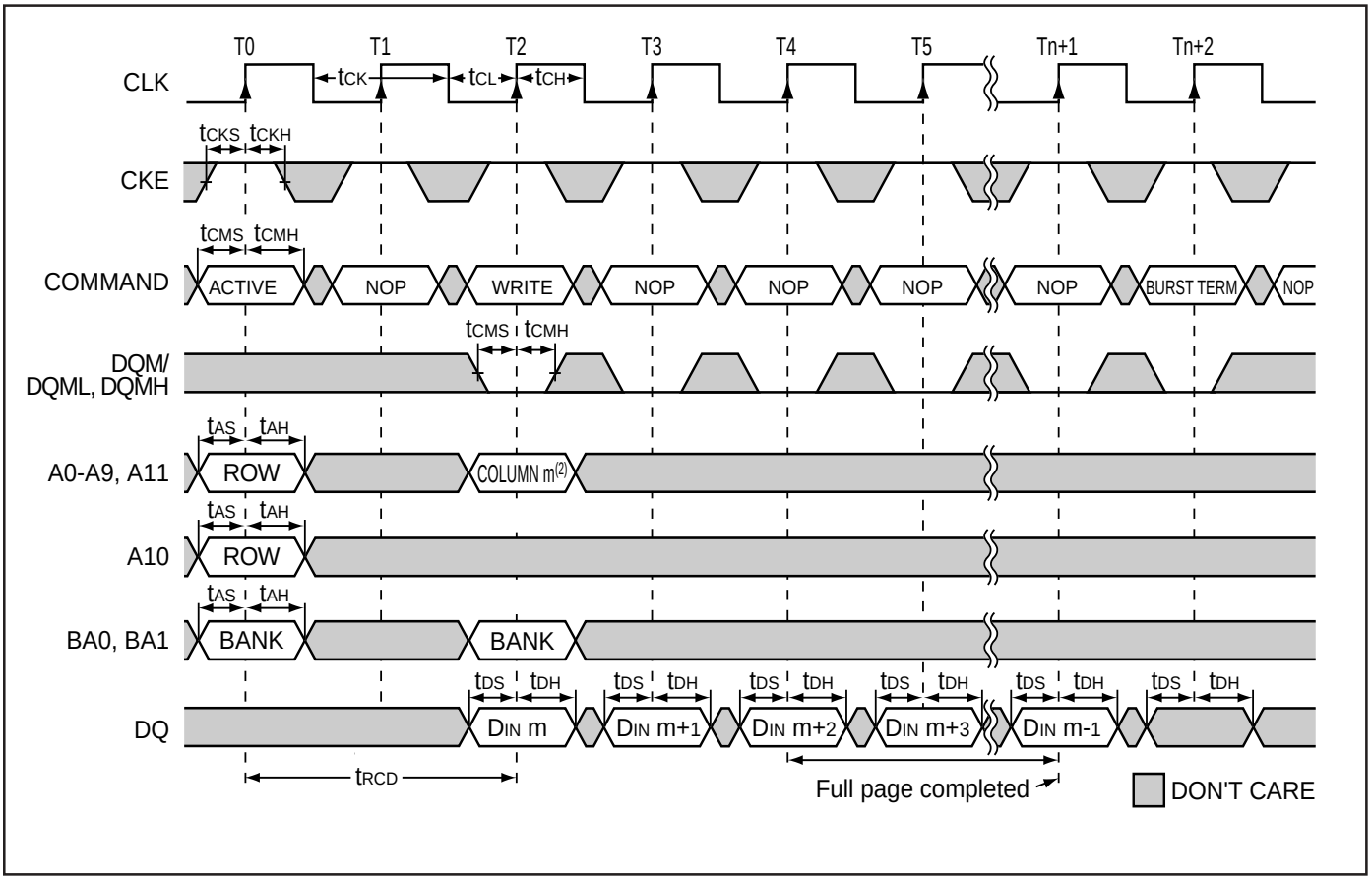
WRITE to PRECHARGE (t_{WR} @ t_{CK} < 15ns)



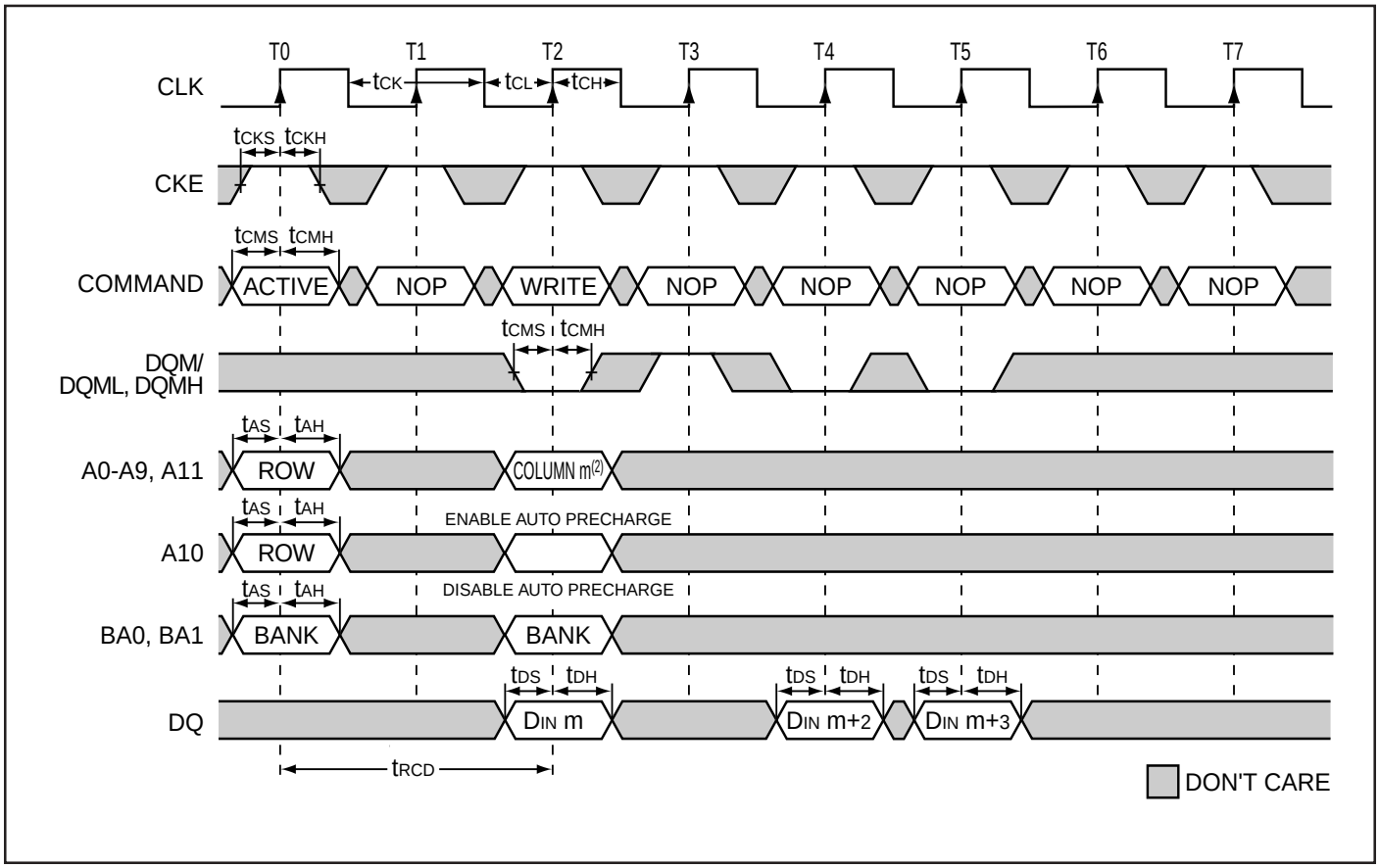
WRITE Burst Termination



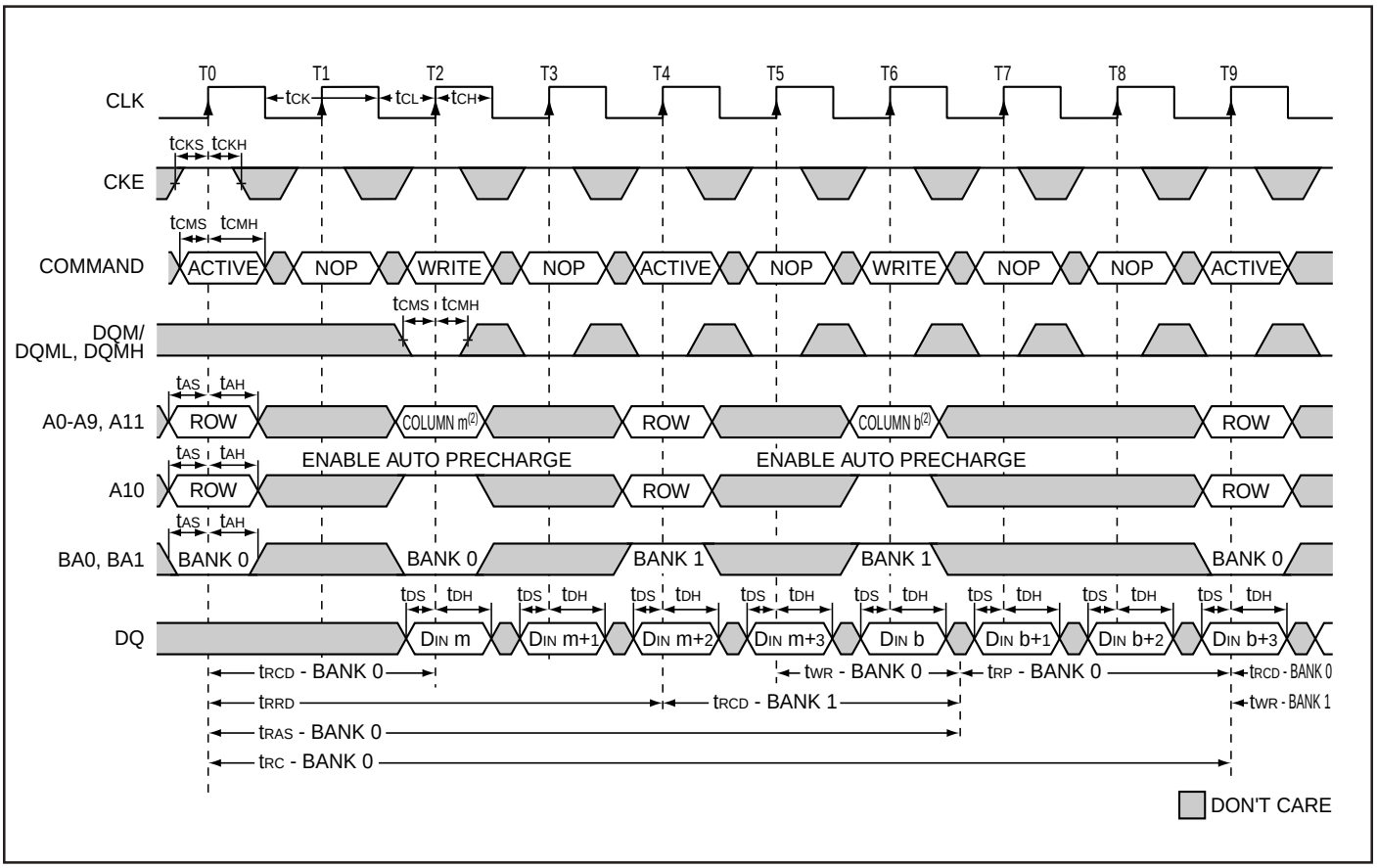
WRITE - FULL PAGE BURST



WRITE - DQM OPERATIOON



ALTERNATING BANK WRITE ACCESS



CLOCK SUSPEND

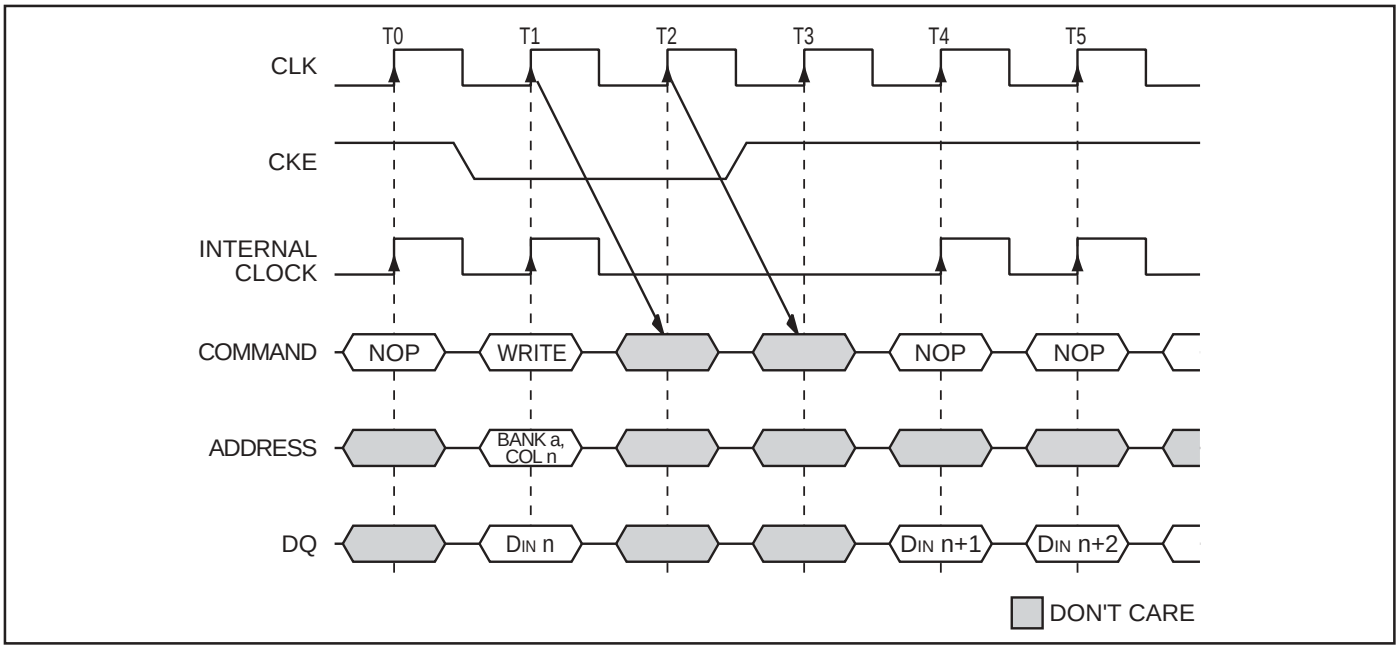
Clock suspend mode occurs when a column access/burst is in progress and CKE is registered LOW. In the clock suspend mode, the internal clock is deactivated, "freezing" the synchronous logic.

For each positive clock edge on which CKE is sampled LOW, the next internal positive clock edge is suspended.

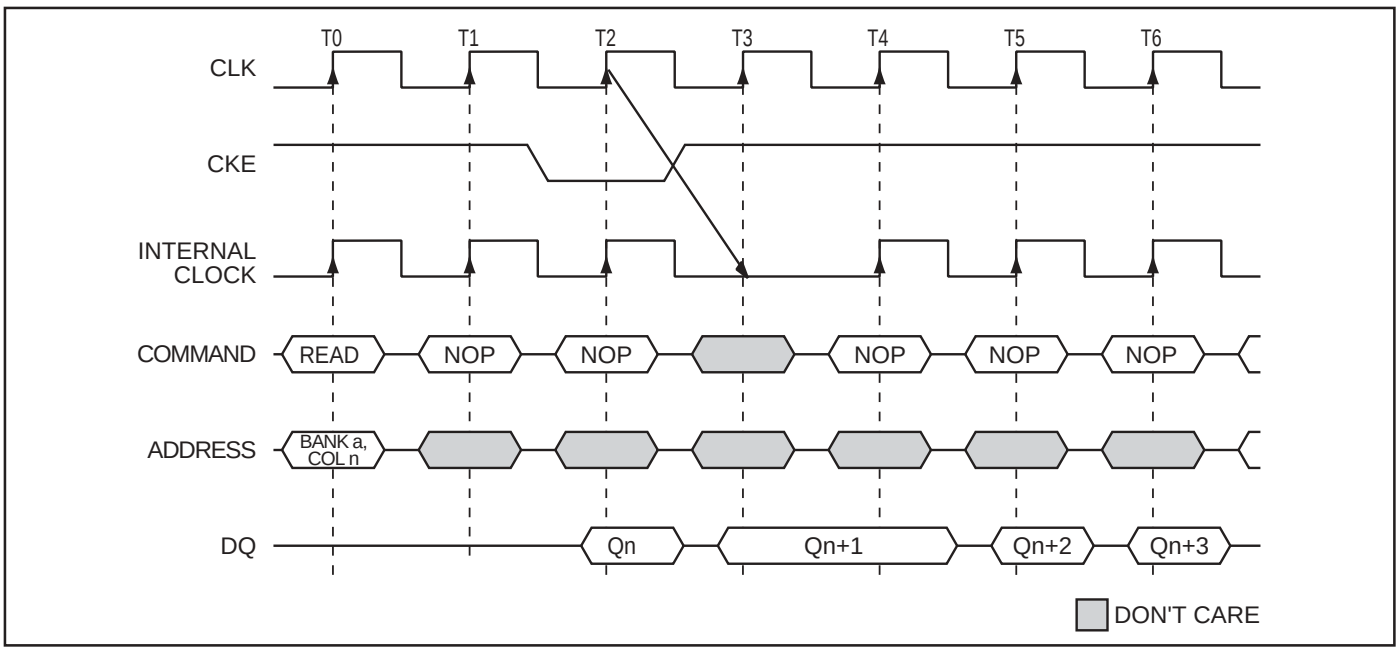
Any command or data present on the input pins at the time of a suspended internal clock edge is ignored; any data present on the DQ pins remains driven; and burst counters are not incremented, as long as the clock is suspended. (See following examples.)

Clock suspend mode is exited by registering CKE HIGH; the internal clock and related operation will resume on the subsequent positive clock edge.

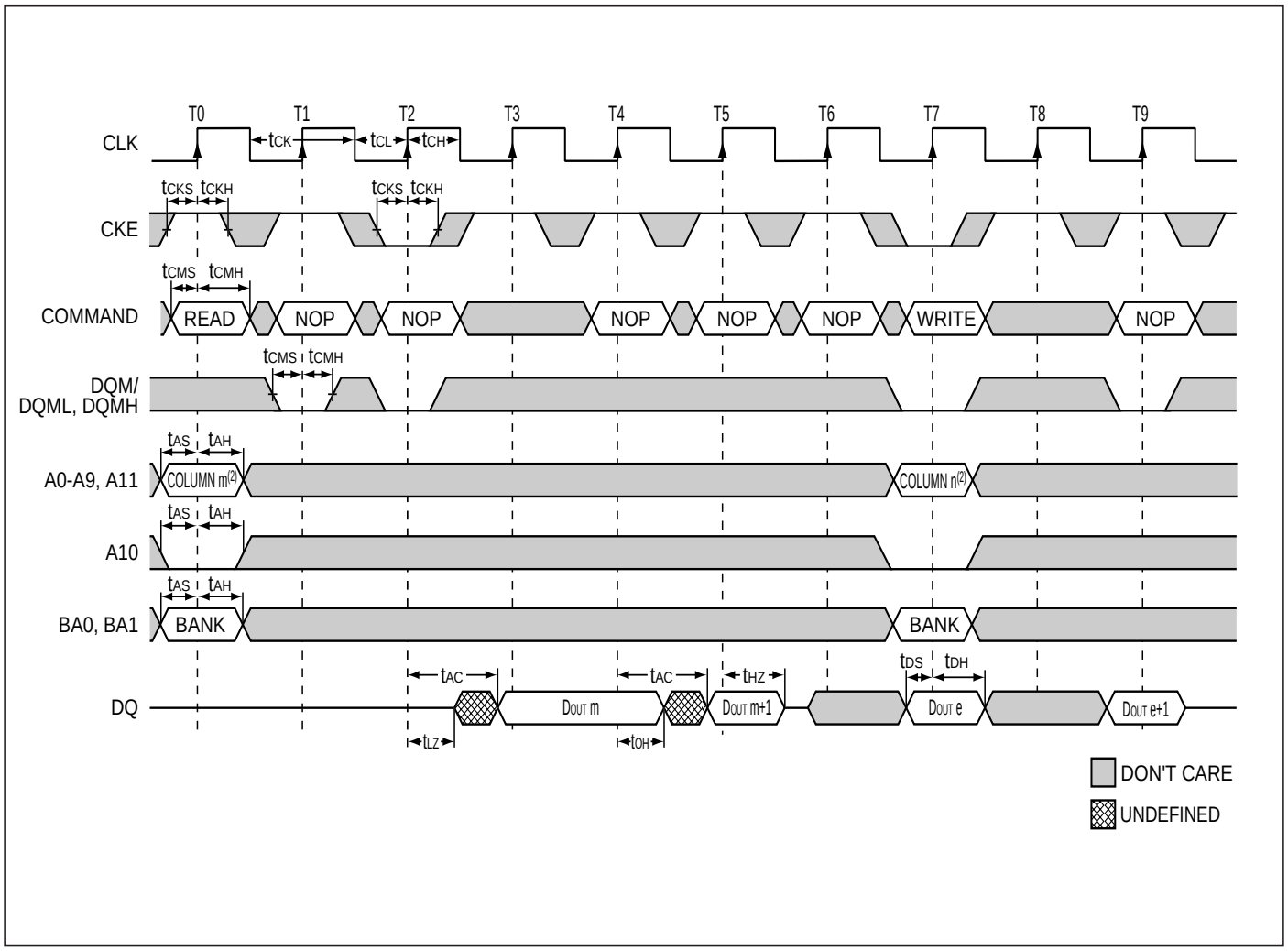
Clock Suspend During WRITE Burst



Clock Suspend During READ Burst



CLOCK SUSPEND MODE



$\overline{CAS}$ latency = 2, burst length = 2

PRECHARGE

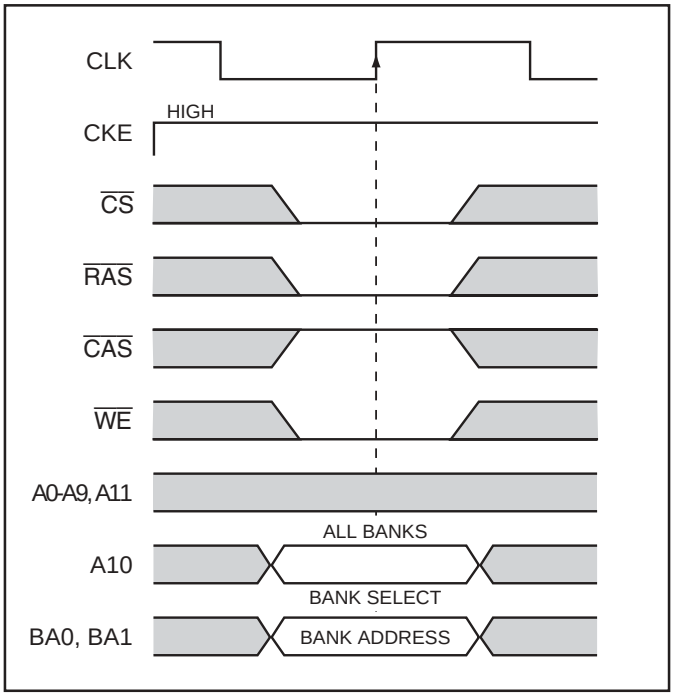
The PRECHARGE command (see figure) is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A10 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 select the bank. When all banks are to be precharged, inputs BA0, BA1 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank.

POWER-DOWN

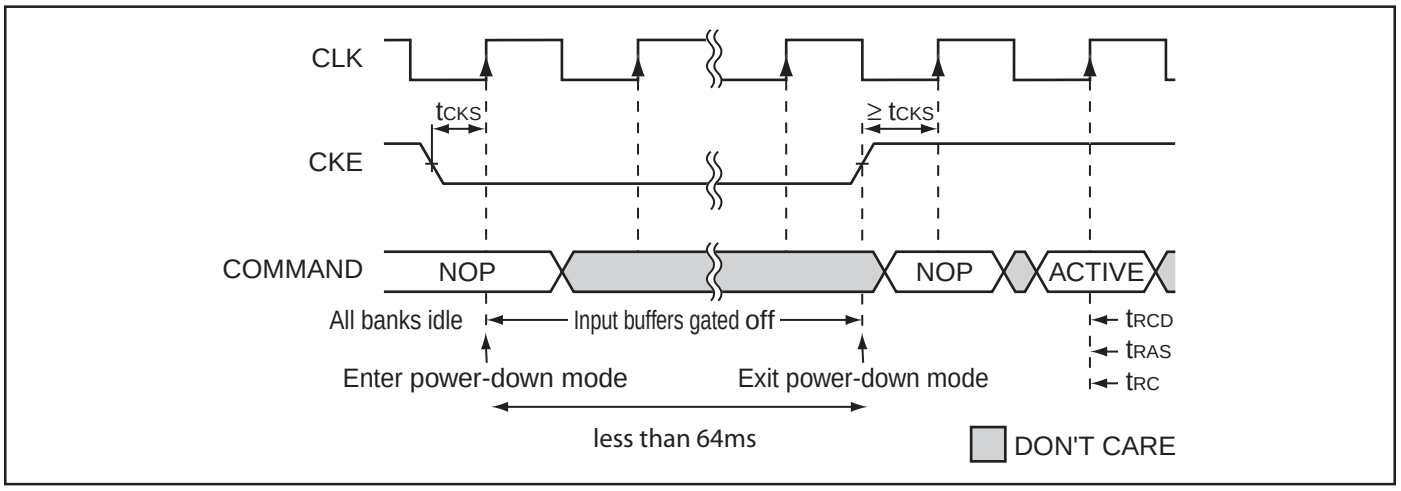
Power-down occurs if CKE is registered LOW coincident with a NOP or COMMAND INHIBIT when no accesses are in progress. If power-down occurs when all banks are idle, this mode is referred to as precharge power-down; if power-down occurs when there is a row active in either bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CKE, for maximum power savings while in standby. The device may not remain in the power-down state longer than the refresh period (64ms) since no refresh operations are performed in this mode.

The power-down state is exited by registering a NOP or COMMAND INHIBIT and CKE HIGH at the desired clock edge (meeting t_{CKS}). See figure below.

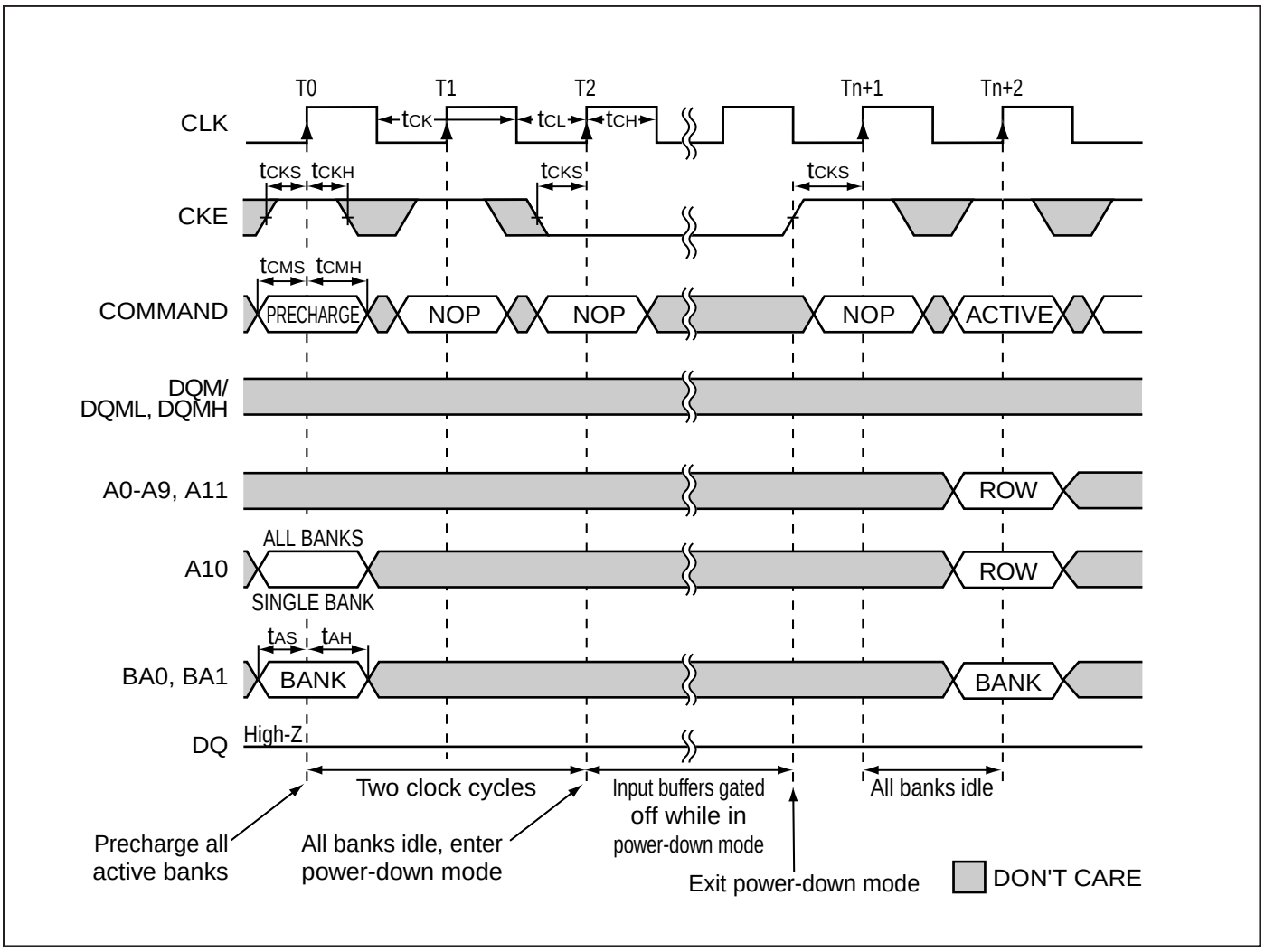
PRECHARGE Command



POWER-DOWN



POWER-DOWN MODE CYCLE



$\overline{CAS}$ latency = 2, 3

BURST READ/SINGLE WRITE

The burst read/single write mode is entered by programming the write burst mode bit (M9) in the mode register to a logic 1. In this mode, all WRITE commands result in the access of a single column location (burst of one), regardless of the programmed burst length. READ commands access columns according to the programmed burst length and sequence, just as in the normal mode of operation (M9 = 0).

CONCURRENT AUTO PRECHARGE

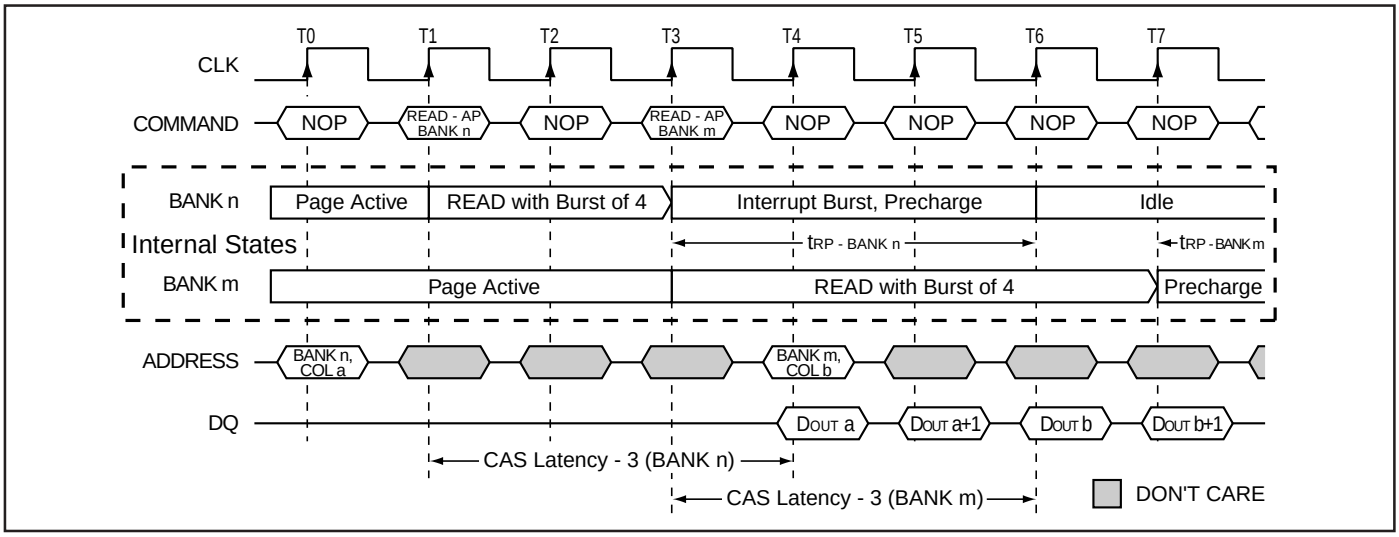
An access command (READ or WRITE) to another bank while an access command with auto precharge enabled is executing is not allowed by SDRAMs, unless the SDRAM supports CONCURRENT AUTO PRECHARGE. *ISSI* SDRAMs support CONCURRENT AUTO PRECHARGE.

Four cases where CONCURRENT AUTO PRECHARGE occurs are defined below.

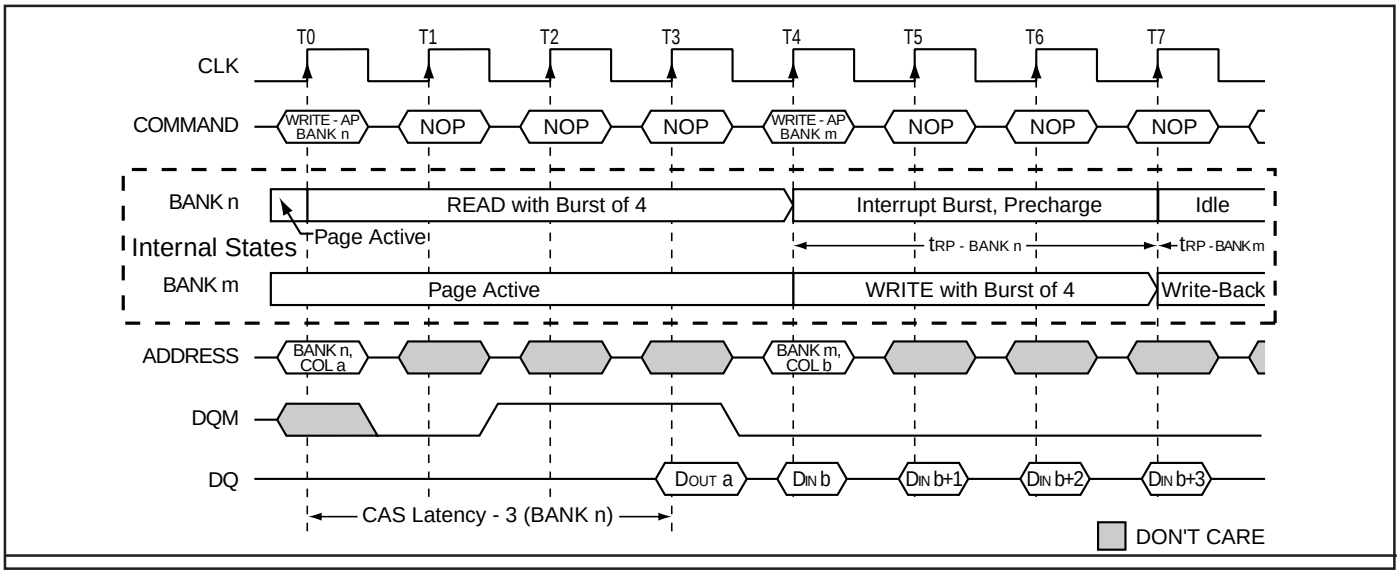
READ with Auto Precharge

1. Interrupted by a READ (with or without auto precharge): A READ to bank m will interrupt a READ on bank n, CAS latency later. The PRECHARGE to bank n will begin when the READ to bank m is registered.
2. Interrupted by a WRITE (with or without auto precharge): A WRITE to bank m will interrupt a READ on bank n when registered. DQM should be used two clocks prior to the WRITE command to prevent bus contention. The PRECHARGE to bank n will begin when the WRITE to bank m is registered.

READ With Auto Precharge interrupted by a READ



READ With Auto Precharge interrupted by a WRITE

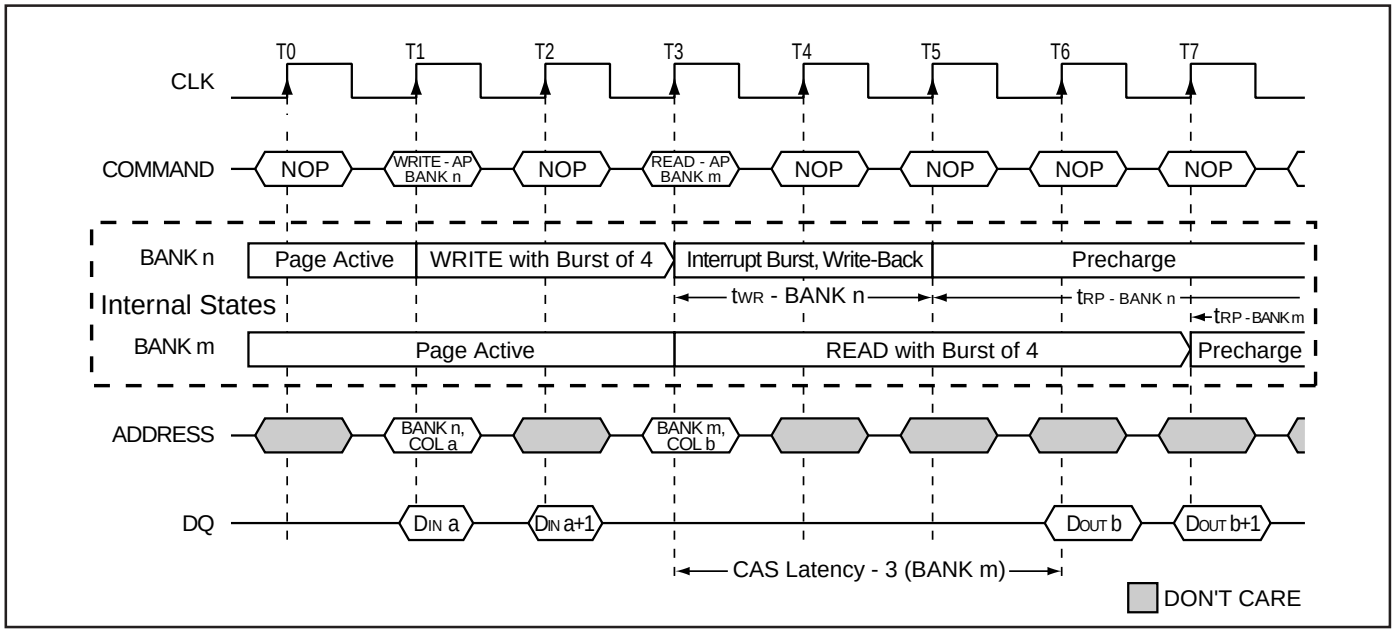


WRITE with Auto Precharge

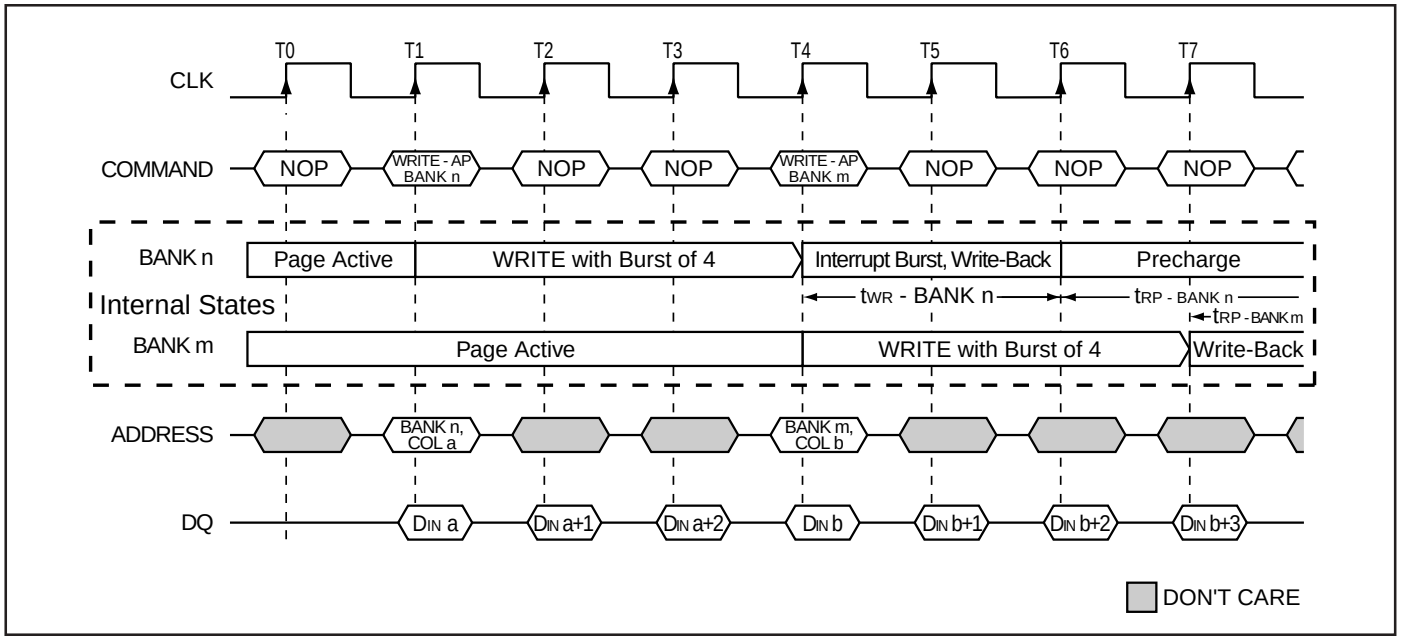
3. Interrupted by a READ (with or without auto precharge): A READ to bank m will interrupt a WRITE on bank n when registered, with the data-out appearing (CAS latency) later. The PRECHARGE to bank n will begin after t_{WR} is met, where t_{WR} begins when the READ to bank m is registered. The last valid WRITE to bank n will be data-in registered one clock prior to the READ to bank m.

4. Interrupted by a WRITE (with or without auto precharge): AWRITE to bank m will interrupt a WRITE on bank n when registered. The PRECHARGE to bank n will begin after t_{WR} is met, where t_{WR} begins when the WRITE to bank m is registered. The last valid data WRITE to bank n will be data registered one clock prior to a WRITE to bank m.

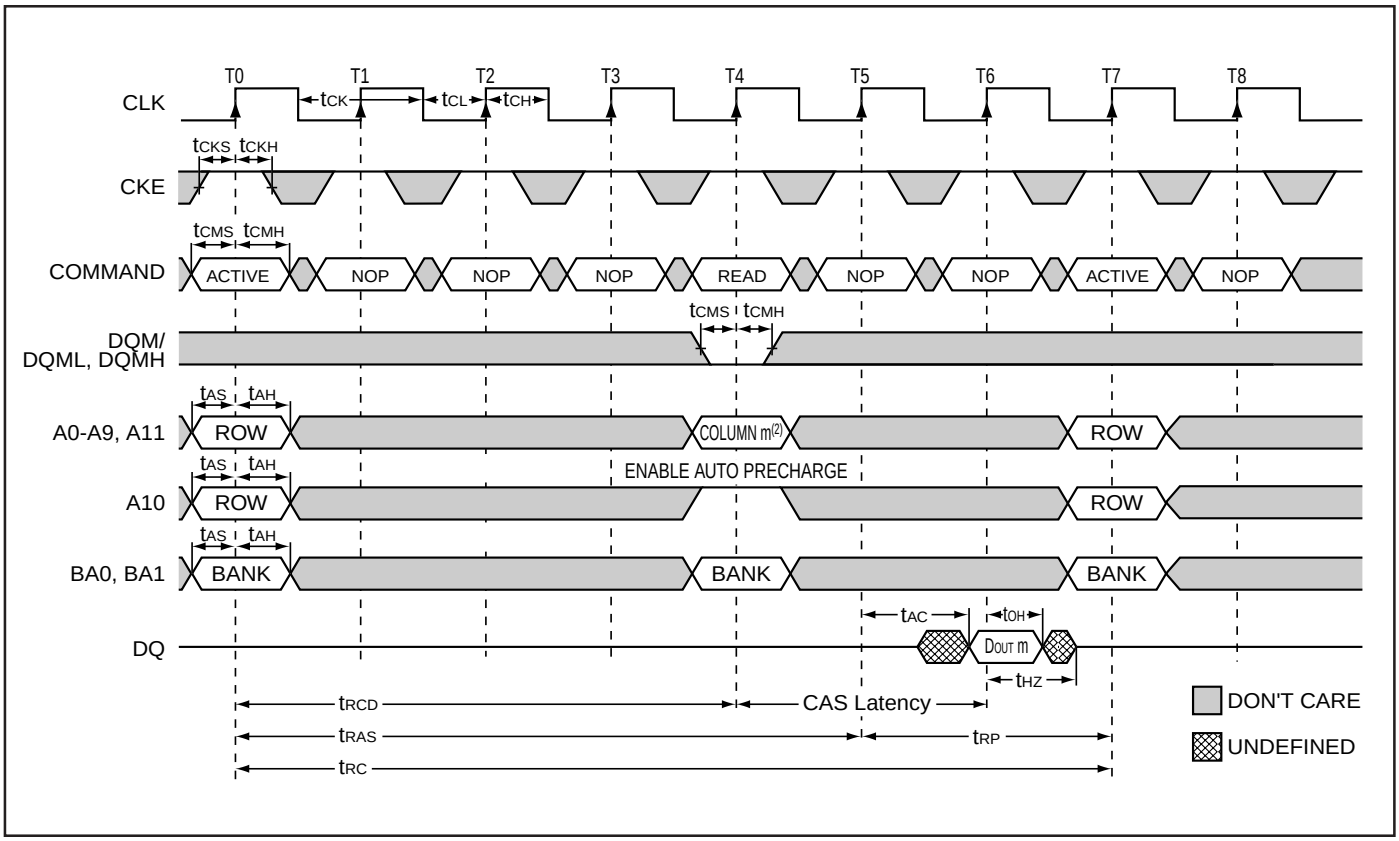
WRITE With Auto Precharge interrupted by a READ



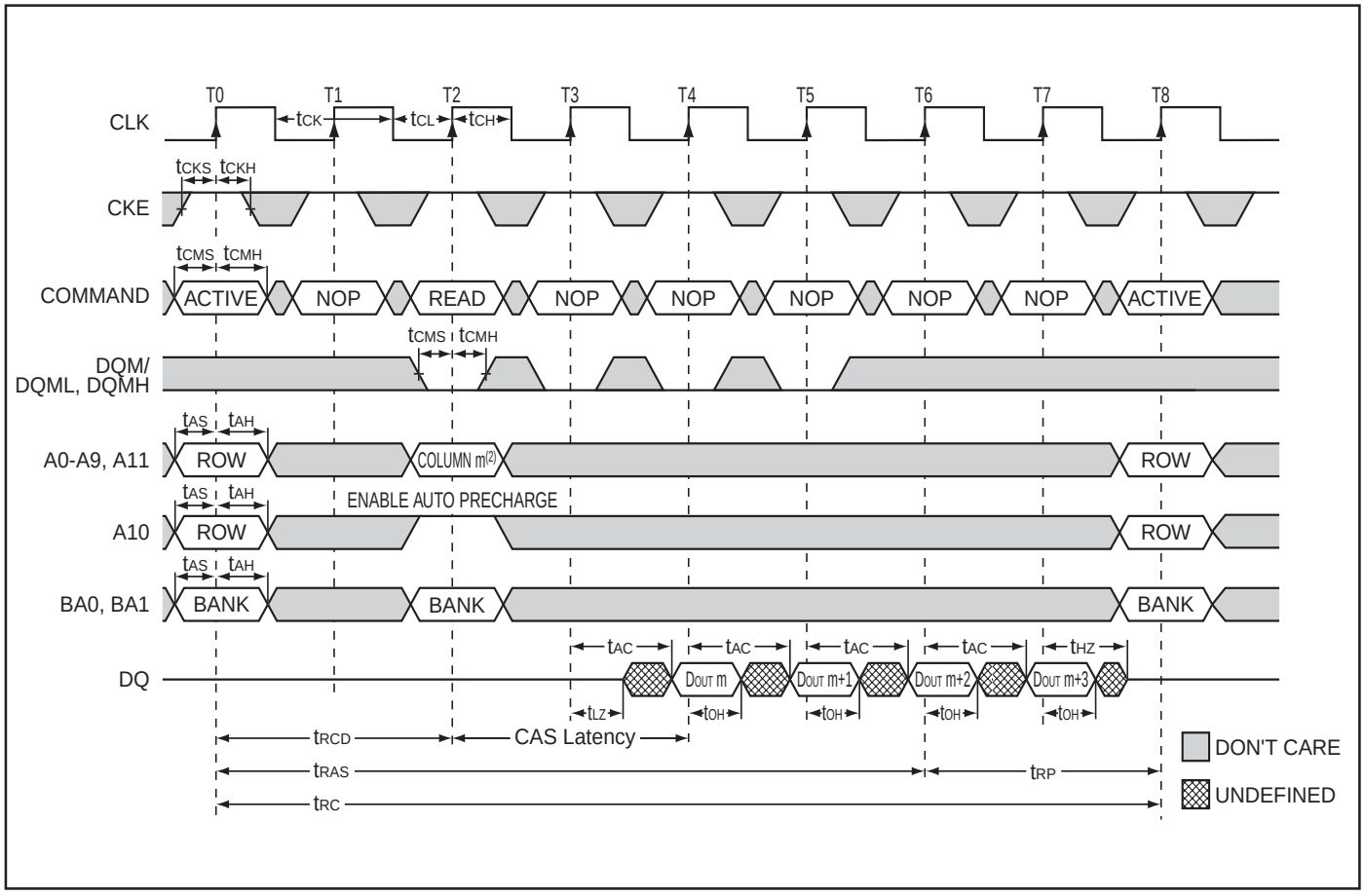
WRITE With Auto Precharge interrupted by a WRITE



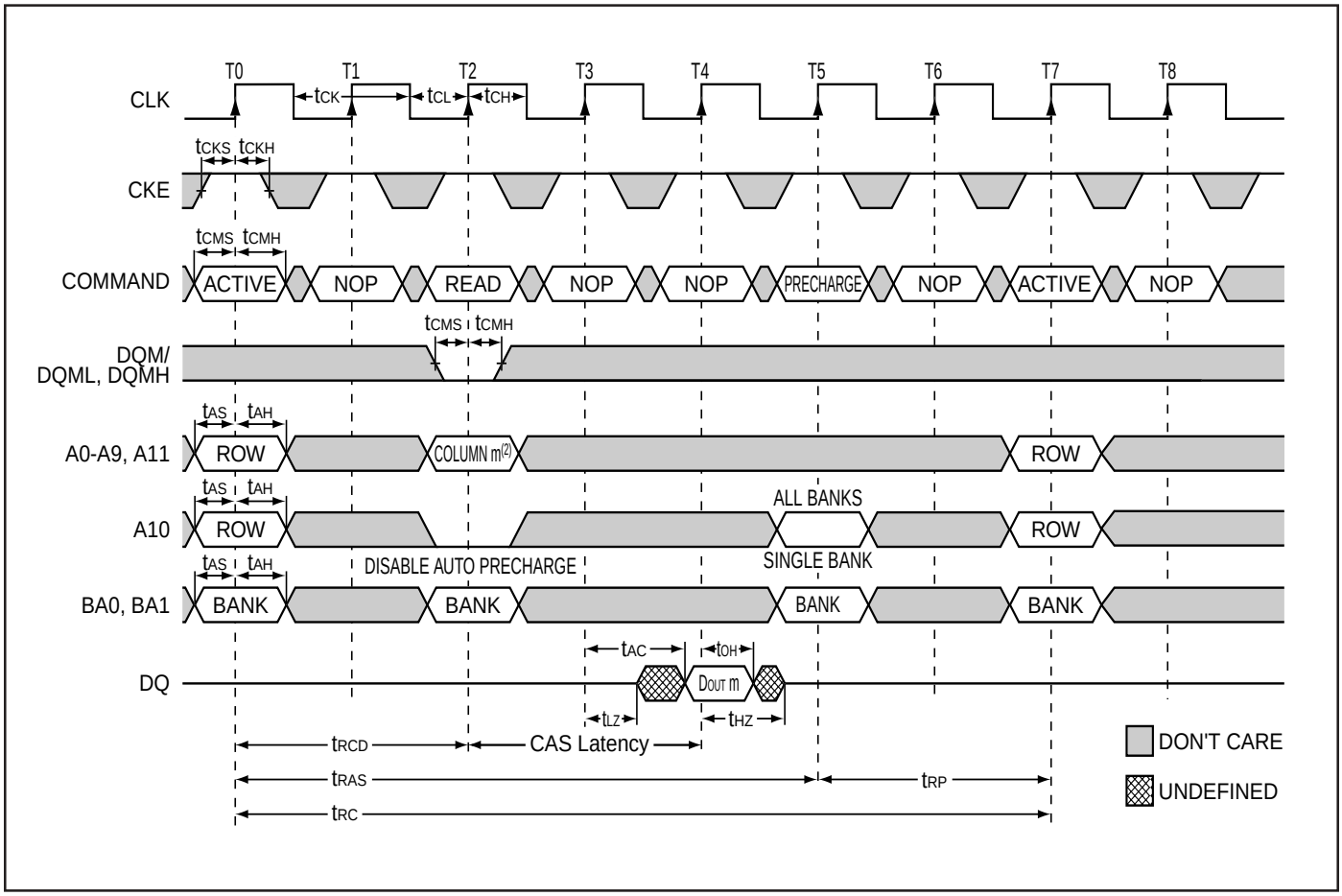
SINGLE READ WITH AUTO PRECHARGE



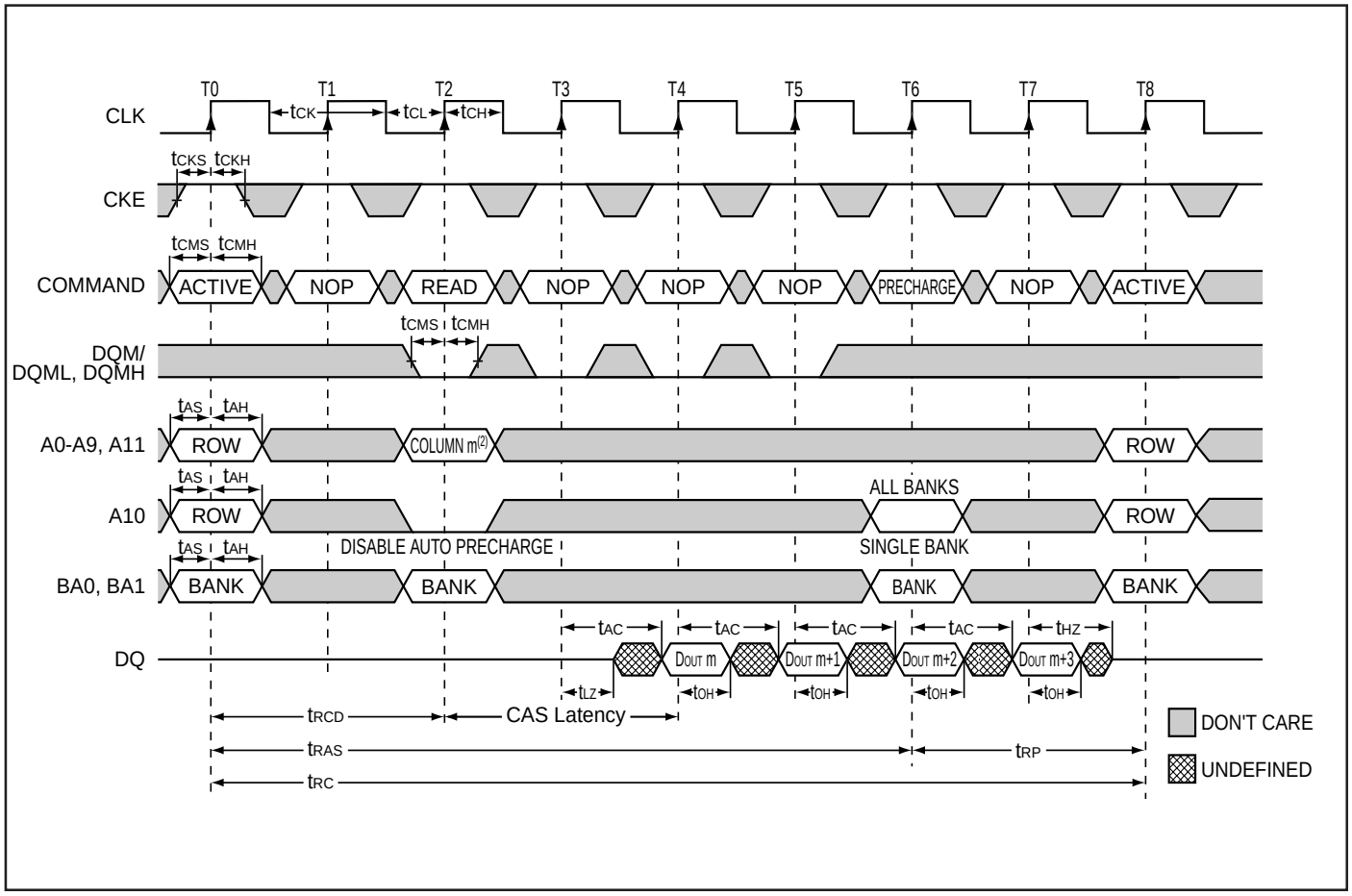
READ WITH AUTO PRECHARGE



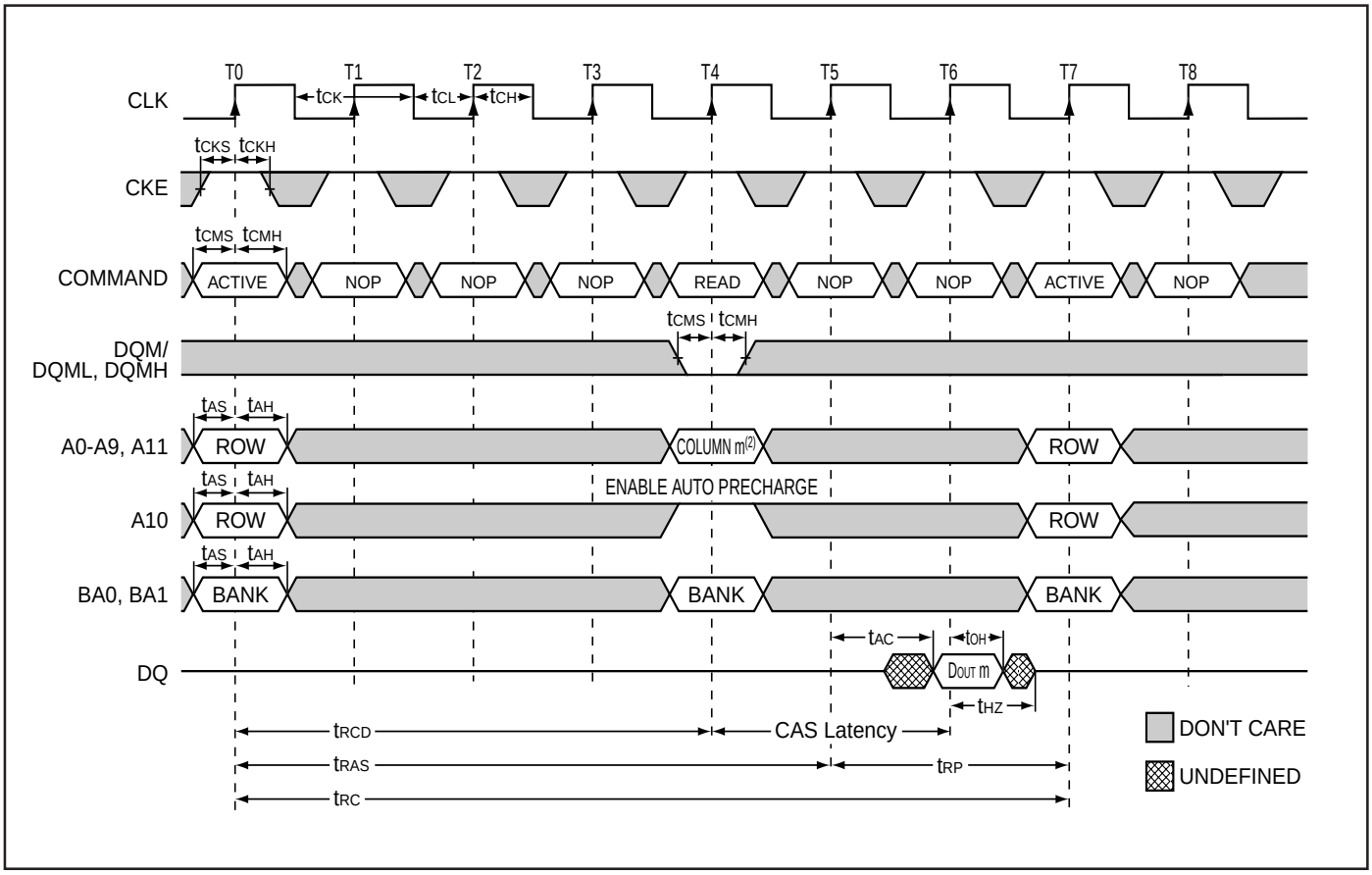
SINGLE READ WITHOUT AUTO PRECHARGE



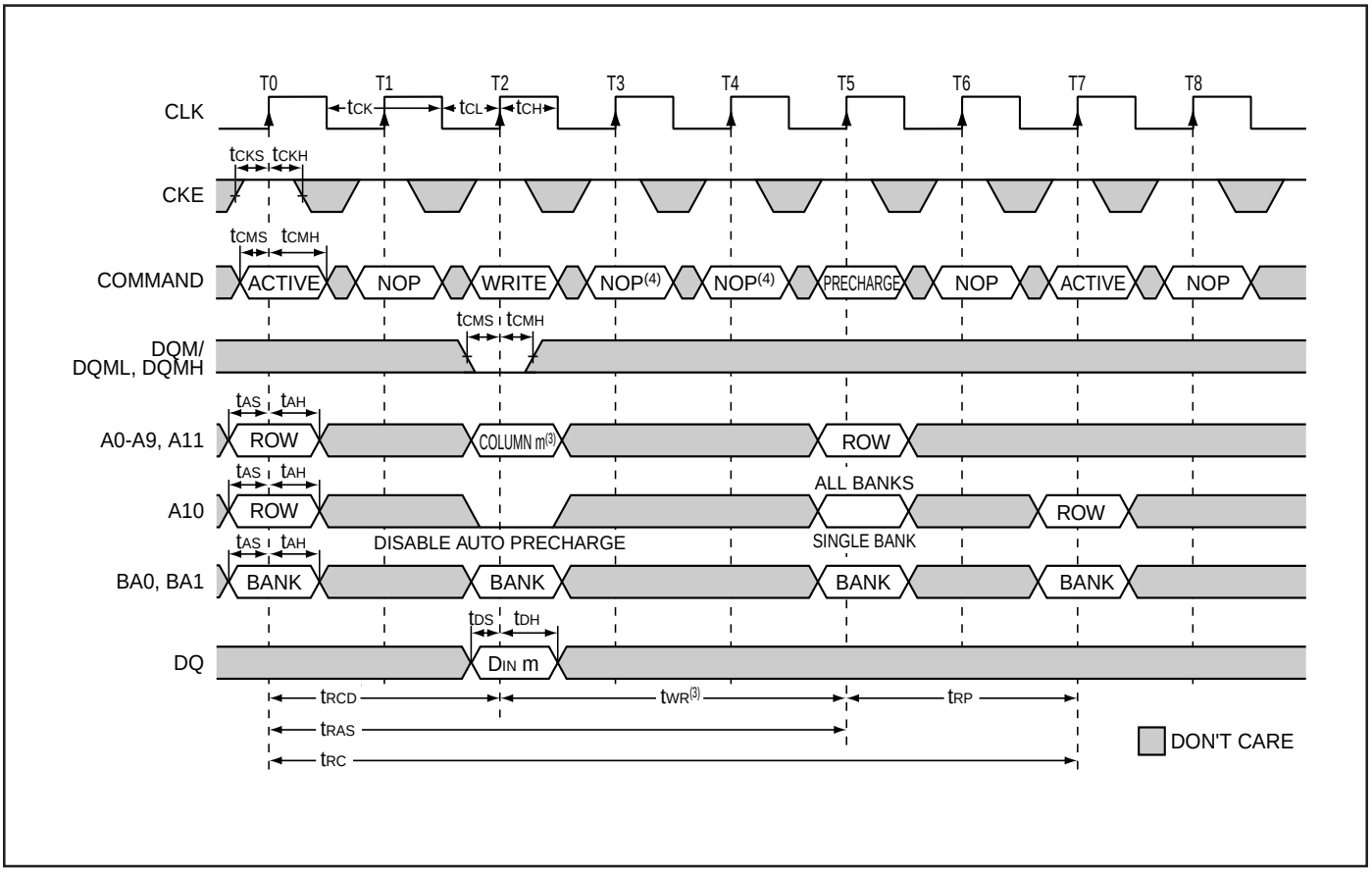
READ WITHOUT AUTO PRECHARGE



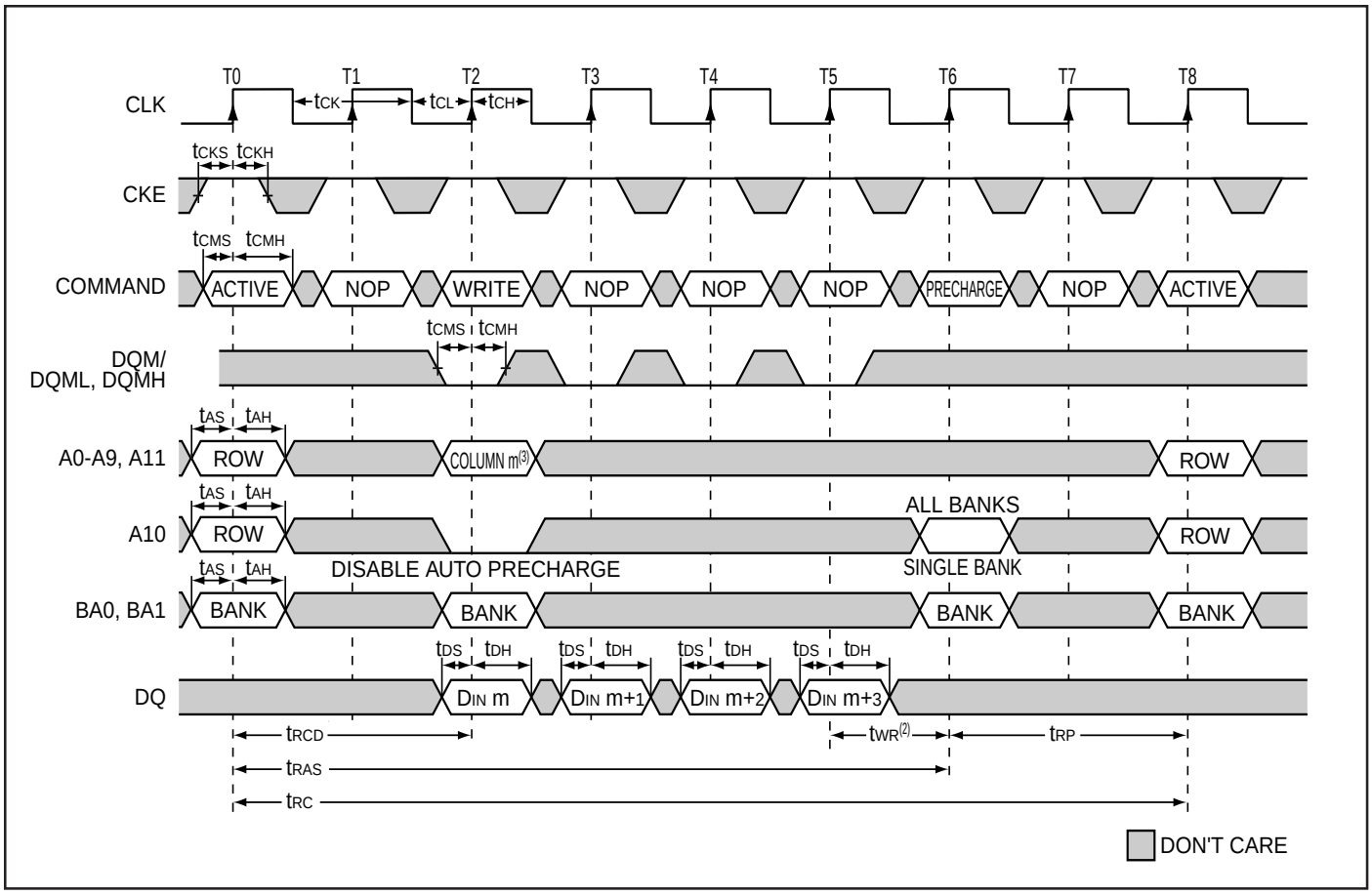
SINGLE READ WITH AUTO PRECHARGE



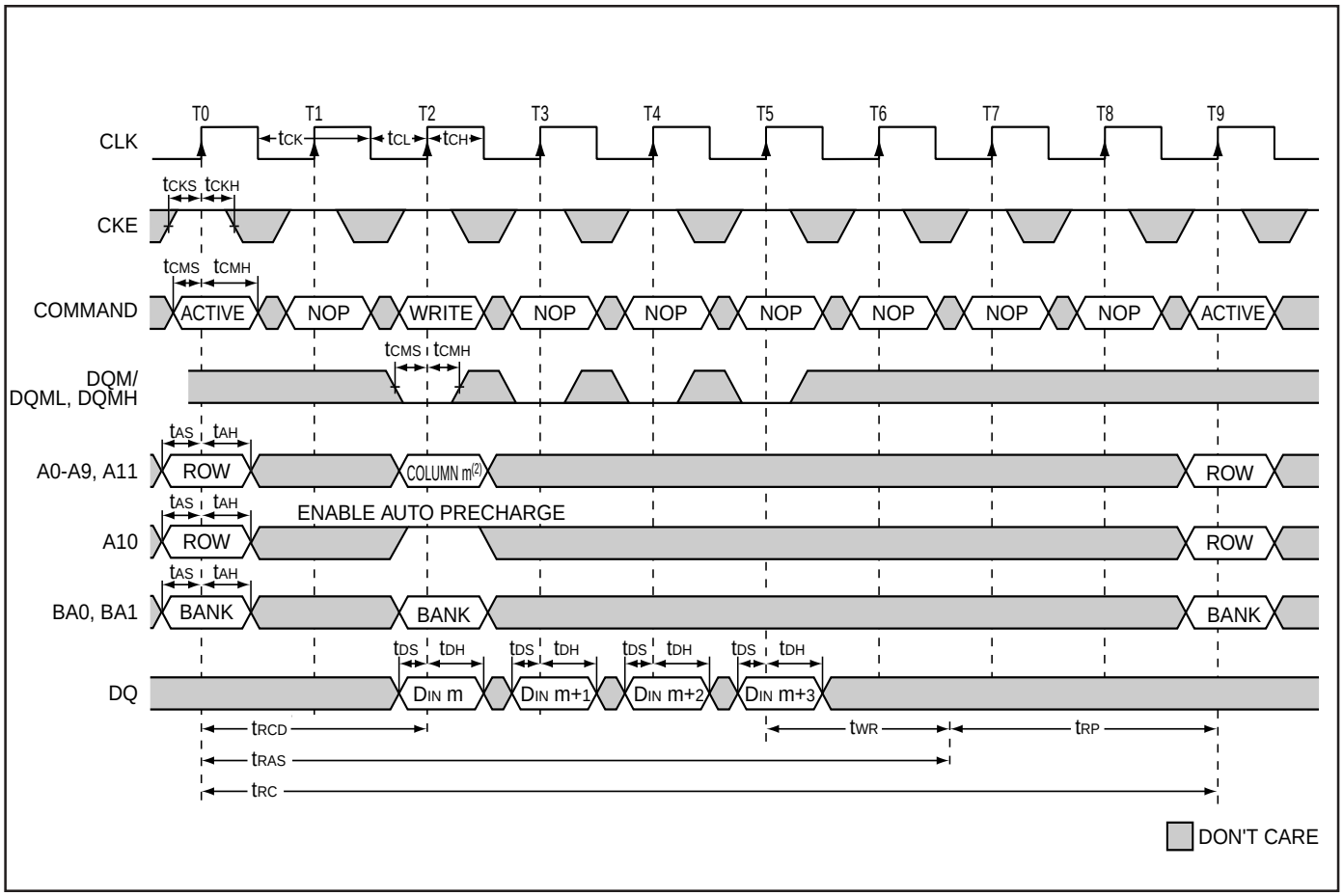
SINGLE WRITE - WITHOUT AUTO PRECHARGE



WRITE - WITHOUT AUTO PRECHARGE



WRITE - WITH AUTO PRECHARGE



ORDERING INFORMATION - V_{DD} = 2.5V

Commercial Range: 0°C to 70°C

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42LS81600A-7T	54pin TSOPII
100 MHz	10	IS42LS81600A-10T	54pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
143 MHz	7	IS42LS16800A-7B	54 pin BGA
		IS42LS16800A-7T	54 Pin TSOPII
100 MHz	10	IS42LS16800A-10B	54 pin BGA
		IS42LS16800A-10T	54 Pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42LS32400A-7B	90 pin BGA
		IS42LS32400A-7T	86-Pin TSOPII
100 MHz	10	IS42LS32400A-10B	90 pin BGA
		IS42LS32400A-10T	86-Pin TSOPII

ORDERING INFORMATION - V_{DD} = 2.5V

Industrial Range: -40°C to 85°C

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42LS81600A-7TI	54pin TSOPII
100 MHz	10	IS42LS81600A-10TI	54pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42LS16800A-7BI	54 pin BGA
		IS42LS16800A-7TI	54 Pin TSOPII
100 MHz	10	IS42LS16800A-10BI	54 pin BGA
		IS42LS16800A-10TI	54 Pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42LS32400A-7BI	90 pin BGA
		IS42LS32400A-7TI	86-Pin TSOPII
100 MHz	10	IS42LS32400A-10BI	90 pin BGA
		IS42LS32400A-10TI	86-Pin TSOPII

ORDERING INFORMATION - V_{DD} = 3.3V

Commercial Range: 0°C to 70°C

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42S81600A-7T	54pin TSOPII
100 MHz	10	IS42S81600A-10T	54pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42S16800A-7B IS42S16800A-7T	54 pin BGA 54 Pin TSOPII
100 MHz	10	IS42S16800A-10B IS42S16800A-10T	54 pin BGA 54 Pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42S32400A-7B IS42S32400A-7T	90 pin BGA 86-Pin TSOPII
100 MHz	10	IS42S32400A-10B IS42S32400A-10T	90 pin BGA 86-Pin TSOPII

ORDERING INFORMATION - V_{DD} = 3.3V

Industrial Range: -40°C to 85°C

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42S81600A-7TI	54pin TSOPII
100 MHz	10	IS42S81600A-10TI	54pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42S16800A-7BI IS42S16800A-7TI	54 pin BGA 54 Pin TSOPII
100 MHz	10	IS42S16800A-10BI IS42S16800A-10TI	54 pin BGA 54 Pin TSOPII

Frequency	Speed (ns)	Order Part No.	Package
133 MHz	7	IS42S32400A-7BI IS42S32400A-7TI	90 pin BGA 86-Pin TSOPII
100 MHz	10	IS42S32400A-10BI IS42S32400A-10TI	90 pin BGA 86-Pin TSOPII