- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Supports 5-V V_{CC} Operation**
- **Inputs Accept Voltages to 5.5 V**
- **Max t_{pd} of 4.1 ns at 3.3 V**
- **Low Power Consumption, 10-µA Max I_{CC}**
- **±24-mA Output Drive at 3.3 V**
- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >2 V at V_{CC} = 3.3 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Protection Exceeds JESD 22**
    - **2000-V Human-Body Model (A114-A)**
    - **200-V Machine Model (A115-A)**
    - **1000-V Charged-Device Model (C101)**

DCT OR DCU PACKAGE
(TOP VIEW)

1OE	1	8	V_{CC}
1A	2	7	2OE
2Y	3	6	1Y
GND	4	5	2A
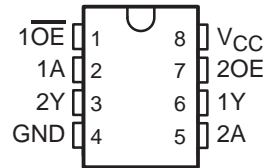
YEA, YEP, YZA, OR YZP PACKAGE
(BOTTOM VIEW)

GND	4	5	2A
2Y	3	6	1Y
1A	2	7	2OE
1OE	1	8	V_{CC}
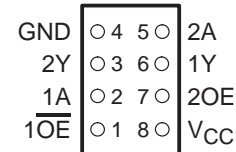
description/ordering information

This dual buffer/line driver is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC2G241 is designed specifically to improve both the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.17-mm Small Bump – YEA	Reel of 3000	SN74LVC2G241YEAR	_ _ _C2_
	NanoFree™ – WCSP (DSBGA) 0.17-mm Small Bump – YZA (Pb-free)		SN74LVC2G241YZAR	
	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP		SN74LVC2G241YEPR	
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC2G241YZPR	
	SSOP – DCT	Reel of 3000	SN74LVC2G241DCTR	C41_ _ _
	VSSOP – DCU	Reel of 3000	SN74LVC2G241DCUR	C41_
		Reel of 250	SN74LVC2G241DCUT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.
YEA/YZA, YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, ● = Pb-free).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

TEXAS INSTRUMENTS

description/ordering information (continued)

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The SN74LVC2G241 is organized as two 1-bit line drivers with separate output-enable (1$\overline{\text{OE}}$, 2OE) inputs. When 1$\overline{\text{OE}}$ is low and 2OE is high, the device passes data from the A inputs to the Y outputs. When 1$\overline{\text{OE}}$ is high and 2OE is low, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{\text{OE}}$ should be tied to V$_{CC}$ through a pullup resistor, and OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sinking or the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using I$_{off}$. The I$_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Function Tables

INPUTS		OUTPUT
1$\overline{\text{OE}}$	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUTS		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

logic diagram (positive logic)
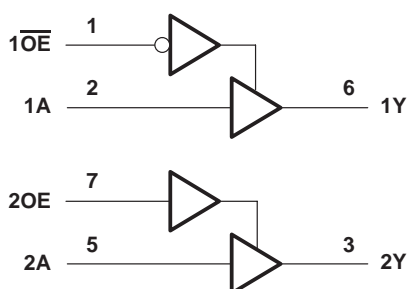
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . –0.5 V to 6.5 V

Input voltage range, V_I (see Note 1) . . . . –0.5 V to 6.5 V

Voltage range applied to any output in the high-impedance or power-off state, V_O
(see Note 1) . . . . –0.5 V to 6.5 V

Voltage range applied to any output in the high or low state, V_O
(see Notes 1 and 2) . . . . –0.5 V to V_{CC} + 0.5 V

Input clamp current, I_{IK} ($V_I < 0$) . . . . –50 mA

Output clamp current, I_{OK} ($V_O < 0$) . . . . –50 mA

Continuous output current, I_O . . . . ±50 mA

Continuous current through V_{CC} or GND . . . . ±100 mA

Package thermal impedance, θ_{JA} (see Note 3): DCT package . . . . 220°C/W
DCU package . . . . 227°C/W
YEA/YZA package . . . . 140°C/W
YEP/YZP package . . . . 102°C/W

Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

			MIN	MAX	UNIT
V_{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 1.95 V	$0.65 \times V_{CC}$		V
		V_{CC} = 2.3 V to 2.7 V	1.7		
		V_{CC} = 3 V to 3.6 V	2		
		V_{CC} = 4.5 V to 5.5 V	$0.7 \times V_{CC}$		
V_{IL}	Low-level input voltage	V_{CC} = 1.65 V to 1.95 V		$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.8	
		V_{CC} = 4.5 V to 5.5 V		$0.3 \times V_{CC}$	
V_I	Input voltage		0	5.5	V
V_O	Output voltage	High or low state	0	V_{CC}	V
		3-state	0	5.5	
I_{OH}	High-level output current	V_{CC} = 1.65 V		−4	mA
		V_{CC} = 2.3 V		−8	
		V_{CC} = 3 V		−16	
				−24	
		V_{CC} = 4.5 V		−32	
I_{OL}	Low-level output current	V_{CC} = 1.65 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 3 V		16	
				24	
		V_{CC} = 4.5 V		32	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V_{CC} = 3.3 V ± 0.3 V		10	
		V_{CC} = 5 V ± 0.5 V		5	
T_A	Operating free-air temperature		−40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP†	MAX	UNIT
V_{OH}		$I_{OH} = -100\ \mu A$		1.65 V to 5.5 V	$V_{CC}-0.1$			V
		$I_{OH} = -4$ mA		1.65 V	1.2			
		$I_{OH} = -8$ mA		2.3 V	1.9			
		$I_{OH} = -16$ mA		3 V	2.4			
		$I_{OH} = -24$ mA			2.3			
		$I_{OH} = -32$ mA		4.5 V	3.8			
V_{OL}		$I_{OL} = 100\ \mu A$		1.65 V to 5.5 V			0.1	V
		$I_{OL} = 4$ mA		1.65 V			0.45	
		$I_{OL} = 8$ mA		2.3 V			0.3	
		$I_{OL} = 16$ mA		3 V			0.4	
		$I_{OL} = 24$ mA					0.55	
		$I_{OL} = 32$ mA		4.5 V			0.55	
I_I	A or Control inputs	$V_I = 5.5$ V or GND		0 to 5.5 V			±5	μA
I_{off}		V_I or $V_O = 5.5$ V		0			±10	μA
I_{OZ}		$V_O = 0$ to 5.5 V		3.6 V			10	μA
I_{CC}		$V_I = 5.5$ V or GND,	$I_O = 0$	1.65 V to 5.5 V			10	μA
ΔI_{CC}		One input at $V_{CC} - 0.6$ V,	Other inputs at V_{CC} or GND	3 V to 5.5 V			500	μA
C_i		$V_I = V_{CC}$ or GND		3.3 V		3.5		pF
C_o		$V_O = V_{CC}$ or GND		3.3 V		6.5		pF

† All typical values are at $V_{CC} = 3.3$ V, $T_A = 25°C$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 5$ V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	3.3	8.8	1.5	4.8	1.4	4.3	1	3.7	ns
t_{en}	$\overline{OE}$	Y	4	9.9	1.9	5.6	1.2	4.7	1.2	3.8	ns
t_{dis}	$\overline{OE}$	Y	1.5	11.6	1	5.8	1.4	4.4	1	3.4	ns
t_{en}	OE	Y	3.2	8.8	1.5	4.7	1.6	4.1	1.1	3.3	ns
t_{dis}	OE	Y	1.7	12.5	1	5.2	1	4.2	1	3.3	ns

operating characteristics, $T_A = 25°$

PARAMETER			TEST CONDITIONS	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	$V_{CC} = 5$ V	UNIT
				TYP	TYP	TYP	TYP	
C_{pd}	Power dissipation capacitance per buffer/driver	Outputs enabled	f = 10 MHz	19	19	20	22	pF
		Outputs disabled		2	2	2	3	

PARAMETER MEASUREMENT INFORMATION
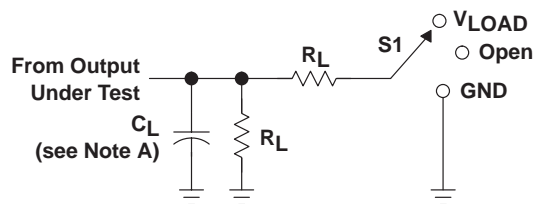
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

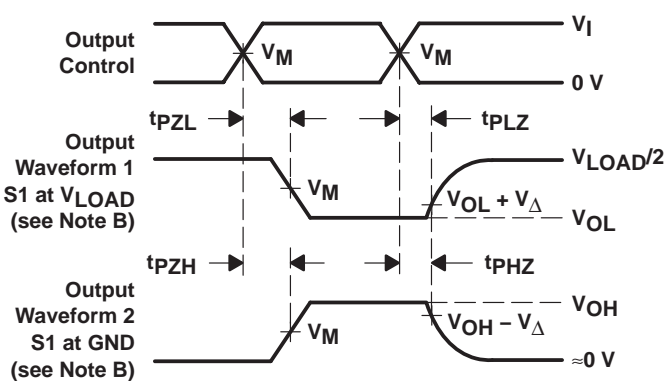| V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
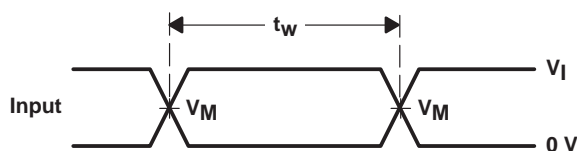
VOLTAGE WAVEFORMS
PULSE DURATION
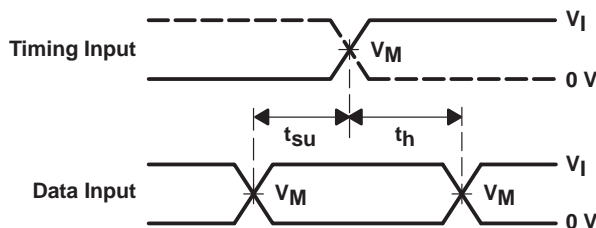
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
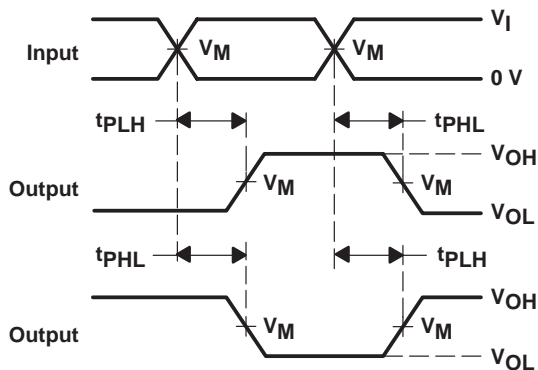
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50$ Ω.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
74LVC2G241DCURE4	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
74LVC2G241DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
74LVC2G241DCUTE4	ACTIVE	US8	DCU	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G241DCTR	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G241DCUR	ACTIVE	US8	DCU	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G241DCUT	ACTIVE	US8	DCU	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC2G241YEAR	ACTIVE	WCSP	YEA	8	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC2G241YEPR	ACTIVE	WCSP	YEP	8	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC2G241YZAR	ACTIVE	WCSP	YZA	8	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM
SN74LVC2G241YZPR	ACTIVE	WCSP	YZP	8	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
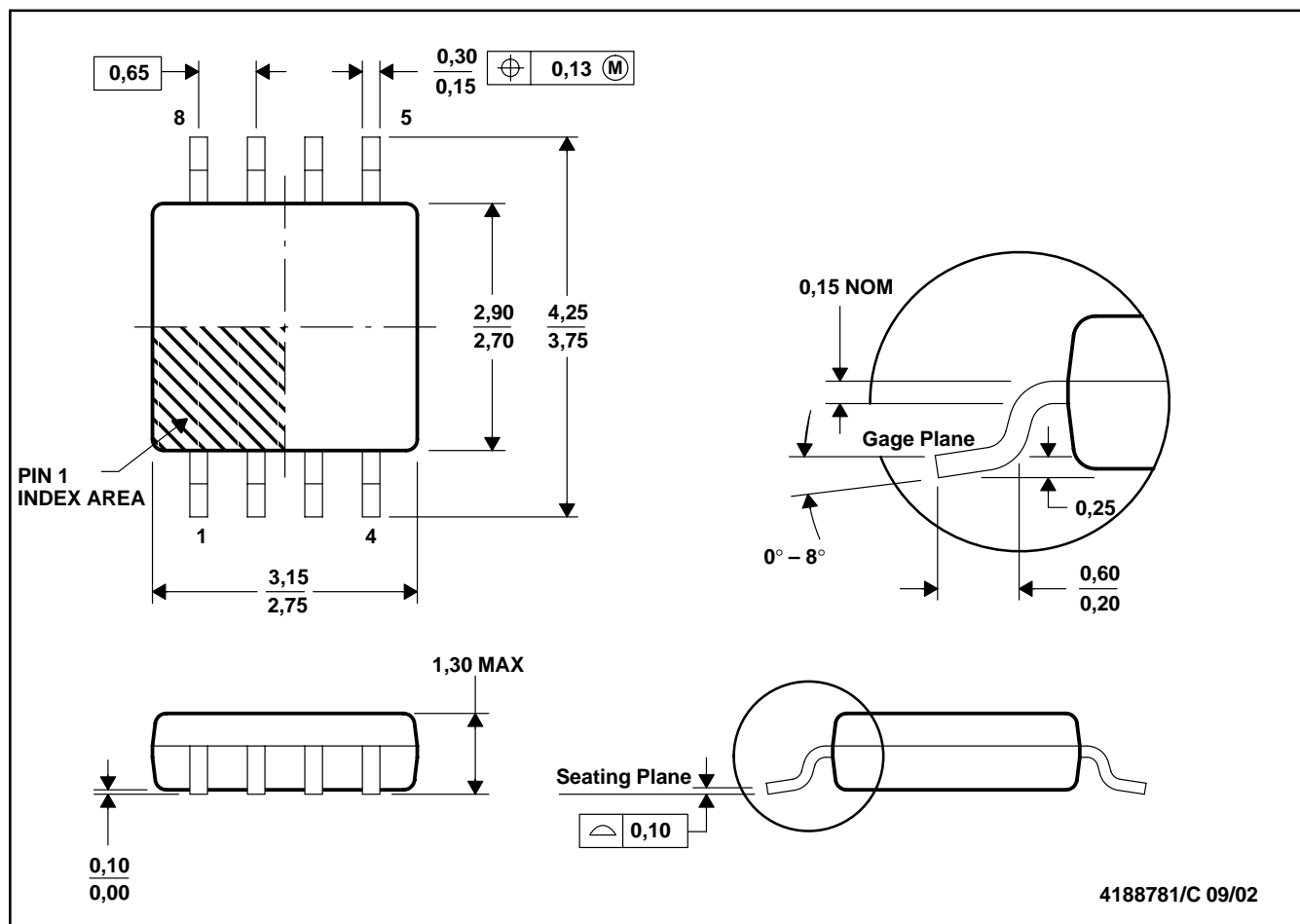
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

DCT (R-PDSO-G8)   **PLASTIC SMALL-OUTLINE PACKAGE**

0,65

0,30
0,15

⊕ 0,13 Ⓜ

8

5

2,90
2,70

4,25
3,75

PIN 1
INDEX AREA

1

4

3,15
2,75

0,15 NOM

Gage Plane

0° – 8°

0,25

0,60
0,20

1,30 MAX

Seating Plane

△ 0,10

0,10
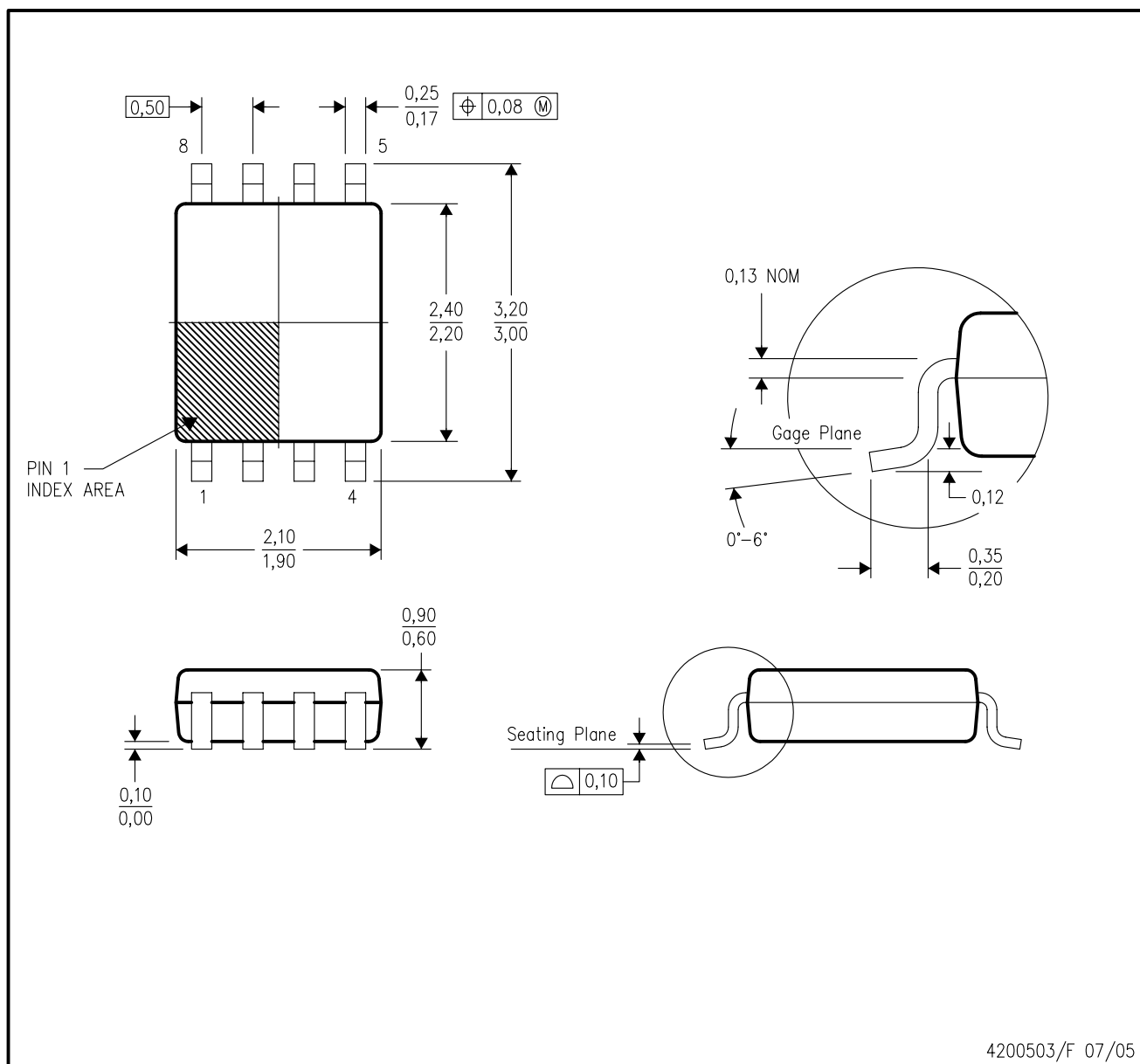0,00

4188781/C 09/02

NOTES: A. All linear dimensions are in millimeters.
           B. This drawing is subject to change without notice.
           C. Body dimensions do not include mold flash or protrusion
           D. Falls within JEDEC MO-187 variation DA.

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DCU (R−PDSO−G8)   PLASTIC SMALL−OUTLINE PACKAGE (DIE DOWN)

4200503/F 07/05
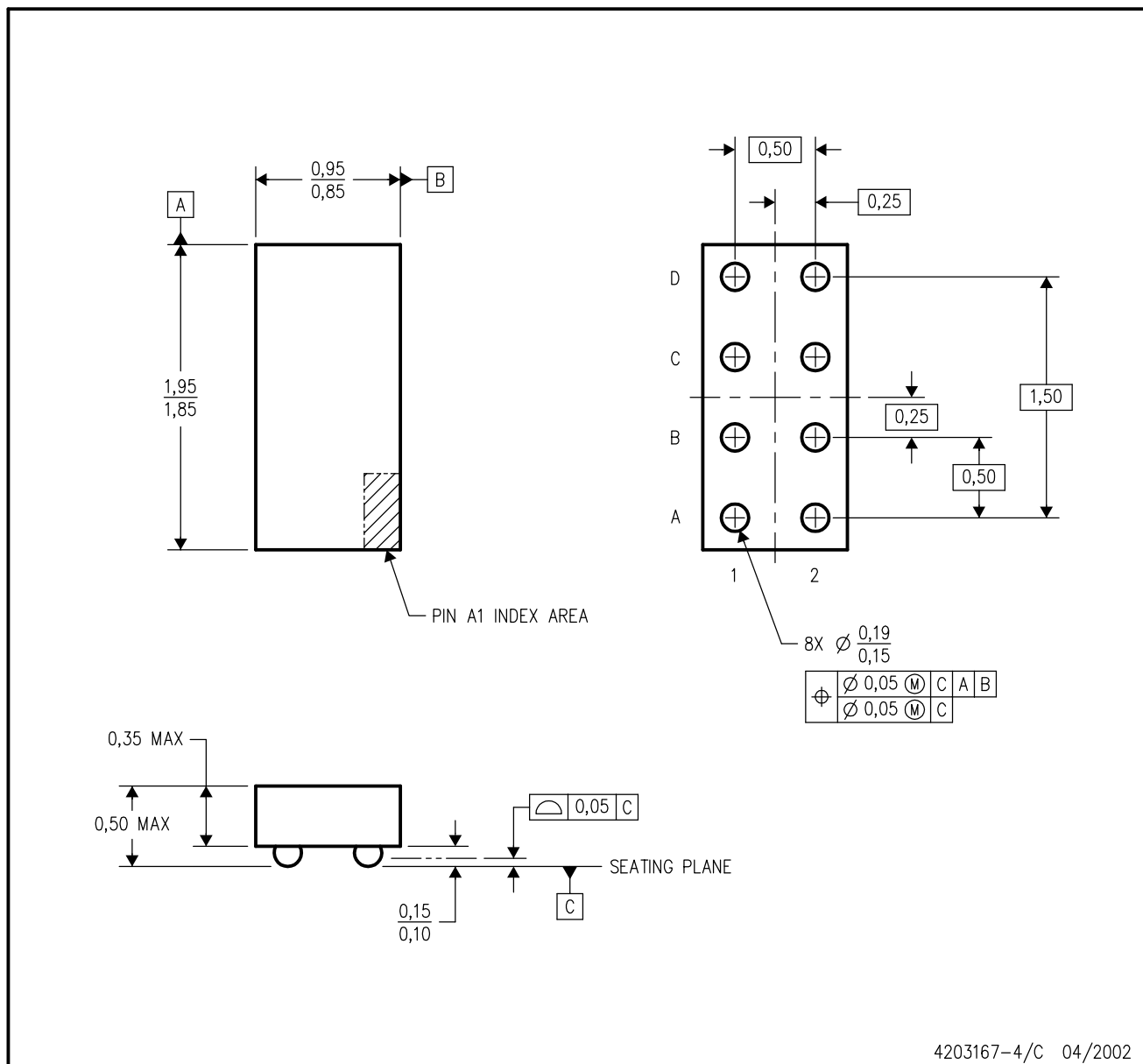
NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
          D.   Falls within JEDEC MO−187 variation CA.

YEA (R−XBGA−N8)

DIE−SIZE BALL GRID ARRAY

0,95
0,85

A

B

1,95
1,85

PIN A1 INDEX AREA

0,50

0,25

D

C

B

A

1,50

0,25

0,50

1   2

8X ⌀ 0,19
0,15

⊕ | ⌀ 0,05 Ⓜ | C | A | B
  | ⌀ 0,05 Ⓜ | C

0,35 MAX

0,50 MAX

⌒ | 0,05 | C

SEATING PLANE

0,15
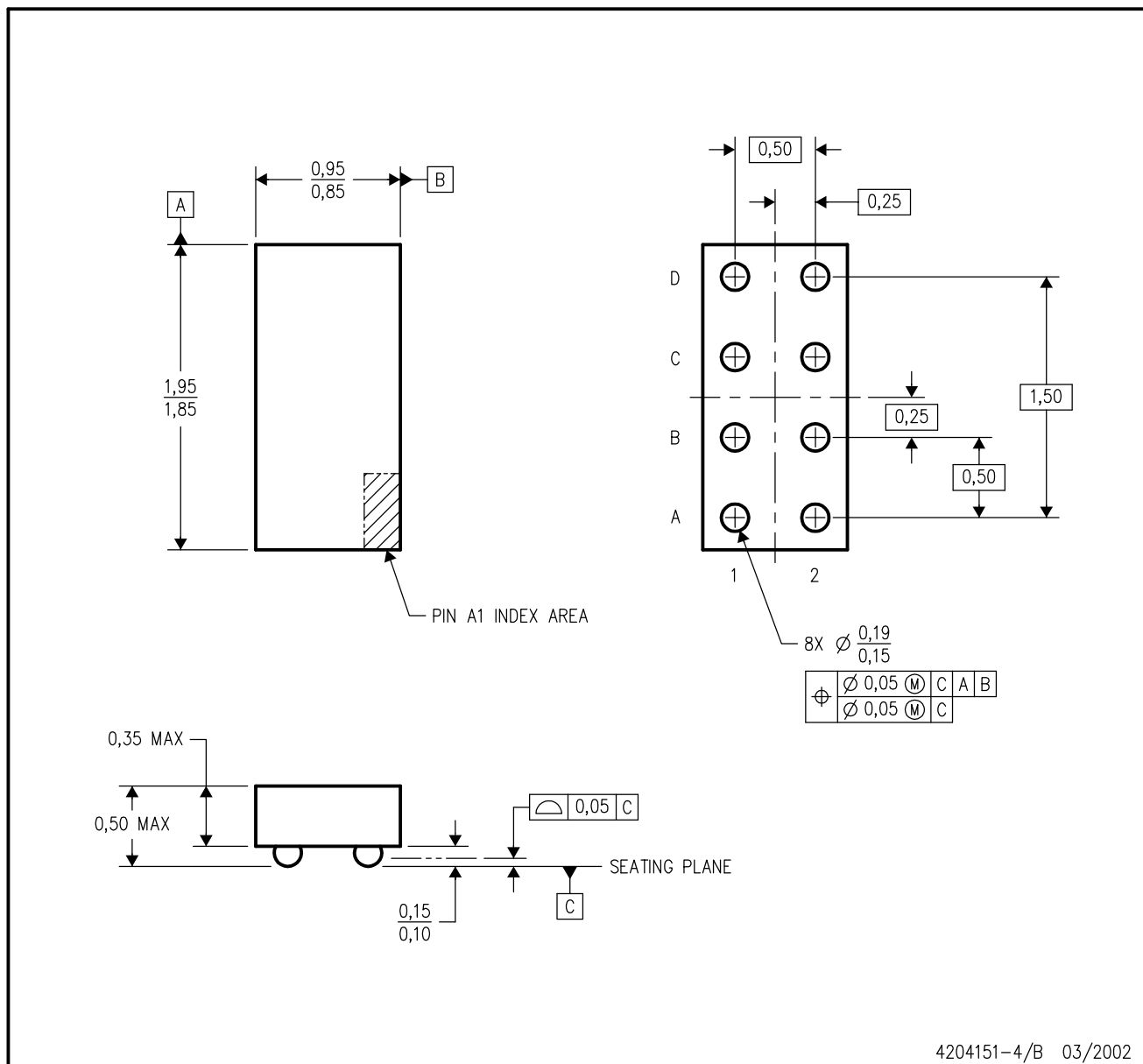0,10

C

4203167−4/C 04/2002

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   NanoStar™ package configuration.
         D.   Package complies to JEDEC MO−211 variation EB.
         E.   This package is tin−lead (SnPb). Refer to the 8 YZA package (drawing 4204151) for lead−free.

NanoStar is a trademark of Texas Instruments.

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www.ti.com

YZA (R−XBGA−N8)   DIE−SIZE BALL GRID ARRAY

0,95 / 0,85

B

A

1,95 / 1,85

PIN A1 INDEX AREA

0,50

0,25

D

C

B

A

1   2

1,50

0,25

0,50

8X Ø 0,19 / 0,15

⊕ | Ø 0,05 Ⓜ | C | A | B
  | Ø 0,05 Ⓜ | C

0,35 MAX

0,50 MAX

0,05 C

SEATING PLANE

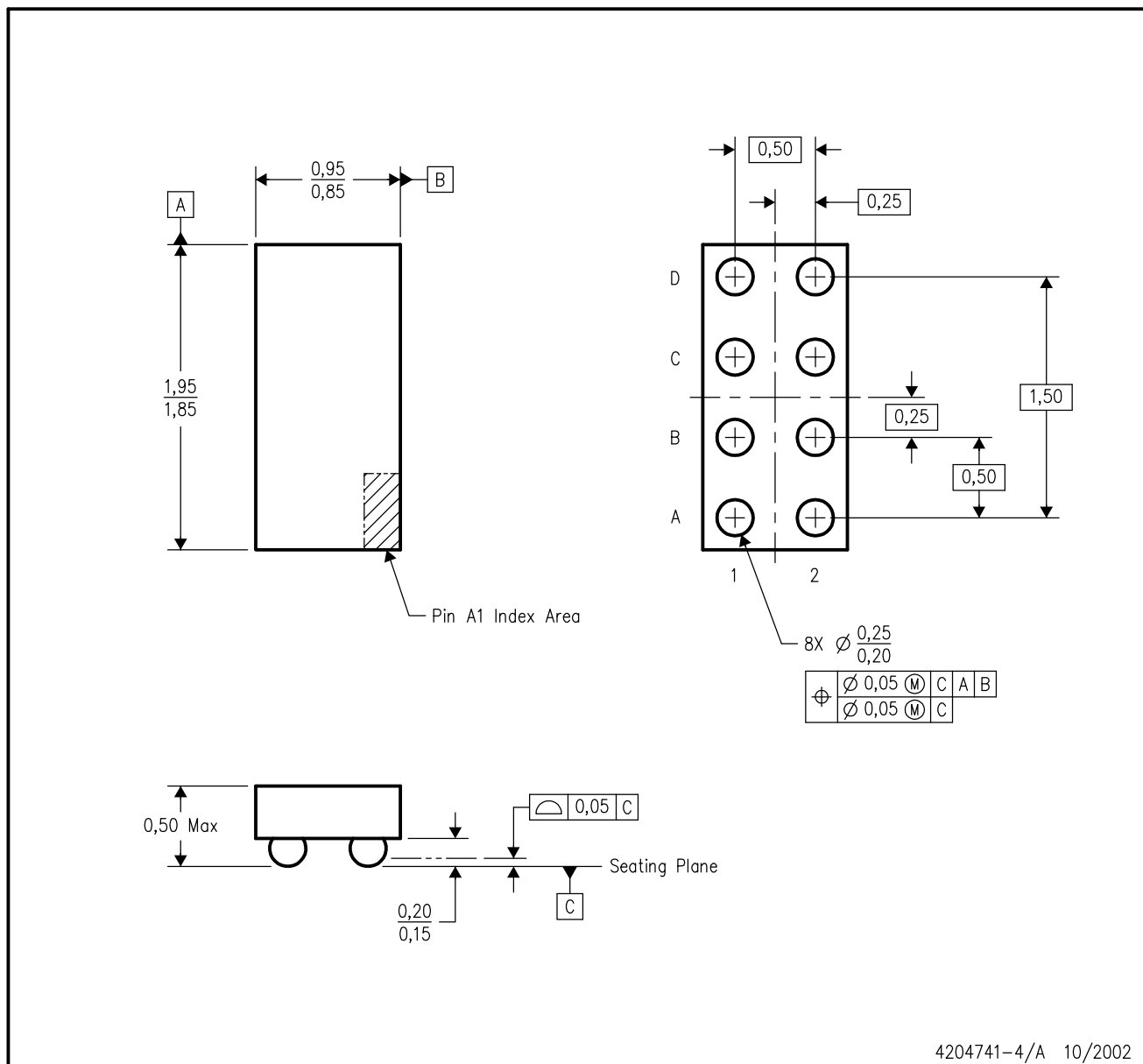0,15 / 0,10

C

4204151−4/B   03/2002

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. NanoFree™ package configuration.
        D. Package complies to JEDEC MO−211 variation EB.
        E. This package is lead−free. Refer to the 8 YEA package (drawing 4203167) for tin−lead (SnPb).
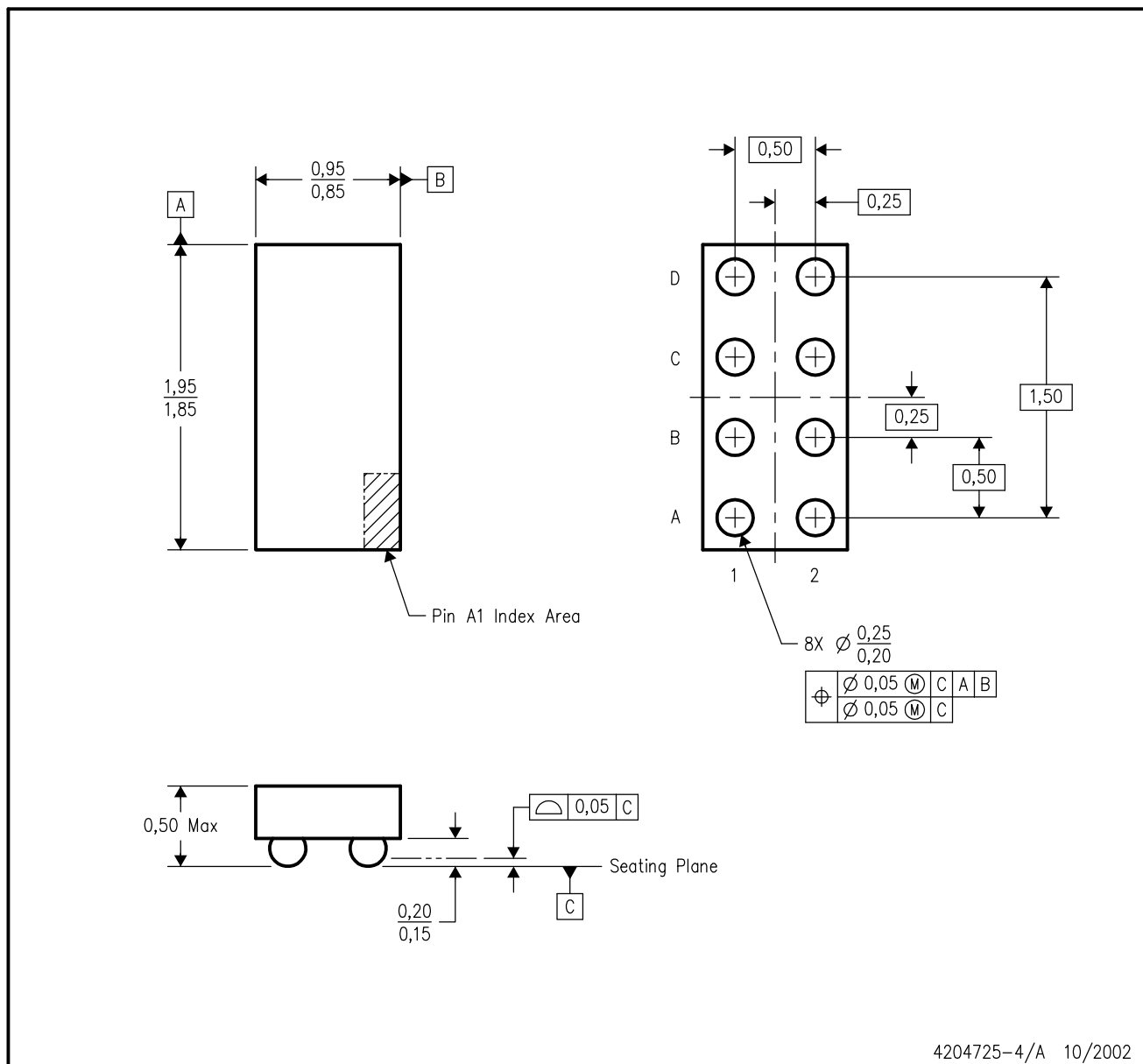
NanoFree is a trademark of Texas Instruments.

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YZP (R−XBGA−N8)   DIE−SIZE BALL GRID ARRAY

0,95 / 0,85 B

A

1,95 / 1,85

Pin A1 Index Area

0,50

0,25

D C B A

1   2

1,50

0,25

0,50

8X ⌀ 0,25 / 0,20

⌖ ⌀ 0,05 Ⓜ C A B
⌀ 0,05 Ⓜ C

0,50 Max

Seating Plane

0,20 / 0,15

⌒ 0,05 C

C

4204741−4/A 10/2002

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. NanoFree™ package configuration.
        D. This package is lead−free. Refer to the 8 YEP package (drawing 4204725) for tin−lead (SnPb).

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TEXAS INSTRUMENTS
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YEP (R−XBGA−N8)   DIE−SIZE BALL GRID ARRAY

$\frac{0,95}{0,85}$ B

A

$\frac{1,95}{1,85}$

Pin A1 Index Area

0,50

0,25

D

C

B

A

1   2

1,50

0,25

0,50

8X Ø $\frac{0,25}{0,20}$

⊕ | Ø 0,05 Ⓜ | C | A | B
  | Ø 0,05 Ⓜ | C

0,50 Max

△ 0,05 C

Seating Plane

$\frac{0,20}{0,15}$

C

4204725−4/A 10/2002

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. NanoStar™ package configuration.
         D. This package is tin−lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead−free.

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Mailing Address: Texas Instruments

Post Office Box 655303 Dallas, Texas 75265