Two 1-Bit, 10MHz, 2nd-Order Delta-Sigma Modulators

FEATURES

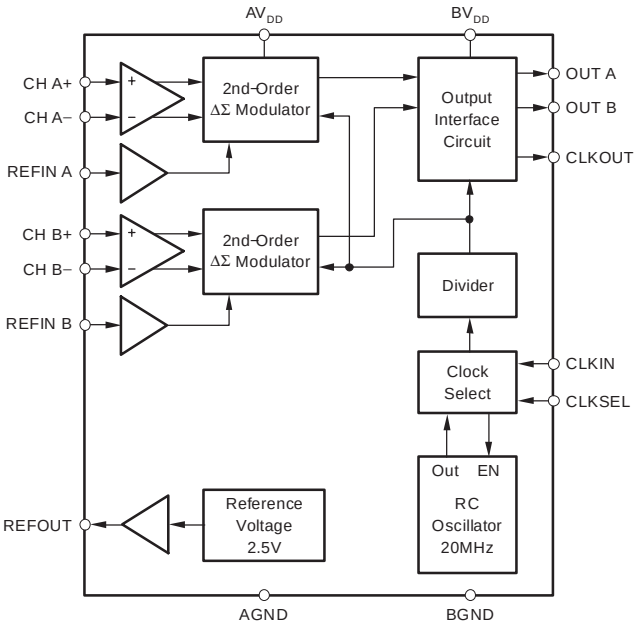
- 16-Bit Resolution
- 14-Bit Linearity
- ±2.5V Input Range at 2.5V
- Internal Reference Voltage: 2%
- Gain Error: 0.5%
- Two Independent Delta-Sigma Modulators
- Two Input Reference Buffers
- On-Chip 20MHz Oscillator
- Selectable Internal or External Clock
- Operating Temperature Range: −40°C to +85°C
- QFN-24 (4x4) Package

APPLICATIONS

- Motor Control
- Current Measurement
- Industrial Process Control
- Instrumentation
- Resolver

DESCRIPTION

The ADS1205 is a two-channel, high-performance, delta-sigma (ΔΣ) modulator with more than 98dB dynamic range, operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers in an industrial environment. With the appropriate digital filter and modulator rate, the device can be used to achieve 16-bit analog-to-digital (A/D) conversion with no missing codes. Effective resolution of 14 bits can be obtained with a digital filter bandwidth of 40kHz at a modulator rate of 10MHz. The ADS1205 is designed for use in high-resolution measurement applications including current measurements, smart transmitters, industrial process control, and resolvers. It is available in a QFN-24 (4x4) package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Package/Ordering Information

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	ADS1205	UNIT
Supply voltage, AGND to AV_{DD}	−0.3 to 6	V
Supply voltage, BGND to BV_{DD}	−0.3 to 6	V
Analog input voltage with respect to AGND	AGND − 0.3 to AV_{DD} + 0.3	V
Reference input voltage with respect to AGND	AGND − 0.3 to AV_{DD} + 0.3	V
Digital input voltage with respect to BGND	BGND − 0.3 to BV_{DD} + 0.3	V
Ground voltage difference, AGND to BGND	±0.3	V
Voltage differences, BV_{DD} to AGND	−0.3 to 6	V
Input current to any pin except supply	±10	mA
Power dissipation	See Dissipation Rating table	
Operating virtual junction temperature range, T_J	−40 to +150	°C
Operating free-air temperature range, T_A	−40 to +85	°C
Storage temperature range, T_{STG}	−65 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$(1)	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
QFN-24 (4x4)	2193mW	21.929mW/°C	1206mW	877.2mW

(1) This is the inverse of the traditional junction-to-ambient thermal resistance ($R_{\theta JA}$). Thermal resistances are not production tested and are for informational purposes only.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, AGND to AV_{DD}		4.5	5	5.5	V
Supply voltage, BGND to BV_{DD}	Low-Voltage Levels	2.7		3.6	V
	5V Logic Levels	4.5	5	5.5	V
Reference input voltage		0.5	2.5	2.6	V
Operating common-mode signal	−IN		2.5		V
Analog inputs	+IN − (−IN)			±0.8 × REFIN	V
External clock(1)		16	20	24	MHz
Operating junction temperature range, T_J		−40		105	°C

(1) With reduced accuracy, clock can go from 1MHz up to 33MHz; see Typical Characteristics.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature range at −40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1205I MIN	ADS1205I TYP(1)	ADS1205I MAX	UNITS
Resolution			16			Bits
DC Accuracy						
INL	Integral linearity error(2)			−1.4	±3	LSB
				−0.002	±0.005	% FSR
	Integral linearity match				6	LSB
					0.009	% FSR
DNL	Differential nonlinearity(3)				±1	LSB
V_{OS}	Input offset error(4)			−1.2	±3	mV
	Input offset error match			0.1	2	mV
TCV_{OS}	Input offset error drift			1.1	8	µV/°C
G_{ERR}	Gain error(4)	Referenced to V_{REF}		−0.01	±0.5	% FSR
	Gain error match			0.09	0.5	% FSR
TCG_{ERR}	Gain error drift			1.3		ppm/°C
PSRR	Power-supply rejection ratio	4.75V < AV_{DD} < 5.25V		78		dB
Analog Input						
FSR	Full-scale differential range	(CH x+) − (CH x−); CH x− = 2.5V			±2.5	V
	Specified differential range	(CH x+) − (CH x−); CH x− = 2.5V			±2	V
	Maximum operating input range(3)		0		AV_{DD}	V
	Input capacitance	Common-mode		3		pF
	Input leakage current	CLK turned off			±1	nA
	Differential input resistance			100		kΩ
	Differential input capacitance			2.5		pF
CMRR	Common-mode rejection ratio	At DC		108		dB
		V_{IN} = ±1.25V_{PP} at 40kHz		117		dB
BW	Bandwidth	FS sine wave, −3dB		50		MHz
Sampling Dynamics						
	Internal clock frequency	CLKSEL = 1	8	9.8	12	MHz
CLKIN	External clock frequency(5)	CLKSEL = 0	1	20	24	MHz
AC Accuracy						
THD	Total harmonic distortion	V_{IN} = ±2V_{PP} at 5kHz		−96.6	−88	dB
SFDR	Spurious-free dynamic range	V_{IN} = ±2V_{PP} at 5kHz	92	98		dB
SNR	Signal-to-noise ratio	V_{IN} = ±2V_{PP} at 5kHz	86	88.9		dB
SINAD	Signal-to-noise + distortion	V_{IN} = ±2V_{PP} at 5kHz	85	88.2		dB
	Channel-to-channel isolation(3)	V_{IN} = ±2V_{PP} at 50kHz		100		dB
ENOB	Effective number of bits		14	14.5		Bits

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for CH x+ = −2V to +2V at 2.5V, expressed either as the number of LSBs or as a percent of measured input range (4V).
(3) Ensured by design.
(4) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(5) With reduced accuracy, the clock frequency can go from 1MHz to 33MHz.
(6) Applicable for 5.0V nominal supply: BV_{DD} (min) = 4.5V and BV_{DD} (max) = 5.5V.
(7) Applicable for 3.0V nominal supply: BV_{DD} (min) = 2.7V and BV_{DD} (max) = 3.6V.

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at −40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1205I MIN	ADS1205I TYP(1)	ADS1205I MAX	UNITS
Voltage Reference Output						
V_{REFOUT}	Reference voltage output	−40°C to +85°C	2.450	2.5	2.550	V
dV_{REFOUT}/dT	Output voltage temperature drift			±20		ppm/°C
	Output voltage noise	f = 0.1Hz to 10Hz, C_L = 10µF		10		µVrms
		f =10Hz to 10kHz, C_L = 10µF		12		µVrms
PSRR	Power-supply rejection ratio			60		dB
I_{OUT}	Output current			10		µA
I_{SC}	Short-circuit current			0.5		mA
	Turn-on settling time	to 0.1% at C_L = 0		100		µs
Voltage Reference Input						
V_{IN}	Reference voltage input		0.5	2.5	2.6	V
	Reference input resistance			100		MΩ
	Reference input capacitance			5		pF
	Reference input current				1	µA
Digital Inputs(6)						
	Logic family		CMOS with Schmitt Trigger			
V_{IH}	High-level input voltage		0.7×BV_{DD}		BV_{DD}+0.3	V
V_{IL}	Low-level input voltage		−0.3		0.3×BV_{DD}	V
I_{IN}	Input current	V_I = BV_{DD} or GND			±50	nA
C_I	Input capacitance			5		pF
Digital Outputs(6)						
	Logic family		CMOS			
V_{OH}	High-level output voltage	BV_{DD} = 4.5V, I_{OH} = −100µA	4.44			V
V_{OL}	Low-level output voltage	BV_{DD} = 4.5V, I_{OL} = +100µA			0.5	V
C_O	Output capacitance			5		pF
C_L	Load capacitance				30	pF
	Data format		Bit Stream			

(1) All typical values are at T_A = +25°C.
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ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating free-air temperature range at −40°C to +85°C, AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS1205I MIN	ADS1205I TYP(1)	ADS1205I MAX	UNITS
Digital Inputs(7)						
	Logic family			LVCMOS		
V_{IH}	High-level input voltage	BV_{DD} = 3.6V	2		BV_{DD}+0.3	V
V_{IL}	Low-level input voltage	BV_{DD} = 2.7V	−0.3		0.8	V
I_{IN}	Input current	V_I = BV_{DD} or GND			±50	nA
C_I	Input capacitance			5		pF
Digital Outputs(7)						
	Logic family			LVCMOS		
V_{OH}	High-level output voltage	BV_{DD} = 2.7V, I_{OH} = −100µA	BV_{DD}−0.2			V
V_{OL}	Low-level output voltage	BV_{DD} = 2.7V, I_{OL} = +100µA			0.2	V
C_O	Output capacitance			5		pF
C_L	Load capacitance				30	pF
	Data format			Bit Stream		
Power Supply						
AV_{DD}	Analog supply voltage		4.5		5.5	V
BV_{DD}	Buffer I/O supply voltage	Low-voltage levels	2.7		3.6	V
		5V logic levels	4.5		5.5	V
AI_{DD}	Analog operating supply current	CLKSEL = 1		11.8	16	mA
		CLKSEL = 0		11.4	15.5	mA
BI_{DD}	Buffer I/O operating supply current	BV_{DD} = 3V, CLKOUT = 10MHz			2	mA
		BV_{DD} = 5V, CLKOUT = 10MHz			2	mA
	Power dissipation	CLKSEL = 0		57	77.5	mW
		CLKSEL = 1		59	80	mW

(1) All typical values are at T_A = +25°C.
(2) Integral nonlinearity is defined as the maximum deviation of the line through the end points of the specified input range of the transfer curve for CH x+ = −2V to +2V at 2.5V, expressed either as the number of LSBs or as a percent of measured input range (4V).
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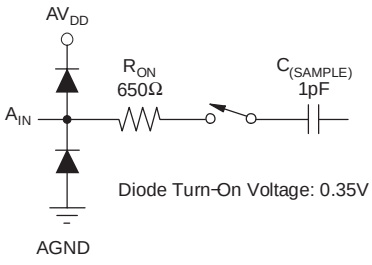
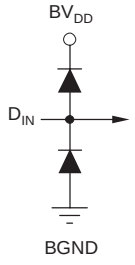
EQUIVALENT INPUT CIRCUIT



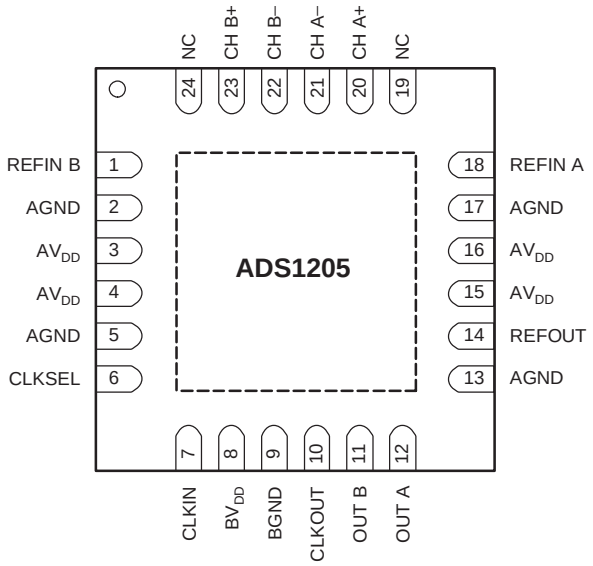
Equivalent Analog Input Circuit



Equivalent Digital Input Circuit

PIN ASSIGNMENTS

RGE PACKAGE
QFN−24
(TOP VIEW)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
REFIN B	1	I	Reference voltage input of channel B: pin for external reference voltage
AGND	2, 5, 13, 17		Analog ground
AV_{DD}	3, 4, 15, 16		Analog power supply; nominal 5V
CLKSEL	6	I	Clock select between internal clock (CLKSEL = 1) or external clock (CLKSEL = 0)
CLKIN	7	I	External clock input
BV_{DD}	8		Digital interface power supply; from 2.7V to 5.5V
BGND	9		Interface ground
CLKOUT	10	O	System clock output
OUT B	11	O	Bit stream from channel B modulator
OUT A	12	O	Bit stream from channel A modulator
REFOUT	14	O	Reference voltage output: output pin of the internal reference source; nominal 2.5V
REFIN A	18	I	Reference voltage input of channel A: pin for external reference voltage
NC	19, 24		No connection; this pin is left unconnected
CH A+	20	I	Analog input of channel A: noninverting input
CH A−	21	I	Analog input of channel A: inverting input
CH B−	22	I	Analog input of channel B: inverting input
CH B+	23	I	Analog input of channel B: noninverting input

PARAMETER MEASUREMENT INFORMATION

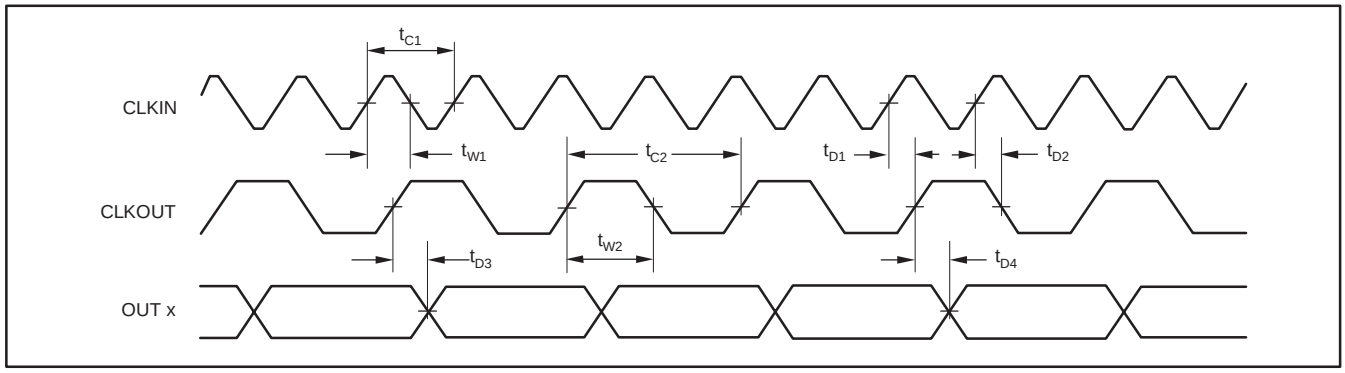


Figure 1. ADS1205 Timing Diagram

TIMING REQUIREMENTS(1)

over recommended operating free-air temperature range at −40°C to +85°C, AV_{DD} = 5V, and BV_{DD} = 2.7 to 5V, unless otherwise noted.

PARAMETER		MIN	MAX	UNIT
t_{C1}	CLKIN period: (CLKSEL = 0)	41.6(2)	1000	ns
t_{W1}	CLKIN high time: (CLKSEL = 0)	10	t_{C1} − 10	ns
t_{C2}	CLKOUT period using internal oscillator (CLKSEL = 1)	83	125	ns
	CLKOUT period using external clock (CLKSEL = 0)	$2 \times t_{C1}$		ns
t_{W2}	CLKOUT high time	$(t_{C2}/2) - 5$	$(t_{C2}/2) + 5$	ns
t_{D1}	CLKOUT rising edge delay after CLKIN rising edge: (CLKOUT = 0)	0	10	ns
t_{D2}	CLKOUT falling edge delay after CLKIN rising edge: (CLKOUT = 0)	0	10	ns
t_{D3}	Data valid delay after rising edge of CLKOUT (CLKSEL = 1)	$(t_{C2}/4) - 8$	$(t_{C2}/4) + 8$	ns
t_{D4}	Data valid delay after rising edge of CLKOUT (CLKSEL = 0)	$t_{W1} - 3$	$t_{W1} + 7$	ns

(1) All input signals are specified with $t_R = t_F$ = 5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$. See Figure 1.
(2) With reduced accuracy, the minimum clock period can go down to 30ns.

TYPICAL CHARACTERISTICS

AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

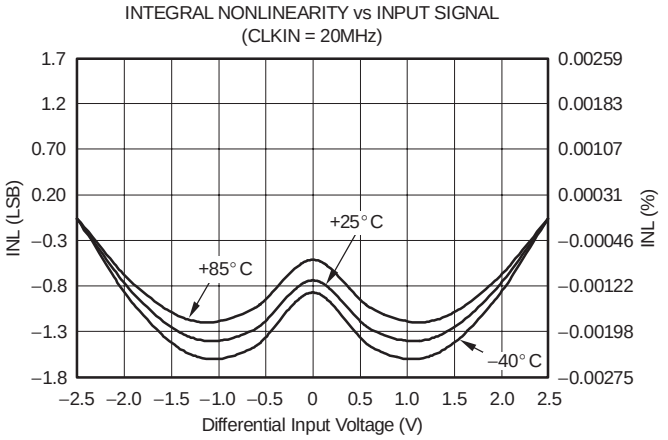


Figure 2

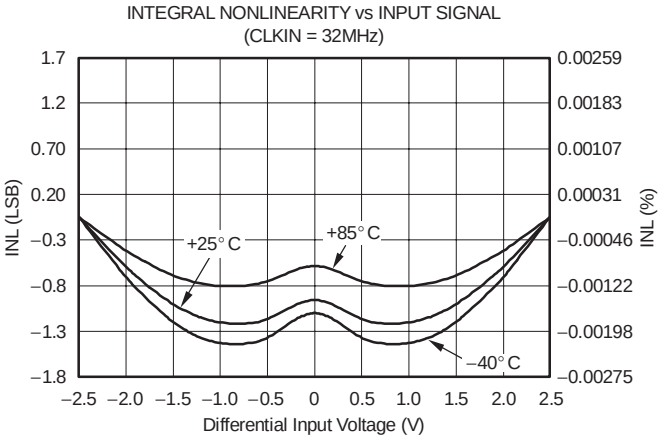


Figure 3

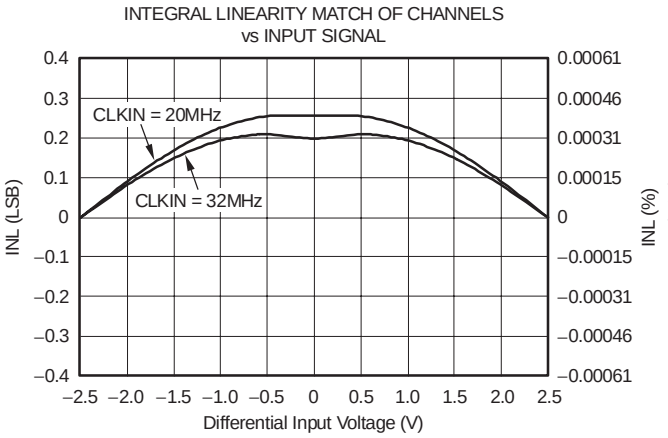


Figure 4

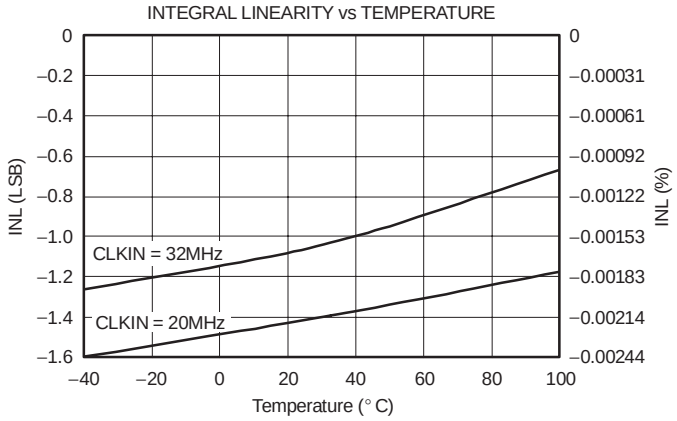


Figure 5

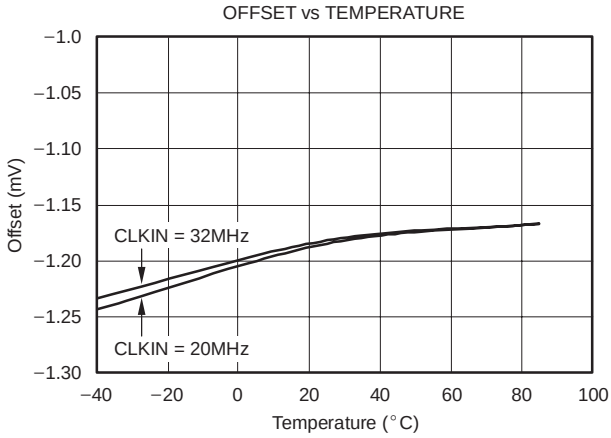


Figure 6

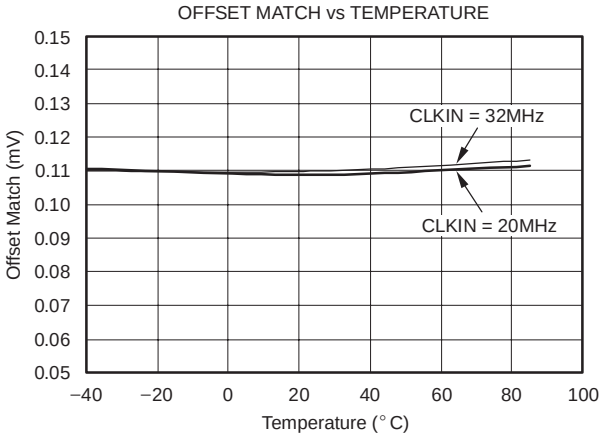


Figure 7

TYPICAL CHARACTERISTICS (continued)

AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

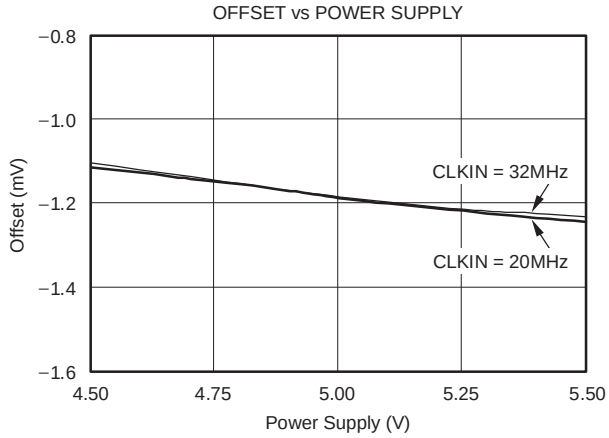


Figure 8

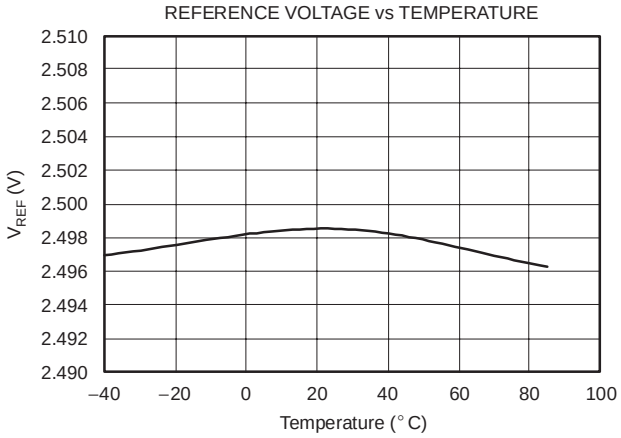


Figure 9

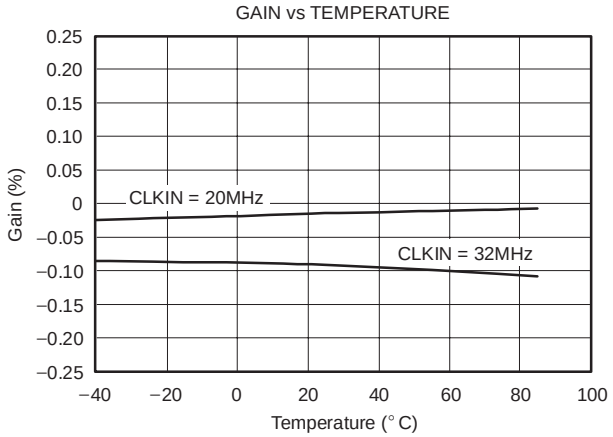


Figure 10

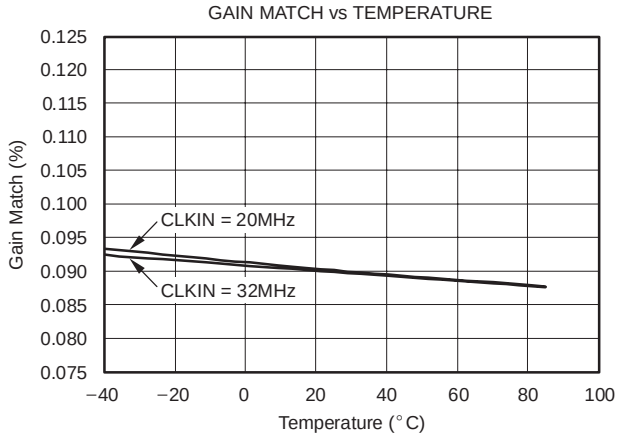


Figure 11

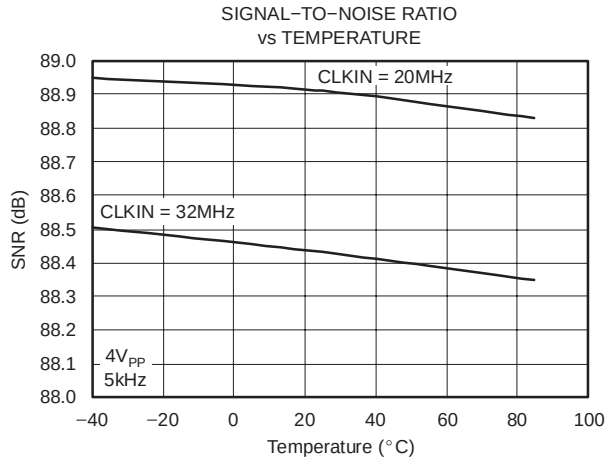


Figure 12

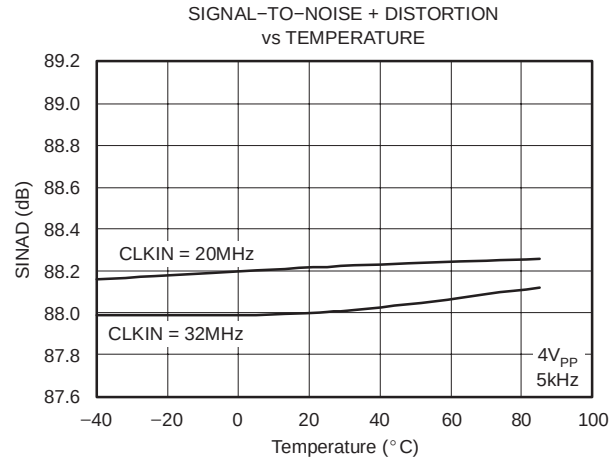


Figure 13

TYPICAL CHARACTERISTICS (continued)

AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs TEMPERATURE
(CLKIN = 20MHz)

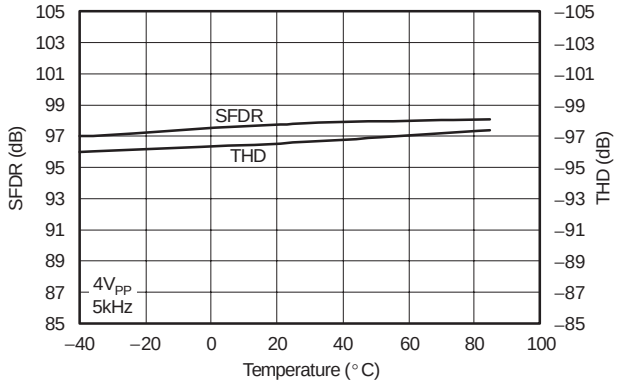


Figure 14

SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs TEMPERATURE
(CLKIN = 32MHz)

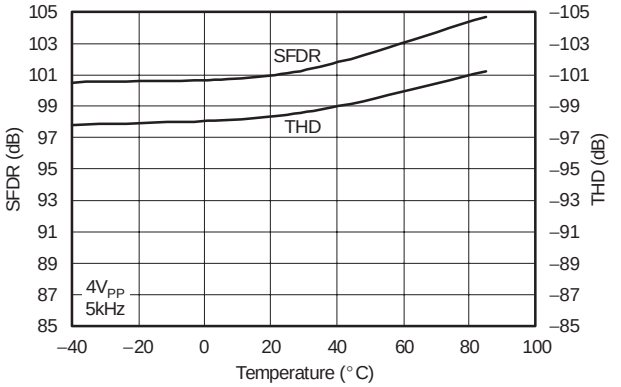


Figure 15

SIGNAL−TO−NOISE AND DISTORTION AND
SIGNAL−TO−NOISE RATIO vs INPUT FREQUENCY
(CLKIN = 20MHz)

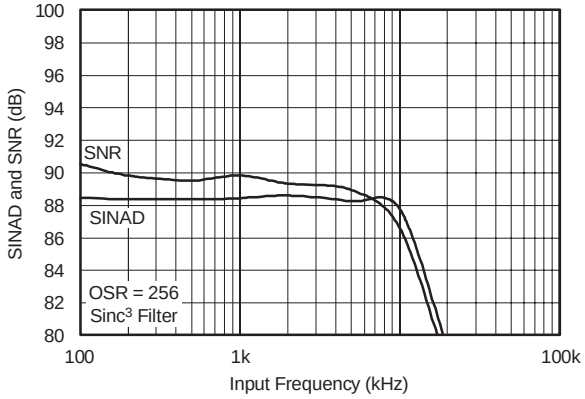


Figure 16

SIGNAL−TO−NOISE AND DISTORTION AND
SIGNAL−TO−NOISE RATIO vs INPUT FREQUENCY
(CLKIN = 32MHz)

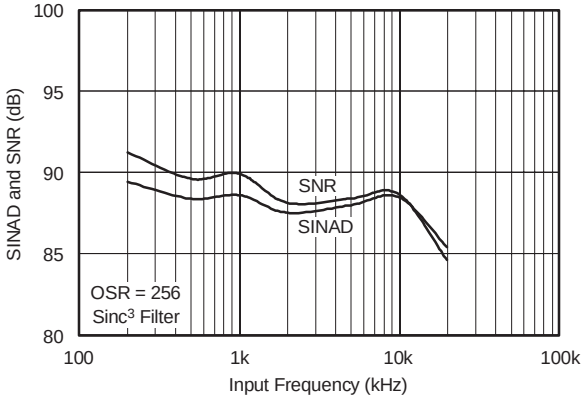


Figure 17

SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY
(CLKIN = 20MHz)

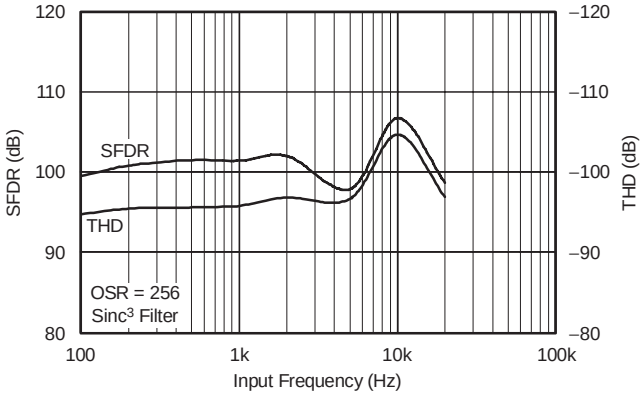


Figure 18

SPURIOUS FREE DYNAMIC RANGE AND
TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY
(CLKIN = 32MHz)

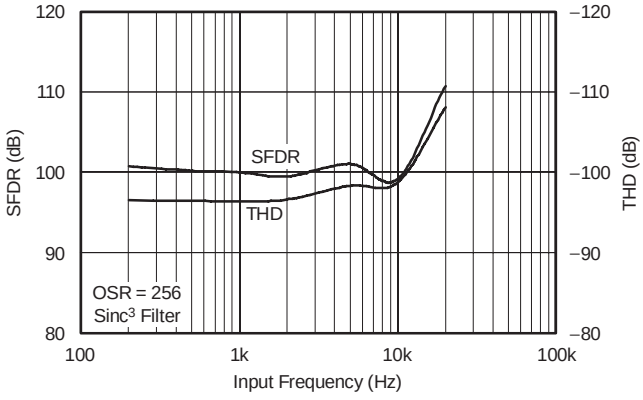


Figure 19

TYPICAL CHARACTERISTICS (continued)

AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

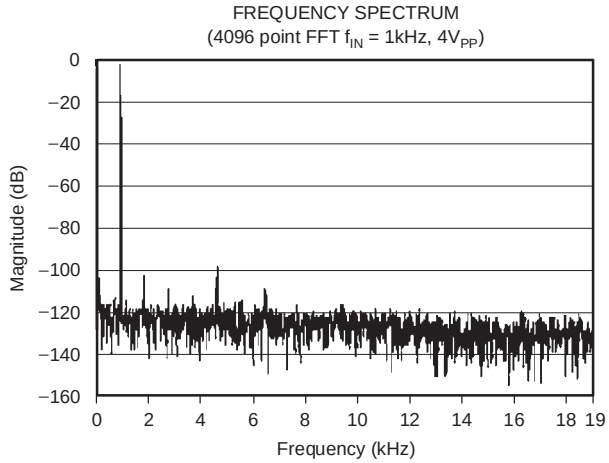


Figure 20

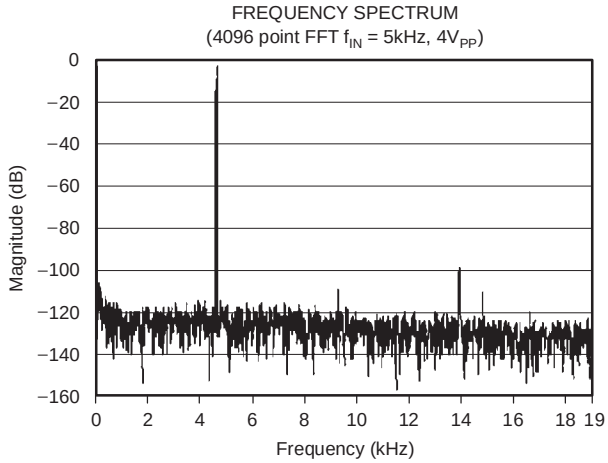


Figure 21

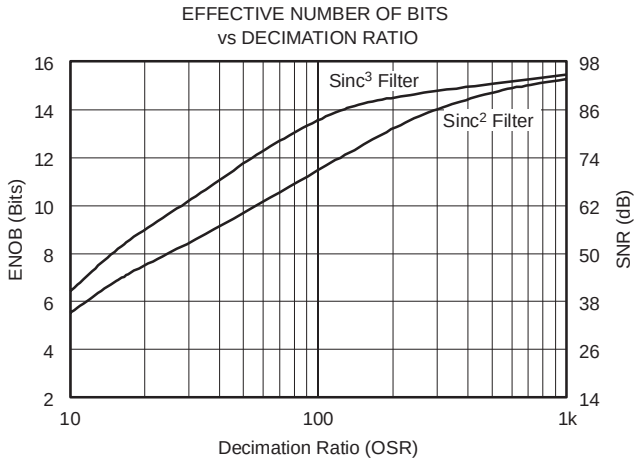


Figure 22

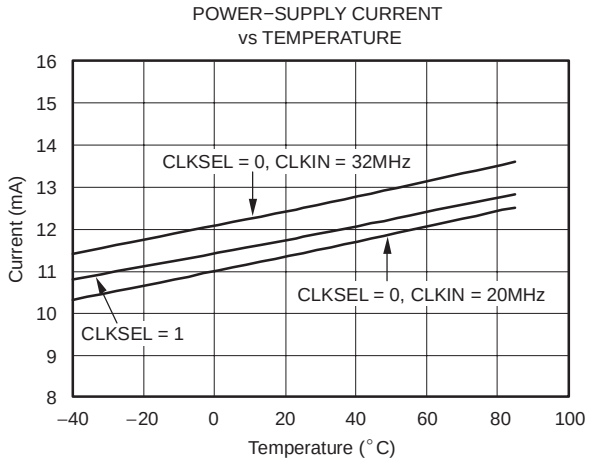


Figure 23

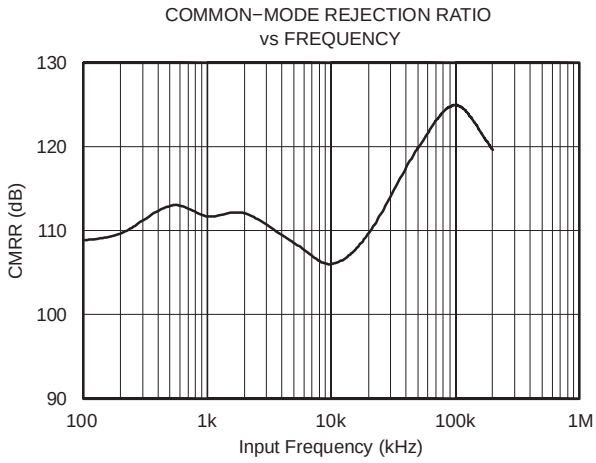


Figure 24

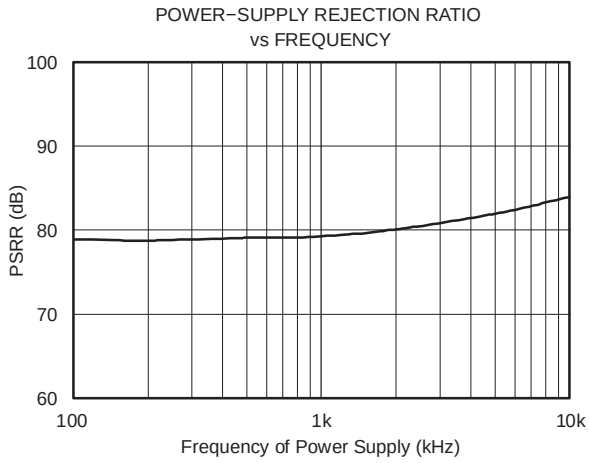


Figure 25

TYPICAL CHARACTERISTICS (continued)

AV_{DD} = 5V, BV_{DD} = 3V, CH x+ = 0.5V to 4.5V, CH x− = 2.5V, REFIN = REFOUT = internal +2.5V, CLKIN = 20MHz, and 16-bit $Sinc^3$ filter with decimation by 256, unless otherwise noted.

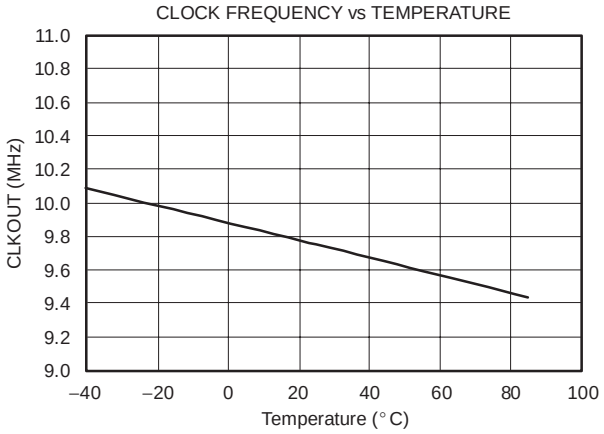


Figure 26

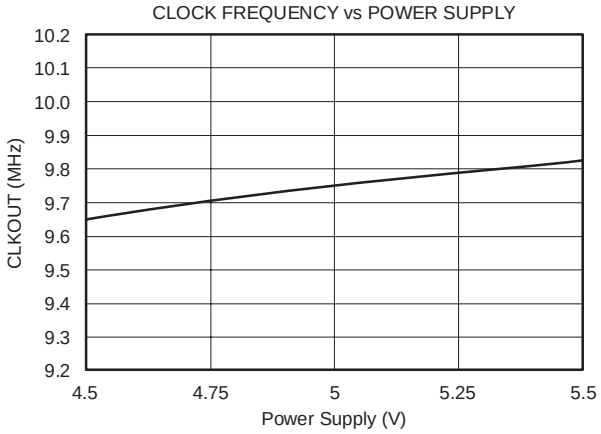


Figure 27

GENERAL DESCRIPTION

The ADS1205 is a two-channel, 2nd-order, CMOS device with two delta-sigma modulators, designed for medium- to high-resolution A/D signal conversions from DC to 39kHz (filter response −3dB) if an oversampling ratio (OSR) of 64 is chosen. The output of the converter (OUT_X) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage.

The modulator shifts the quantization noise to high frequencies. A low-pass digital filter should be used at the output of the delta-sigma modulator. The filter serves two functions. First, it filters out high-frequency noise. Second, the filter converts the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation).

An application-specific integrated circuit (ASIC) or field-programmable gate array (FPGA) could be used to implement the digital filter. Figure 28 and Figure 29 show typical application circuits with the ADS1205 connected to an FPGA or ASIC.

The overall performance (that is, speed and accuracy) depends on the selection of an appropriate OSR and filter type. A higher OSR produces greater output accuracy while operating at a lower refresh rate. Alternatively, a lower OSR produces lower output accuracy, but operates at a higher refresh rate. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range exceeding 98dB with an OSR = 256.

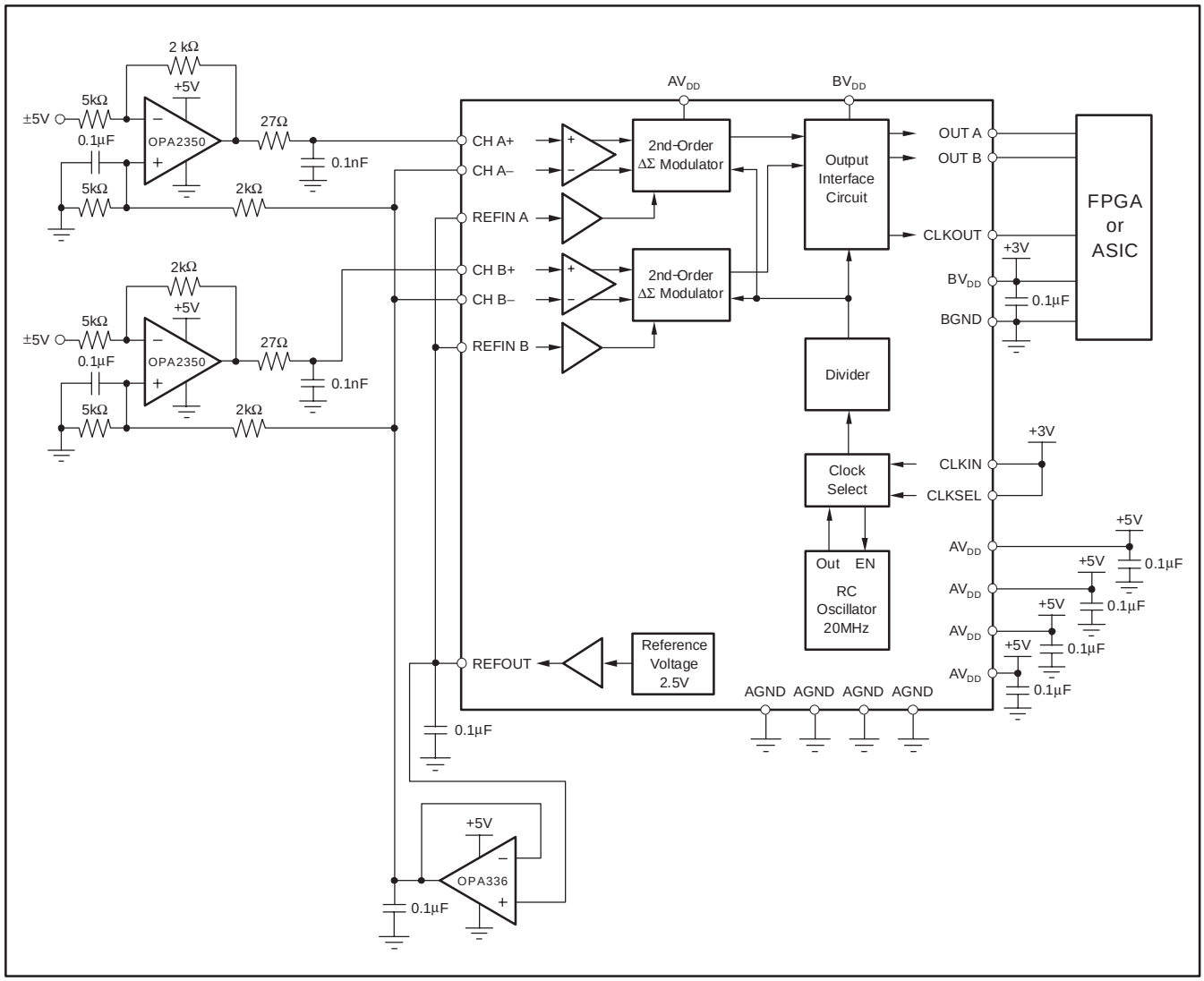


Figure 28. Single-Ended Connection Diagram for the ADS1205 Delta-Sigma Modulator

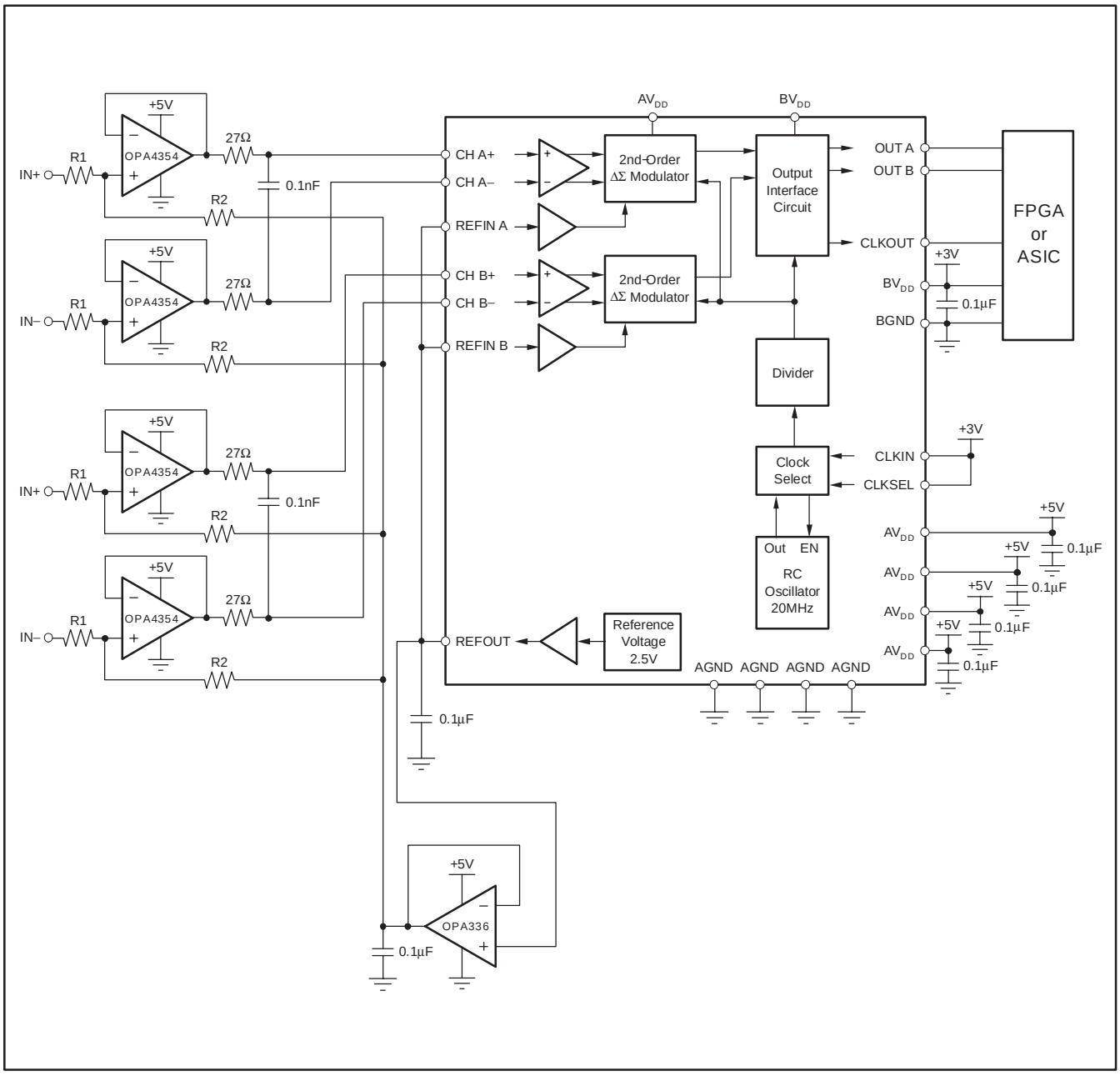


Figure 29. Differential Connection Diagram for the ADS1205 Delta-Sigma Modulator

THEORY OF OPERATION

The differential analog input of the ADS1205 is implemented with a switched-capacitor circuit. This circuit implements a 2nd-order modulator stage, which digitizes the analog input signal into a 1-bit output stream. The clock source can be internal as well as external. Different frequencies for this clock allow for a variety of solutions and signal bandwidths. Every analog input signal is continuously sampled by the modulator and compared to a reference voltage that is applied to the REFINx pin. A digital stream, which accurately represents the analog input voltage over time, appears at the output of the corresponding converter.

ANALOG INPUT STAGE

Analog Input

The topology of the analog inputs of ADS1205 is based on a fully differential switched-capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (108dB), and excellent power-supply rejection.

The input impedance of the analog input is dependent on the modulator clock frequency (f_{CLK}), which is also the sampling frequency of the modulator. Figure 30 shows the basic input structure of one channel of the ADS1205. The relationship between the input impedance of the ADS1205 and the modulator clock frequency is:

$$Z_{IN} = \frac{100k\Omega}{f_{MOD}/10MHz} \quad (1)$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is high. This high impedance may cause degradation in gain, linearity, and THD. The importance of this effect depends on the desired system performance. There are two restrictions on the analog input signals, CH x+ and CH x−. If the input voltage exceeds the range (GND – 0.3V) to (V_{DD} + 0.3V), the input current must be limited to 10mA because the input protection diodes on the front end of the converter will begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog voltage resides within ±2V (with V_{REF} as a midpoint); however, the FSR input voltage is ±2.5V.

Modulator

The ADS1205 can be operated in two modes. When CKLSEL = 1, the two modulators operate using the internal clock, which is fixed at 20MHz. When CKLSEL = 0, the modulators operate using an external clock. In both modes, the clock is divided by two internally and functions as the modulator clock. The frequency of the external clock can vary from 1MHz to 33MHz to adjust for the clock requirements of the application.

The modulator topology is fundamentally a 2nd-order, switched-capacitor, delta-sigma modulator, such as the one conceptualized in Figure 31. The analog input voltage and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing analog voltages at X2 and X3. The voltages at X2 and X3 are presented to their individual integrators. The output of these integrators progresses in a negative or positive direction. When the value of the signal at X4 equals the comparator reference voltage, the output of the comparator switches from negative to positive, or positive to negative, depending on its original state. When the output value of the comparator switches from high to low or vice versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators forces the value of the integrator output to track the average of the input.

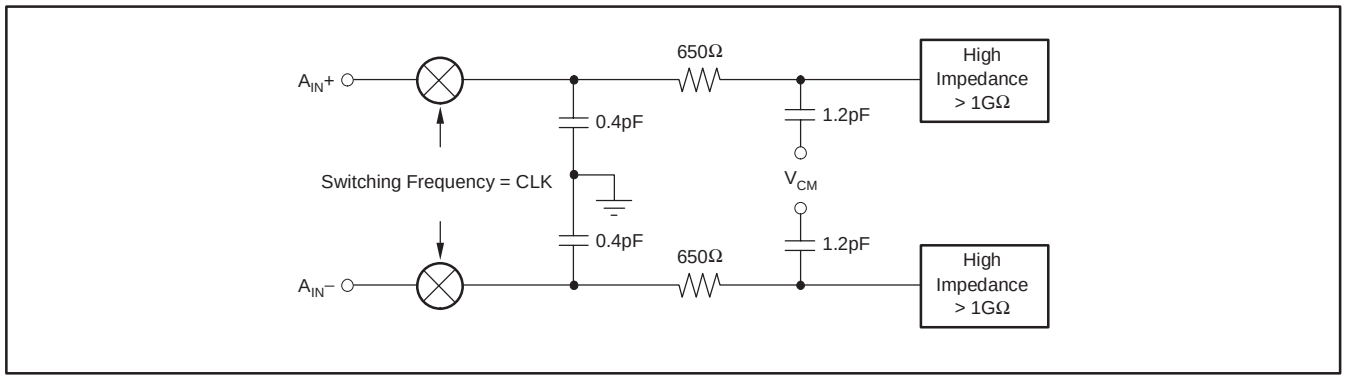


Figure 30. Input Impedance of the ADS1205

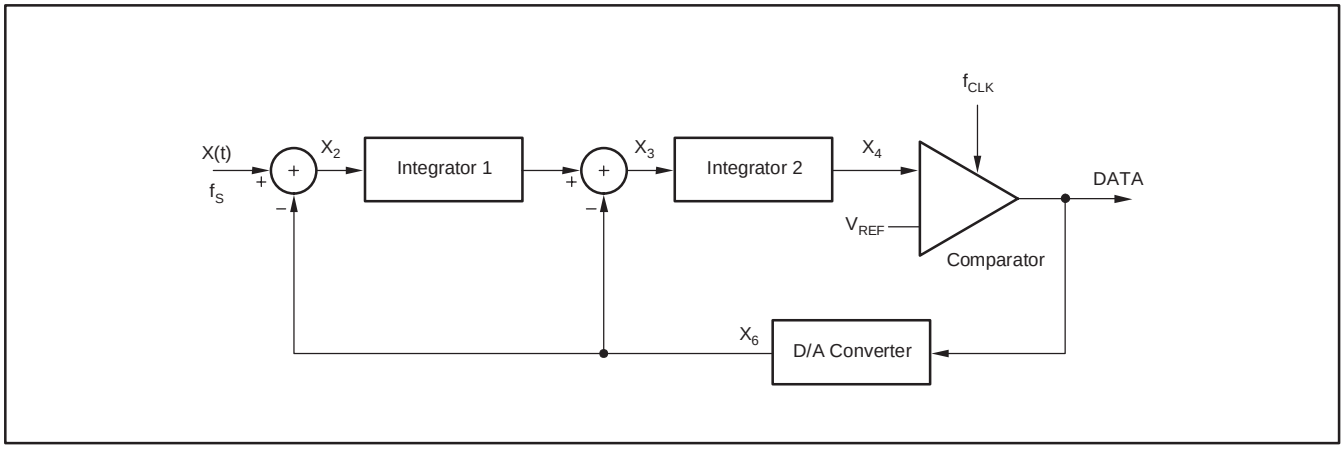


Figure 31. Block Diagram of the 2nd-Order Modulator

DIGITAL OUTPUT

A differential input signal of 0V will ideally produce a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of +2V produces a stream of ones and zeros that are high 80% of the time. A differential input of –2V produces a stream of ones and zeros that are high 20% of the time. The input voltage versus the output modulator signal is shown in Figure 32.

DIGITAL INTERFACE

INTRODUCTION

The analog signal connected to the input of the delta-sigma modulator is converted using the clock signal applied to the modulator. The result of the conversion, or modulation, is generated and sent to the OUTx pin from the delta-sigma modulator. In most applications where a direct connection is realized between the delta-sigma modulator and an ASIC or FPGA (each with an implemented filter), the two standard signals per modulator (CLKOUT and OUTx) are provided from the modulator. The output clock signal is equal for both modulators. If CLKSEL = 1, CLKIN must always be set either high or low.

MODES OF OPERATION

The system clock of the ADS1205 is 20MHz by default. The system clock can be provided either from the internal 20MHz RC oscillator or from an external clock source. For this purpose, the CLKIN pin is provided; it is controlled by the mode setting, CLKSEL.

The system clock is divided by two for the modulator clock. Therefore, the default clock frequency of the modulator is 10MHz. With a possible external clock range of 1MHz to 33MHz, the modulator operates between 500kHz and 16.5MHz.

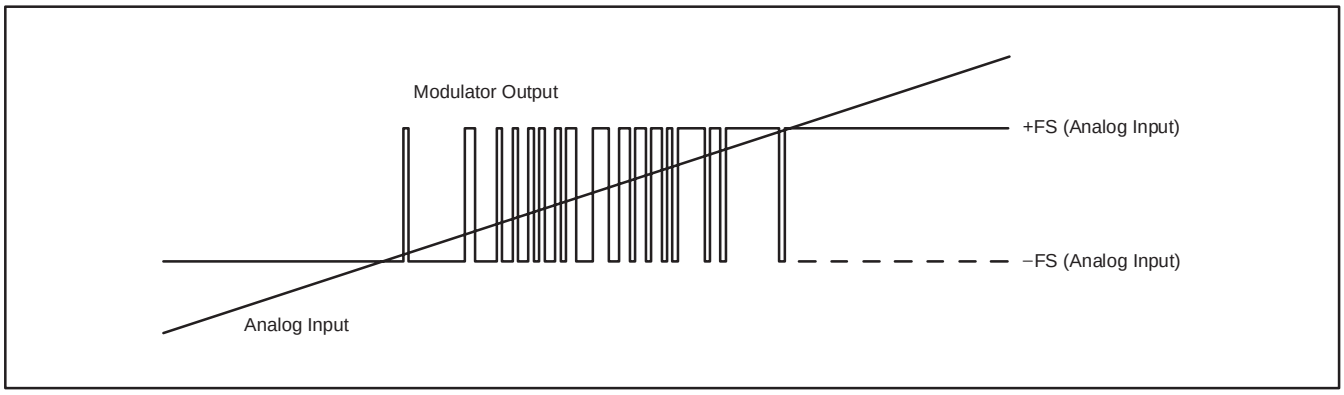


Figure 32. Analog Input vs Modulator Output of the ADS1205

FILTER USAGE

The modulator generates only a bitstream, which does not output a digital word like an A/D converter. In order to output a digital word equivalent to the analog input voltage, the bitstream must be processed by a digital filter.

A very simple filter, built with minimal effort and hardware, is the Sinc^3 filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (for example, a count of digital gates). For oversampling ratios in the range of 16 to 256, this is a good choice. All the characterizations in the data sheet are also done using a Sinc^3 filter with an oversampling ratio of OSR = 256 and an output word length of 16 bits.

In a Sinc^3 filter response (shown in Figure 33 and Figure 34), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3dB point is located at half the Nyquist frequency or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type for better frequency response.

This performance can be improved, for example, by a cascaded filter structure. The first decimation stage can be a Sinc^3 filter with a low OSR and the second stage a high-order filter.

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

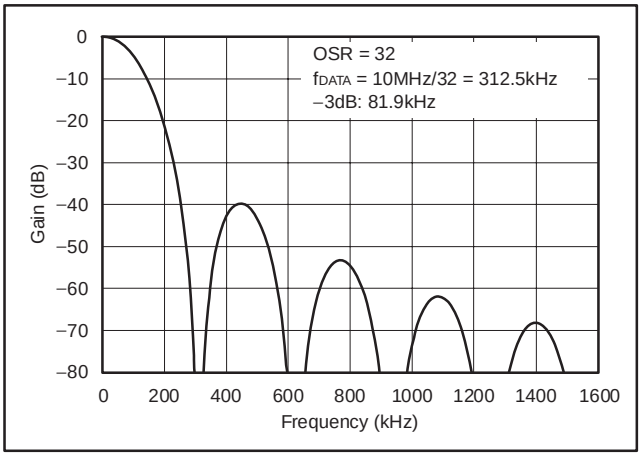


Figure 33. Frequency Response of Sinc^3 Filter

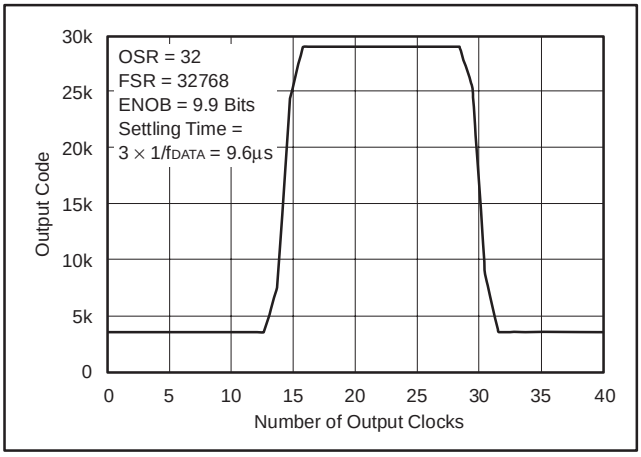


Figure 34. Pulse Response of Sinc^3 Filter (f_{MOD} = 10MHz)

The effective number of bits (ENOB) can be used to compare the performance of ADCs and delta-sigma modulators. Figure 35 shows the ENOB of the ADS1205 with different filter types. In this data sheet, the ENOB is calculated from the SNR:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (3)$$

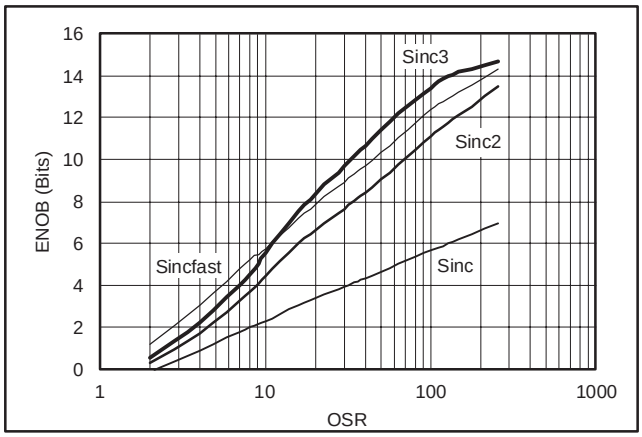


Figure 35. Measured ENOB vs OSR

In motor control applications, a very fast response time for overcurrent detection is required. There is a constraint between 1µs and 5µs with 3 bits to 7 bits resolution. The time for full settling is dependent on the filter order. Therefore, the full settling of the $Sinc^3$ filter needs three data clocks and the $Sinc^2$ filter needs two data clocks. The data clock is equal to the modulator clock divided by the OSR. For overcurrent protection, filter types other than $Sinc^3$ might be a better choice. A simple example is a $Sinc^2$ filter. The Sincfast is a modified $Sinc^2$ filter:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 \left(1 + z^{-2 \times OSR}\right) \quad (4)$$

Figure 36 compares the settling time of different filter types operating with a 10MHz modulator clock.

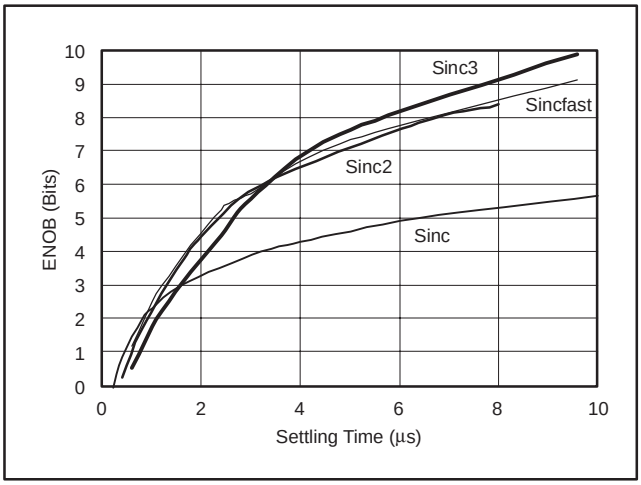


Figure 36. Measured ENOB vs Settling Time

For more information, see application note SBAA094, *Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications*, available for download at www.ti.com.

LAYOUT CONSIDERATIONS

POWER SUPPLIES

An applied external digital filter rejects high-frequency noise. PSRR and CMRR improve at higher frequencies because the digital filter suppresses high-frequency noise. However, the suppression of the filter is not infinite, so high-frequency noise still influences the conversion result.

Inputs to the ADS1205, such as CH x+, CH x−, and CLKIN, should not be present before the power supply is on. Violating this condition could cause latch-up. If these signals are present before the supply is on, series resistors should be used to limit the input current to a maximum of 10mA. Experimentation may be the best way to determine the appropriate connection between the ADS1205 and different power supplies.

GROUNDING

Analog and digital sections of the design must be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. Do not join the ground planes; instead, connect the two with a moderate signal trace underneath the converter. However, for different applications with DSPs and switching power supplies, this process might be different.

For multiple converters, connect the two ground planes as close as possible to one central location for all of the converters. In some cases, experimentation may be required to find the best point to connect the two planes together.

DECOUPLING

Good decoupling practices must be used for the ADS1205 and for all components in the design. All decoupling capacitors, specifically the 0.1µF ceramic capacitors, must be placed as close as possible to the pin being decoupled. A 1µF and 10µF capacitor, in parallel with the 0.1µF ceramic capacitor, can be used to decouple AV_{DD} to AGND as well as BV_{DD} to BGND. At least one 0.1µF ceramic capacitor must be used to decouple every AV_{DD} to AGND and BV_{DD} to BGND, as well as for the digital supply on each digital component.

The digital supply sets the I/O voltage for the interface and can be set within a range of 2.7V to 5.5V.

In cases where both the analog and digital I/O supplies share the same supply source, an RC filter of 10Ω and 0.1µF can be used to help reduce the noise in the analog supply.

PACKAGING INFORMATION

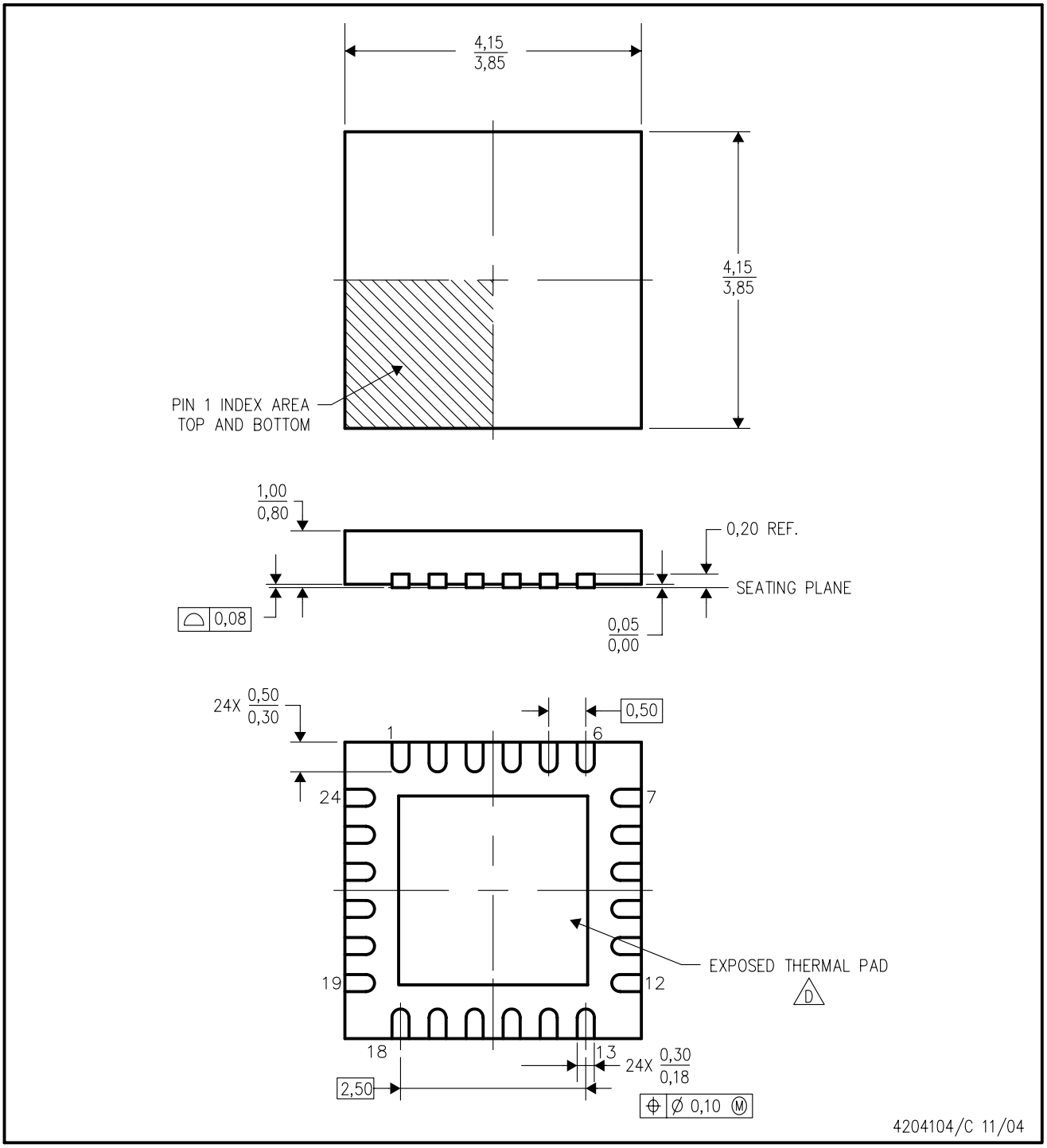
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1205IRGER	ACTIVE	QFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1205IRGERG4	ACTIVE	QFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1205IRGET	ACTIVE	QFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1205IRGETG4	ACTIVE	QFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGE (S–PQFP–N24) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

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