

HA16686MP

Read Pulse Generator

Description

The HA16686MP generates a digital read data signal from the read signal output by a hard disk drive. It is a one-chip version of the HA16676MP read data generator and the HA16663 read pulse generator.

Preamplified signals from the magnetic head are passed through an AGC, then through a filter and differentiator to generate the output signal. A gate signal for the read data is also generated.

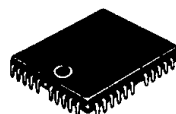
Features

- Transfer rates up to 10 Mbps
- AGC input amplifier ensures stable reproduction independent of media or head type.
- AGC can be disabled when writing
- AGC output can be fixed for servo feedback, and differential amplifier for peak hold detection
- Digital read data output is TTL compatible
- Compact surface-mount package
- Use with the HA16652P/MP, HA16688MP, HA16689MP HDD R/W circuit for compact HDD controller board designs

Ordering Information

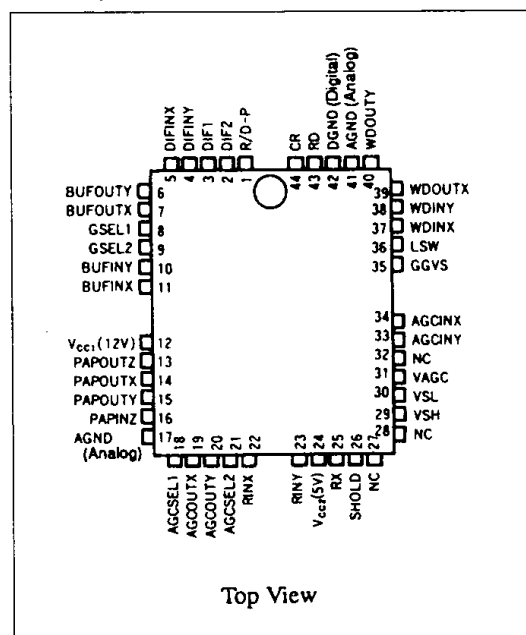
Type No.	Package
HA16686MP	MP-44

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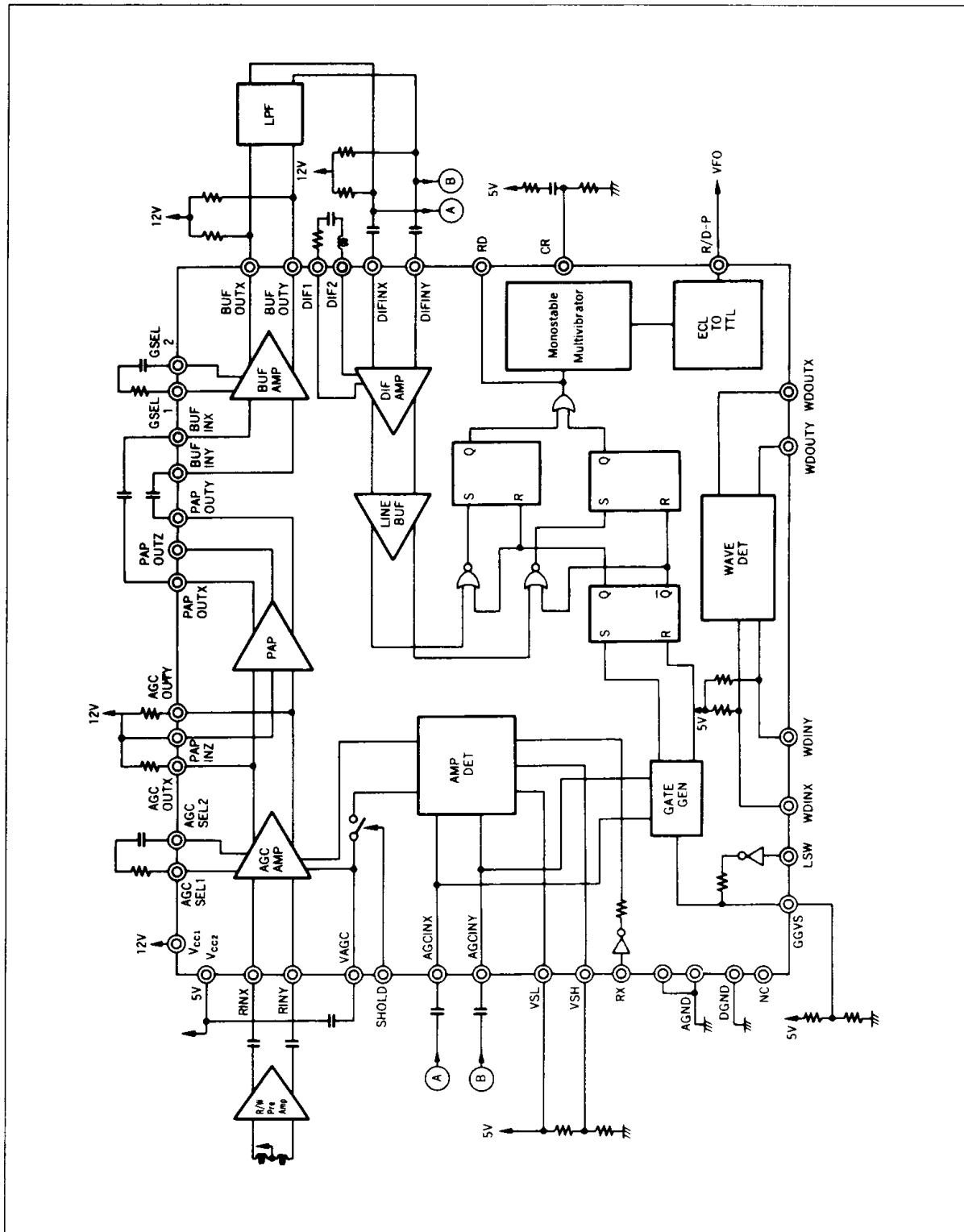


(MP-44)

Pin Assignment



Block Diagram



Pin Descriptions

Type	Pin No.	Name	Function
Power supply	12	V _{CC1}	+12 V power supply (analog)
	24	V _{CC2}	+5 V power supply (digital)
	17, 41	AGND	Analog GND
	42	DGND	Digital GND
Inputs	22	R _{INX}	Differential inputs for read signal from disk drive
	23	R _{INY}	
	10	B _{UFINX}	Differential inputs for buffer amplifier to lowpass filter
	11	B _{UFINX}	
	5	D _{IFINX}	Differential inputs for differentiating amplifier
	4	D _{IFINX}	
	34	A _{GCINX}	Differential inputs for AGC output amplitude detector
	33	A _{GCINX}	
	30	V _{SL}	AGC amplitude detector low-level slice voltage—corresponds to discharge current threshold
	29	V _{SH}	AGC amplitude detector high-level slice voltage—corresponds to charge current threshold
	25	R _X	AGC loop on/off select RX = High: AGC loop off (minimum AGC loop gain) RX = Low: AGC loop on
	26	S _{HOLD}	Constant AGC gain select (low input fixes gain)
	35	G _{GV} S	Gate generator voltage slice level
	36	L _{SW}	G _{GV} S level select (V _{G_{GV}S} lowered by 0.2 V when input is high)
	37	W _{DINX}	Differential inputs for peak hold bandwidth amplifier (internally biased)
	38	W _{DINX}	
Outputs	19	A _G C _{OUTX}	Differential outputs from AGC (open collector)
	20	A _G C _{OUTY}	
	14	P _A P _{OUTX}	Differential outputs from AGC output buffer (emitter follower)
	13	P _A P _{OUTZ}	
	15	P _A P _{OUTY}	
	7	B _U F _{OUTX}	Differential outputs from the LPF buffer amplifier
	6	B _U F _{OUTY}	
	31	V _A G _C	Discharge current from AGC amplitude detector
	16	P _A P _{INZ}	
	39	W _D OUTX	Differential outputs from peak hold bandwidth amplifier (open emitter)
	40	W _D OUTY	
	43	R _D	Read data (ECL)
	1	R/D-P	Read data pulse (TTL): Pulswidth is determined by external CR network
External Components	18	A _G CSEL1	CR network for selecting the gain and lowpass cutoff frequency for the AGC
	21	A _G CSEL2	
	8	GSEL1	CR network for selecting the gain and lowpass cutoff frequency of the LPF buffer amplifier
	9	GSEL2	
	3	DIF1	LCR network for selecting sensitivity and gain of the differentiating amplifier
	2	DIF2	
	44	CR	CR network for selecting the pulswidth of the read data pulse

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Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Rating	Unit	Pins
Power supply voltage	V _{CC1}	15	V	
	V _{CC2}	7	V	
Input voltage	V _{I1}	V _{CC1}	V	PAPINZ
	V _{I2}	5.5	V	SHOLD
	V _{I3}	V _{CC2}	V	RX, VSL, VSH, GGVS, LSW
Output voltage	V _{O1}	V _{CC1}	V	VAGC
Output current	I _{O1}	-10	mA	PAPOUTX, PAPOUTY, PAPOUTZ
	I _{O2}	-2	mA	RD
	I _{O3}	4	mA	R/D-P
	I _{O4}	-440	μA	R/D-P
	I _{O5}	-5	mA	WDOUTX, WDOUTY
	I _{O6}	-30	mA	CR
Differential input voltage	V _{ID1}	500	mV _{p-p}	RINX, RINY
	V _{ID2}	3	V _{p-p}	BUFINX, BUFINY
	V _{ID3}	3	V _{p-p}	DIFINX, DIFINY
	V _{ID4}	3	V _{p-p}	AGCINX, AGCINY
	V _{ID5}	2	V _{p-p}	WDINX, WDINY
Operating temperature	T _{opr}	0 to 70	°C	
Storage temperature	T _{stg}	-55 to 125	°C	
Operating junction temperature	T _{jopr}	150	°C	
Power dissipation	P _T	940	mW	

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Notes:

1. Applies to RX, VSL, VSH, GGVS, and LSW.
2. Applies to PAPOUTX, PAPOUTY, and PAPOUTZ.



Electrical Characteristics

DC Characteristics (Ta = 25°C)

Functional Block	Parameter	Symbol	Min	Typ	Max	Unit	Pins	Test Conditions
Power supplies	Operating power supply voltage 1	V _{CC1}	10.8	12.0	13.2	V	V _{CC1}	
	Operating power supply voltage 2	V _{CC2}	4.5	5.0	5.5	V	V _{CC2}	
	Current consumption 1	I _{CC1}	—	25	33	mA	V _{CC1}	V _{CC1} = 13.2 V, V _{CC2} = 5.5 V
	Current consumption 2	I _{CC2}	—	58	76	mA	V _{CC2}	V _{CC1} = 13.2 V, V _{CC2} = 5.5 V
AGC	Differential input resistance	R _{IA}	—	3	—	kΩ	RINX	
	Input bias voltage	V _{BA}	3.0	3.5	4.0	V	RINY	V _{CC1} = 12 V, V _{CC2} = 5 V
	Differential input offset voltage	V _{OFA}	−130	0	130	mV	AGCOUTX AGCOUTY	
	In-phase output voltage	V _{OCA}	10.6	11.1	11.5	V		V _{CC1} = 12 V
	Output sink current	I _{OSA}	1.6	3	4.6	mA		V _{CC2} = 5 V, R _L = 300 Ω
LPF buffer	Differential input resistance	R _{IB}	—	10	—	kΩ	BUFINX	
	Input bias voltage	V _{BB}	4.35	4.85	5.2	V	BUFINY	V _{CC1} = 12 V, V _{CC2} = 5 V
	Differential output offset voltage	V _{OFB}	−230	0	230	mV	BUFOUTX BUFOUTY	
	In-phase output voltage	V _{OCB}	9.8	10.5	11.2	V		V _{CC1} = 12 V
	Output sink current	I _{OSB}	1.8	3.5	5.5	mA		V _{CC2} = 5 V, R _L = 430 Ω
Differentiating amplifier	Differential input resistance	R _{ID}	—	10	—	kΩ	DIFINX	
	Input bias voltage	V _{BD}	3.4	3.6	3.8	V	DIFINY	V _{CC1} = 12 V, V _{CC2} = 5 V
	Output sink current	I _{OSD}	0.45	0.75	1.4	mA	DIF 1 DIF 2	
AGC controller	Differential input resistance	R _{IC}	—	10	—	kΩ	AGCINX	V _{CC1} = 12 V, V _{CC2} = 5 V
	Input bias voltage	V _{BC}	4.8	4.95	5.2	V	AGCINTY	
	Input bias current	I _{BS}	—	3	12	μA	VSL VSH	
	AGC voltage	V _{AGC}	6.3	7	7.6	V	VAGC	V _{CC1} = 12 V, V _{CC2} = 5 V, R _X = 2.0 V
	Input current when SHOLD = low	I _{IAGC}	—	2.5	5.0	μA		V _{CC1} = 12 V, V _{CC2} = 5 V V _{AGC} = 7 V
	Input high voltage	V _{IH}	2.0	—	—	V	RX	
	Input low voltage	V _{IL}	—	—	0.8	V		
	Input high current	I _{IH}	—	100	300	μA		V _{CC1} = 12 V, V _{CC2} = 5 V, V _{IH} = 2.4 V
	Input low current	I _{IL}	−1.0	−0.2	—	mA		V _{CC1} = 12 V, V _{CC2} = 5 V, V _{IL} = 0.4 V
	Input high voltage	V _{IH}	2.0	—	—	V	SHOLD	V _{CC1} = 12 V, V _{CC2} = 5 V
	Input low voltage	V _{IL}	—	—	0.8	V		
	Input high current	I _{IH}	—	3	10	μA		V _{CC1} = 12 V, V _{CC2} = 5 V, V _{IH} = 2.4 V
	Input low current	I _{IL}	—	0	5	μA		V _{CC1} = 12 V, V _{CC2} = 5 V, V _{IL} = 0.4 V
	Input high voltage	V _{IH}	2.0	—	—	V	LSW	V _{CC1} = 12 V, V _{CC2} = 5 V
	Input low voltage	V _{IL}	—	—	0.8	V		
Gate generator	Input high current	I _{IH}	—	100	300	μA		V _{CC1} = 12 V, V _{CC2} = 5 V, V _{IH} = 2.4 V
	Input low current	I _{IL}	−1.0	−0.2	—	mA		V _{CC1} = 12 V, V _{CC2} = 5 V, V _{IL} = 0.4 V
	Input voltage 1	V _{G1}	—	1.5	—	V	GGVS	V _{CC1} = 12 V, V _{CC2} = 5 V, L _{SW} = 0.4 V
	Input voltage 2	V _{G2}	—	1.3	—	V		V _{CC1} = 12 V, V _{CC2} = 5 V, L _{SW} = 2.0 V
	Output high voltage	V _{OH}	3.9	4.2	4.5	V	RD	V _{CC1} = 12 V, V _{CC2} = 5 V
	Differential input resistance	R _{IW}	—	10	—	kΩ	WDINX WDINY	
	Input bias voltage	V _{BW}	4.8	4.95	5.2	V		V _{CC1} = 12 V, V _{CC2} = 5 V
Peak hold amplifier	In-phase output voltage	V _{OCW}	9.5	10.2	10.9	V	WDOUTX WDOUTY	



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DC Characteristics (cont)

Functional Block	Parameter	Symbol	Min	Typ	Max	Unit	Pins	Test Conditions
Monostable multivibrator	Output high voltage	V_{OH}	3.26	3.53	3.8	V	CR	$V_{CC1} = 12\text{ V}$, $V_{CC2} = 5\text{ V}$
	Output low voltage	V_{OL}	1.7	2	2.48	V		
	Output high voltage	V_{OH}	2.5	3.4	—	V	R/D - P	$V_{CC2} = 4.5\text{ V}$, $I_{OH} = -400\text{ }\mu\text{A}$
	Output low voltage	V_{OL}	—	0.3	0.5	V		$V_{CC2} = 4.5\text{ V}$, $I_{OL} = 2\text{ mA}$
AGC output buffer	Input bias current	I_{BP}	—	7.5	45	μA	PAPINZ	$V_{CC1} = 12\text{ V}$, $V_{CC2} = 5\text{ V}$

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Pins	Test Conditions
Differential voltage gain	A_{VW}	—	6	—	dB	WDOUTX WDOUTY	$f = 1\text{ MHz}$
Bandwidth	BW_W	—	30	—	dB	WDOUTX WDOUTY	$f = 1\text{ MHz}$
Output rise time	t_r	—	7	—	ns	R/D - P	$V_{CC} = 5\text{ V}$, $R_{T1} = 30\text{ }\Omega$
Output fall time	t_f	—	5	—	ns		$R_{T2} = 2.2\text{ k}\Omega$
Output delay time	t_{pdHL}	—	20	—	ns		$C_T = 150\text{ pF}$
Output pulsewidth	t_W	—	50	—	ns		

