National Semiconductor

TP3051, TP3056 Parallel Interface CODEC/Filter COMBO®

General Description

The TP3051, TP3056 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing the A/D and D/A conversion architecture shown in *Figure 1* and a parallel I/O data bus interface. The devices are fabricated using National's advanced double poly microCMOS process.

The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-255 law or A-law PCM format. Auto-zero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads. The TP3051 μ-law and TP3056 A-law devices are pin compatible parallel interface COMBOs for bus-oriented systems.

Features

- Complete CODEC and filtering system including:
  - — Transmit high pass and low pass filtering
  - — Receive low pass filter with sin x/x correction
  - — Receive power amplifier
  - — Active RC noise filters
  - — μ-255 law COder and DECoder—TP3051
  - — A-law COder and DECoder—TP3056
  - — Internal precision voltage reference
  - — Internal auto-zero circuitry
- Meets or exceeds all LSSGR and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- High speed TRI-STATE® data bus
- 2 loopback test modes

Block Diagram

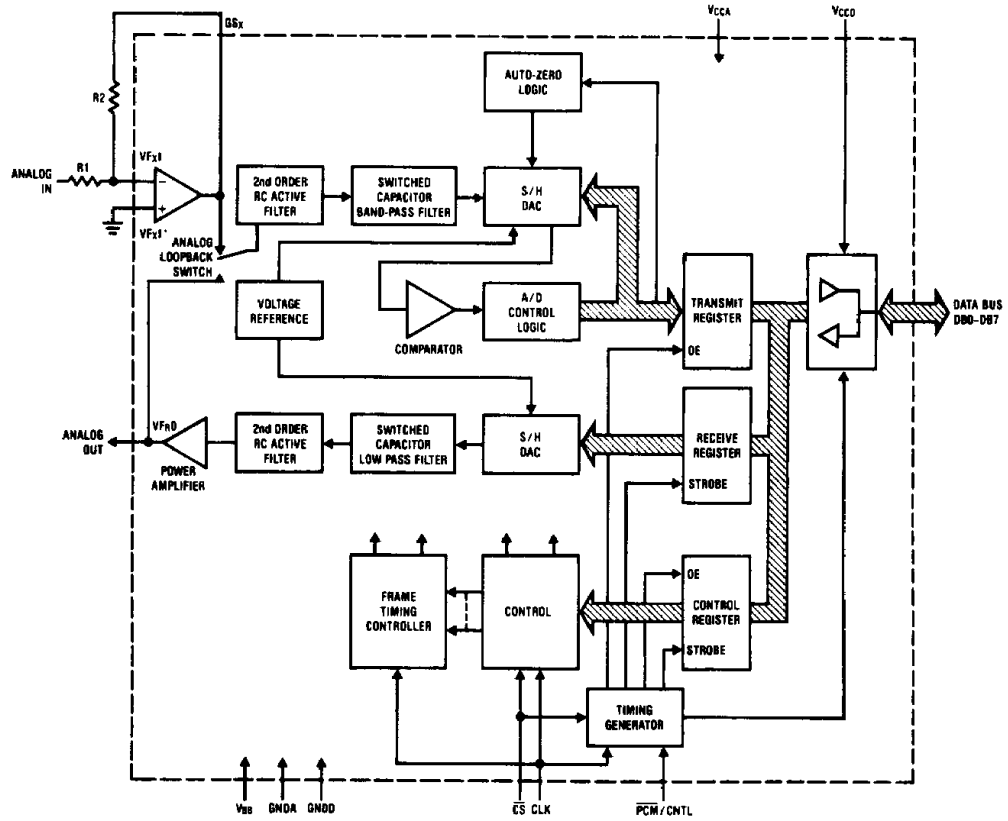

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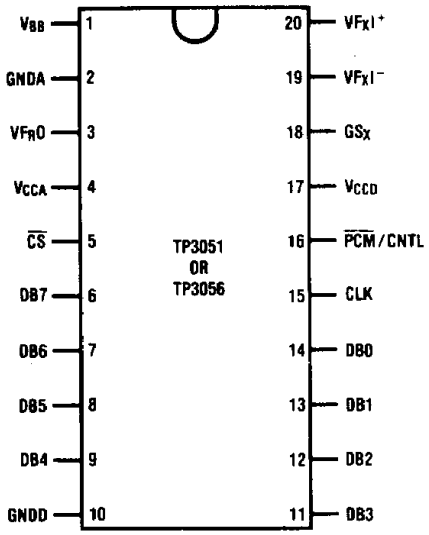
FIGURE 1

Connection Diagrams

Dual-In-Line Package



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Top View

Order Number TP3051J or TP3056J
See NS Package Number J20A

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All analog signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier. This output can drive a 600Ω load to ±2.5V.
V_{CCA}	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5V \pm 5\%$. Must be connected to V_{CCD}.
$\overline{CS}$	Device chip select input which controls READ, WRITE and TRI-STATE® operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
DB7	Bit 7 I/O on the data bus. The PCM LSB.
DB6	Bit 6 I/O on the data bus.
DB5	Bit 5 I/O on the data bus.
DB4	Bit 4 I/O on the data bus.
GNDD	Digital ground. All digital signals are referenced to this pin.
DB3	Bit 3 I/O on the data bus.
DB2	Bit 2 I/O on the data bus.
DB1	Bit 1 I/O on the data bus.
DB0	Bit 0 I/O on the data bus. This is the PCM sign bit.
CLK	The clock input for the switched-capacitor filters and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.

Symbol	Function
$\overline{PCM}$/CNTL	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	Positive power supply pin for the bus drivers. $V_{CCD} = 5V \pm 5\%$. Must be connected to V_{CCA}.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

CLOCK AND DATA BUS CONTROL

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table I and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/$\overline{WRITE}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in *Figures 4a* and *4b*.

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0–DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The TP3051, TP3056 is powered-up via a command to the control register (see Control Register Functions). This sets

Functional Description (Continued)

the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

TABLE I. Control Bit Functions

Control Bits	Function
C0, C1	Select Clock Frequency **C0 C1 Frequency** 0 X 1.024 MHz 1 0 0.768 MHz or 0.772 MHz 1 1 1.28 MHz
C2, C3	Digital and Analog Loopback **C2 C3 Mode** 1 X digital loopback 0 1 analog loopback 0 0 normal
C4	Power-Down/Power-Up (Note 1) 1 = power-down 0 = power-up
C5	TP3051—Don't care (Note 1) TP3056 1 = Not implemented. Do not use. 0 = A-law with even bit inversion
C6–C7	Don't Care (Note 1)

Note 1: These bits are always set to logical "1" when reading back the control register.

DATA BUS NOMENCLATURE

The normal order for serial PCM transmission is sign bit first, whereas the normal order for serial data is LSB first. The parallel data bus is defined as follows:

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

READING THE BUS

If CLK is low when $\overline{CS}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched on the negative-going transition. If $\overline{PCM}$/CNTL is low during the falling $\overline{CS}$ transition, then the bus data is defined as PCM voice data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame, i.e., at an 8 kHz rate.

If $\overline{PCM}$/CNTL is high during the falling $\overline{CS}$ transition, the bus data is latched into the control register. This does not affect frame synchronization.

WRITING THE BUS

If CLK is high when $\overline{CS}$ goes low, at the next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated onto the bus, depending on the level of $\overline{PCM}$/CNTL at the $\overline{CS}$ transition. If $\overline{PCM}$/CNTL is low during the $\overline{CS}$ falling transition, the transmit register data is written to the bus.

An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame; i.e., at an 8 kHz rate.

If $\overline{PCM}$/CNTL is high during the $\overline{CS}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

CONTROL REGISTER FUNCTIONS

Writing to the control register allows the user to set the various operating states of the TP3051 and TP3056. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select

   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writing control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Loopback

   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the TP3051 or TP3056 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.

3. Analog Loopback

   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is entered by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.

4. Power-Down/Power-Up

   The TP3051 or TP3056 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 powers-up the device.

TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 2*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (TP3051) or A-law (TP3056) coding schemes. A precision voltage reference is trimmed in manufacturing

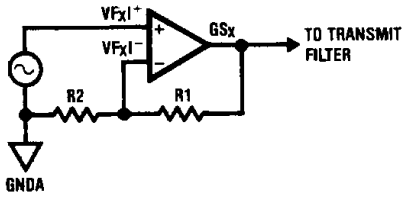
Functional Description (Continued)

to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

DECODER AND RECEIVE FILTER SECTION

The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 kHz. The decoder is of A-law (TP3056) or μ-law (TP3051) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600Ω load to a level of 7.2 dBm. See *Figure 3.* The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.



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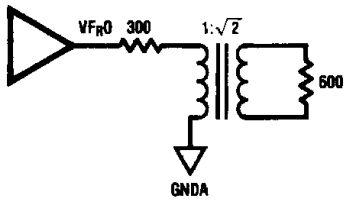
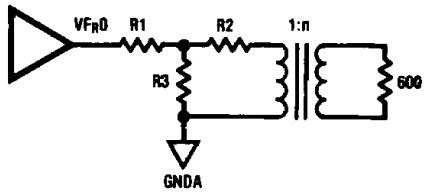
Non-inverting transmit gain = $20 \log_{10} \left(\frac{R1 + R2}{R2} \right)$

Set gain to provide peak overload level = t_{MAX} at GS_X (see Transmission Characteristics)

FIGURE 2. Transmit Gain Adjustment



Maximum output power = 7.2 dBm total, 4.2 dBm to the load.



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See Applications information for attenuator design guide.

FIGURE 3. Receive Gain Adjustment

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

GNDD to GNDA	±0.3V
V_{CCA} or V_{CCD} to GNDD or GNDA	7V
V_{BB} to GNDD or GNDA	−7V
Voltage at Any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GNDD − 0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD (Human Body Model)	1000V

Electrical Characteristics

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, T_A = 0°C to 70°C; typical characteristics specified at nominal supply voltages, T_A = 25°C; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% Electrical testing at T_A = 25°C. All other limits are assured by correlation with other production test and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	DB0–DB7, I_L = 2.5 mA			**0.4**	V
V_{OH}	Output High Voltage	DB0–DB7, I_H = −2.5 mA	**2.4**			V
I_{IL}	Input Low Current	GNDD ≤ V_{IN} ≤ V_{IL}	**−3**		**3**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−3**		**3**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	DB0–DB7, GNDD ≤ V_O ≤ V_{CC}	**−3**		**3**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance, GS_X	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance, GS_X		10			kΩ
C_LXA	Load Capacitance, GS_X				50	pF
V_OXA	Output Dynamic Range, GS_X	R_L = 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	D.C. Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	D.C. Test	**60**			dB
RECEIVE POWER AMPLIFIER						
R_ORF	Output Resistance, VF_RO			1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				50	pF
VOS_RO	Output DC Offset Voltage		**−200**		**200**	mV
POWER DISSIPATION						
I_{CC0}	Power-Down Current	No Load (Note 1)		0.5	**1.5**	mA
I_{BB0}	Power-Down Current	No Load (Note 1)		0.05	**0.3**	mA
I_{CC1}	Active Current	No Load		6.0	**9.0**	mA
I_{BB1}	Active Current	No Load		6.0	**9.0**	mA

Note 1: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Timing Specifications

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, $T_A = 0°C$ to 70°C; typical characteristics specified at nominal supply voltages, $T_A = 25°C$; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to 70°C by correlation with 100% Electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production test and/or product design and characteristics. All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$. See Definitions and Timing Conventions section for test method information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock		760		ns
t_{WCH}	Width of Clock High		**330**		ns
t_{WCL}	Width of Clock Low		330		ns
t_{RC}	Rise Time of Clock			50	ns
t_{FC}	Fall Time of Clock			50	ns
t_{HCCS}	Hold Time from CLK to $\overline{CS}$ Low		**100**		ns
t_{SCLC}	Set-Up Time of $\overline{CS}$ Low to CLK		**100**		ns
t_{SCHC}	Set-Up Time from $\overline{CS}$ High to Second CLK Edge		**0**		ns
t_{WCS}	Width of Chip Select		**100**		ns
t_{SPCM}	Set-Up Time of $\overline{PCM}$/CNTL to $\overline{CS}$		**0**		ns
t_{HPCM}	Hold Time from $\overline{CS}$ to $\overline{PCM}$/CNTL		**100**		ns
t_{SDC}	Set-Up Time of Data In to CLK		**50**		ns
t_{HCD}	Hold Time from CLK to Data In		20		ns
t_{DDO}	Delay Time to Data Out Valid	$C_L = 0$ pF to 200 pF	**90**	**260**	ns
t_{DDZ}	Delay Time to Data Output Disabled	$C_L = 0$ pF to 200 pF	20	80	ns

Switching Time Waveforms

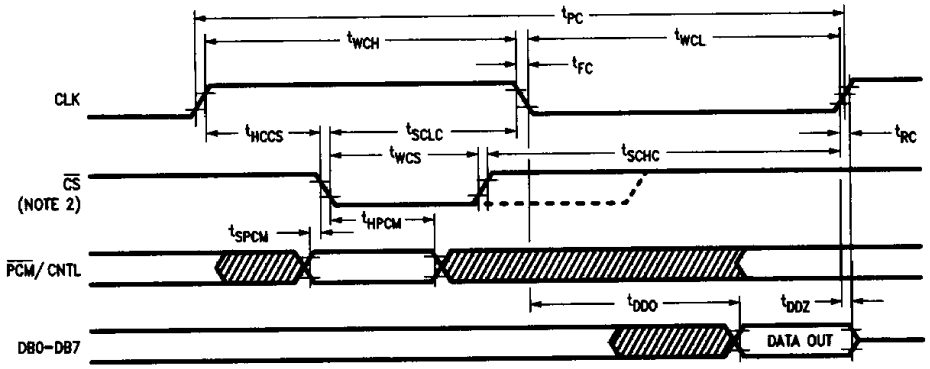

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FIGURE 4a. Timing Waveforms for COMBO Writing to the Bus

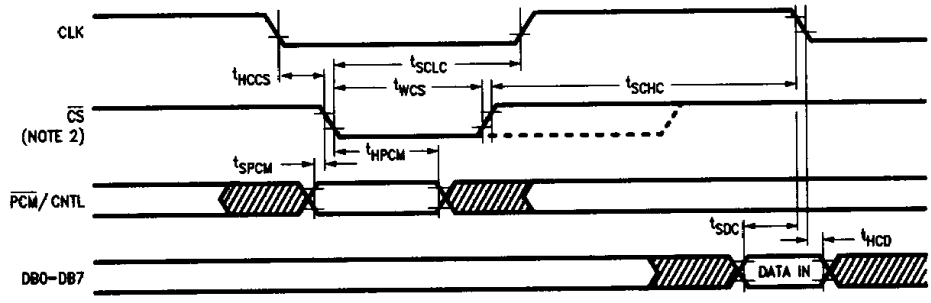

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FIGURE 4b. Timing Waveforms for COMBO Reading from the Bus

Note 2: READ and WRITE $\overline{CS}$ pulses must each occur at an 8 kHz rate, and may occur on consecutive half-cycles of CLK if required, although this is not a restriction.

Transmission Characteristics

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
	0 dBm0	TP3051 TP3056		1.2276 1.2276		Vrms Vrms
t_{MAX}	Maximum Overload Level	TP3051 (+3.17 dBm0) TP3056 (+3.14 dBm0)		2.501 2.492		V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V_{CCA} = V_{CCD} = 5.0V, V_{BB} = −5.0V Input at GS_X = 0 dBm0 at 1020 Hz	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz–3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7**		−40 −30 **−26** **−0.1** **0.15** **0.1** **0** **−14** **−32**	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variation with Level	Sinusoidal Method Reference Level = −10 dBm0 VF_XI^+ = −40 dBm0 to +3 dBm0 VF_XI^+ = −50 dBm0 to −40 dBm0 VF_XI^+ = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V_{CCA} = V_{CCD} = 5V, V_{BB} = −5V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	**−0.15** **−0.35** **−0.7**		**0.15** **0.05** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variation with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded −10 dBm0 Signal PCM Level = −40 dBm0 to +3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
V_{RO}	Receive Output Drive Level	R_L = 600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3051, (Note 3)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3056, VF_XI^+ = 0V (Note 3)		−74	**−69**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3051, PCM Code Equals Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3056, PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0V			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = 0V, V_{CCA} = V_{CCD} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 4)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = 0 Vrms, V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 4)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 V_{CC} = 5.0 V_{DC} + 100 mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBc
		f = 25 kHz–50 kHz	**36**			dBc
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 V_{BB} = −5.0 V_{DC} + 100 mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBc
		f = 25 kHz–50 kHz	**36**			dBc
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			**−32**	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 5) Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 XMT RCV = −55 dBm0 XMT RCV	 **33** **36** **29** **30** **14** **15**			 dB dB dB dB dB dB
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz at 0 dBm0 Transmit Level Steady PCM Receive Code		−90	**−70**	dB
CT_{R-X}	Receive to Transmit Crosstalk 0 dBm0 Receive Level	f = 300 Hz–3400 Hz at 0 dBm0 (Note 2)		−90	**−70**	dB

Note 3: Measured by extrapolation from the distortion test result at −50 dB m0.

Note 4: CT_{R-X}, $PPSR_X$, and $NPSR_X$ are measured with a −50 dBm0 activation signal applied at VF_XI^+.

Note 5: Devices are measured using C message weighted filter for μ-law and psophometric weighted filter for A-law.

Encoding Format at Data Bus Output

	TP3051 μ-Law								TP3056 True A-Law, C5 = 0 (Includes Even Bit Inversion)							
	MSB							LSB	MSB							LSB
V_{IN} = + Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = +0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
V_{IN} = − 0V	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = − Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Applications Information

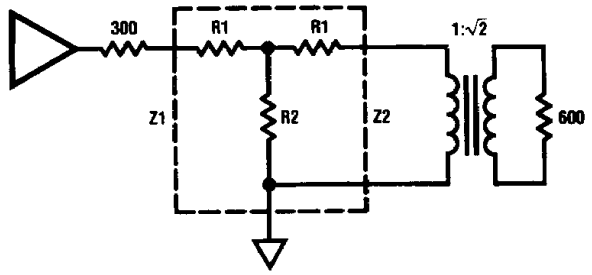
POWER SUPPLIES

While the pins of the TP3051/6 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used. GNDA and GNDD MUST be connected together adjacent to each COMBO not on the connector or backplane wiring.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CCA} and V_{BB}.

For best performance, the ground point of each COMBO on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

T-Pad Attenuator



TL/H/8834-8

$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

Where: $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

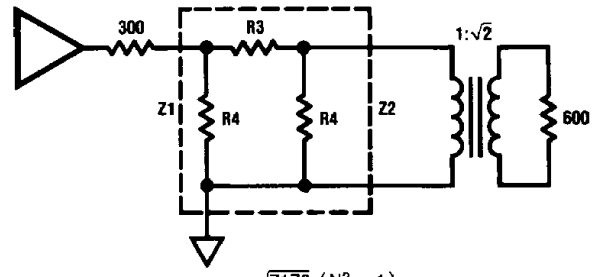
$$S = \sqrt{\frac{Z1}{Z2}}$$

Also: $Z = \sqrt{Z_{SC}\,Z_{OC}}$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

π-Pad Attenuator



TL/H/8834-9

$$R3 = \sqrt{\frac{Z1Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

FIGURE 5. T-Pad and π-Pad Attenuator Models

The positive power supply to the bus drivers, V_{CCD}, is provided on a separate pin from the positive supply for the CODEC and filter circuits to minimize noise injection when driving the bus. V_{CCA} and V_{CCD} MUST be connected together close to the CODEC/filter at the point where the 0.1 μF decoupling capacitor is connected.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family COMBO receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. (See *Figure 5.*) Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closer practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Note: See Application Note 370 for further details.