



EMIF06-VID01C1

6 LINES LOW CAPACITANCE EMI FILTER AND ESD PROTECTION

IPAD™

MAIN APPLICATION

Where EMI filtering in ESD sensitive equipment is required:

- LCD and camera for mobile phones
- Computers and printers
- Communication systems
- MCU board

DESCRIPTION

The EMIF06-VID01C1 is a 6 lines highly integrated array designed to suppress EMI / RFI noise in all systems subjected to electromagnetic interferences.

The EMIF06-VID01C1 Flip-Chip packaging means the package size is equal to the die size. Additionally, this filter includes an ESD protection circuitry which prevents the protected device from destruction when subjected to ESD surges up to 15 kV.

BENEFITS

- High efficiency EMI filtering (-40db @ 900MHz)
- Low line capacitance suitable for high speed data bus
- Low serial resistance for camera impedance adaptation
- Optimized PCB space consuming:
2.92mm x 1.29mm
- Very thin package: 0.69 mm
- High efficiency in ESD suppression on inputs pins (IEC61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reducing of parasitic elements through integration & wafer level packaging

COMPLIES WITH THE FOLLOWING STANDARDS: IEC61000-4-2

Level 4 on input pins 15kV (air discharge)
 8kV (contact discharge)

MIL STD 883E - Method 3015-6 Class 3

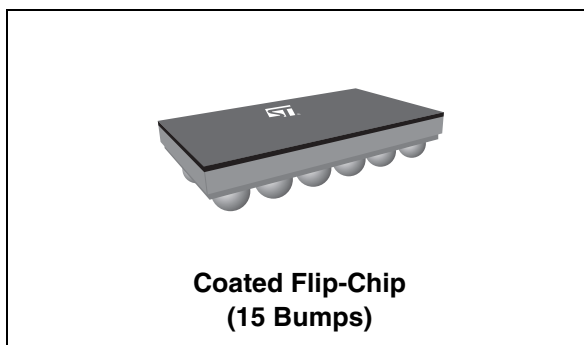


Table 1: Order Code

Part Number	Marking
EMIF06-VID01C1	GR

Figure 1: Pin Configuration (ball side)

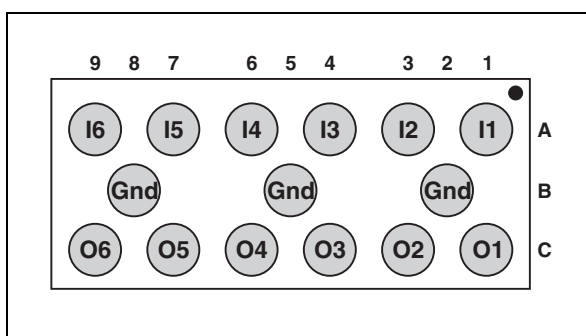
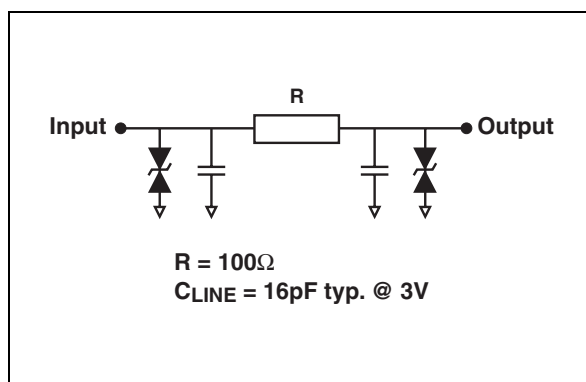


Figure 2: Configuration



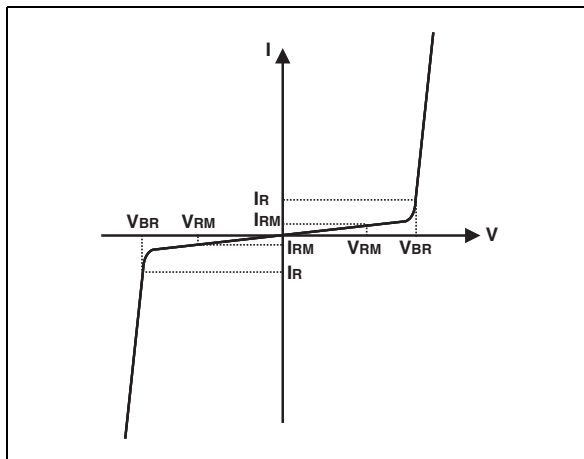
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Table 2: Absolute Ratings (limiting values)

Symbol	Parameter and test conditions	Value	Unit
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Table 3: Electrical Characteristics ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
R	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	$I_R = 1\text{mA}$	6	8	10	V
I_{RM}	$V_{RM} = 3\text{V per line}$			500	nA
R	$I = 10\text{mA}$	80	100	120	Ω
C_{line}	$V_R = 3\text{V DC}$ 1MHz $V_{OSC} = 30\text{mV}$		16	19	pF

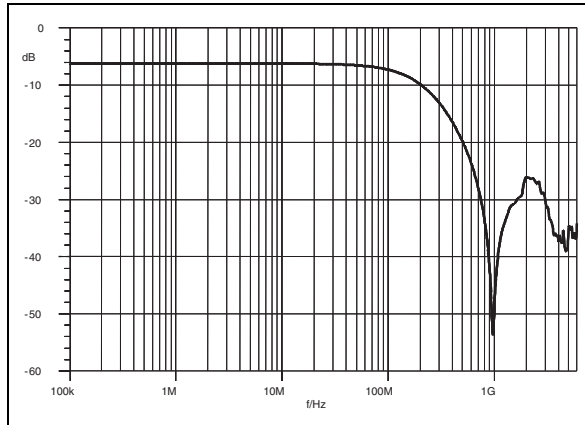
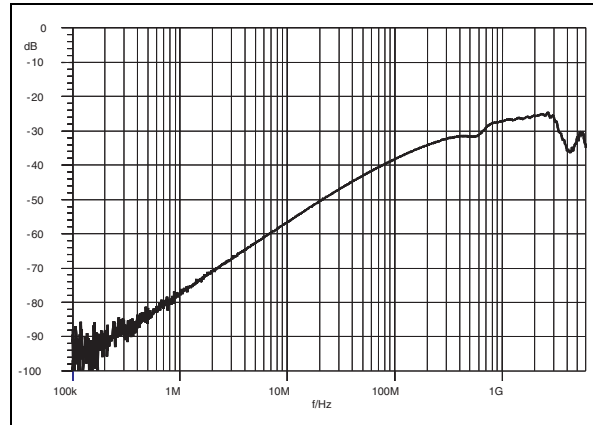
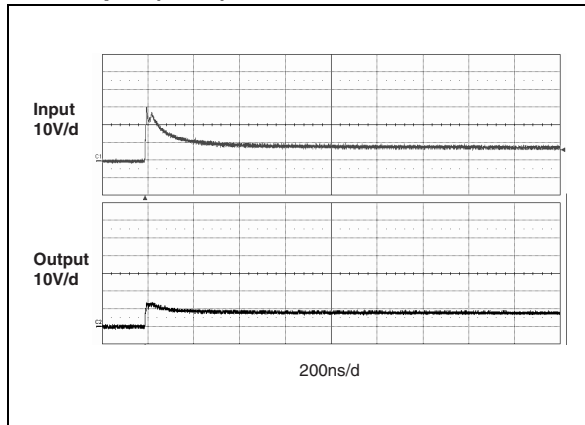
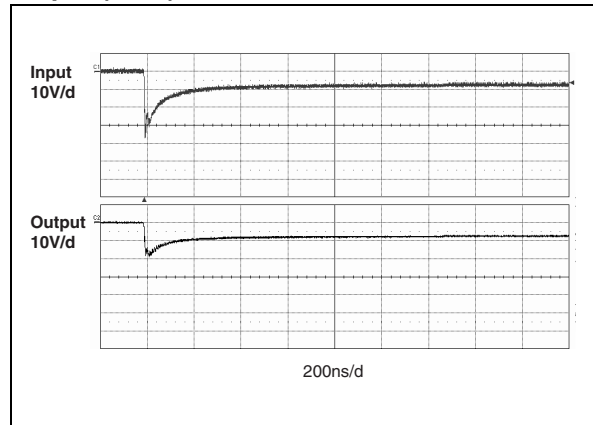
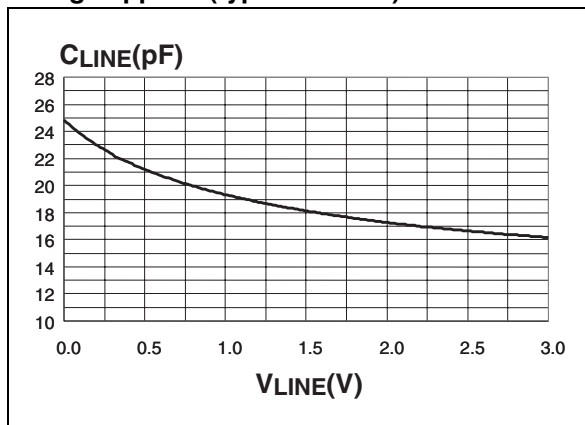
Figure 3: S21 (dB) attenuation measurement**Figure 4: Analog crosstalk measurement****Figure 5: ESD response to IEC61000-4-2 (+15kV air discharge) on one input V(in) and on one output (Vout)****Figure 6: ESD response to IEC61000-4-2 (-15kV air discharge) on one input V(in) and on one output (Vout)****Figure 7: Junction capacitance versus reverse voltage applied (typical values)**

Figure 8: Ordering Information Scheme

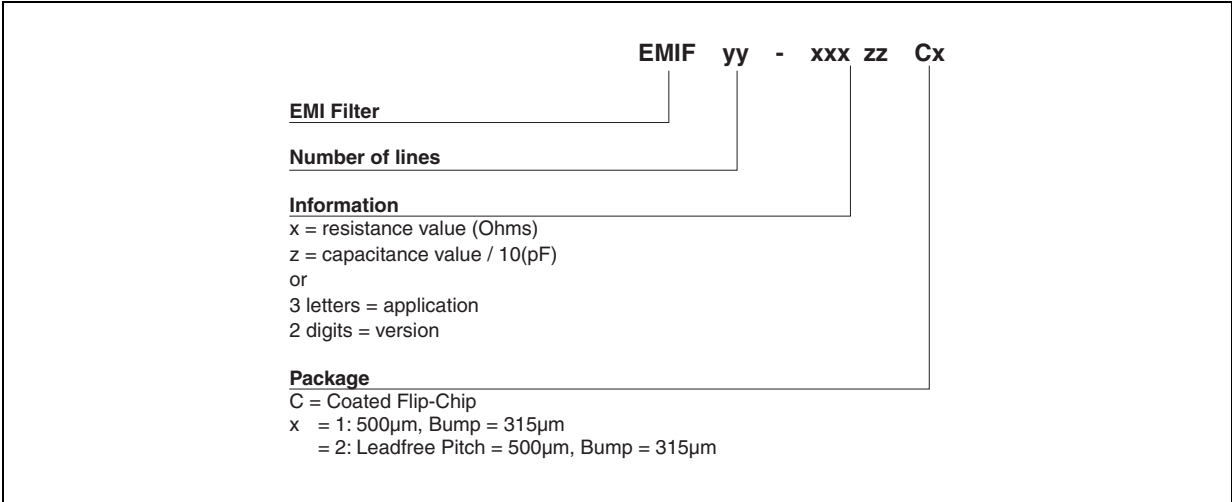


Figure 9: FLIP-CHIP Package Mechanical Data

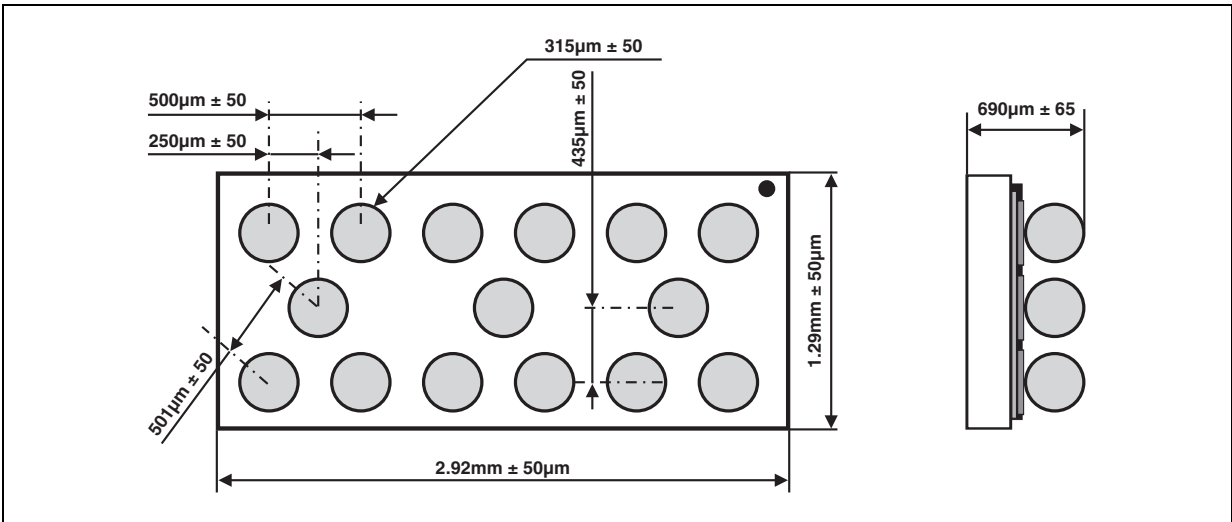


Figure 10: Foot Print Recommendations

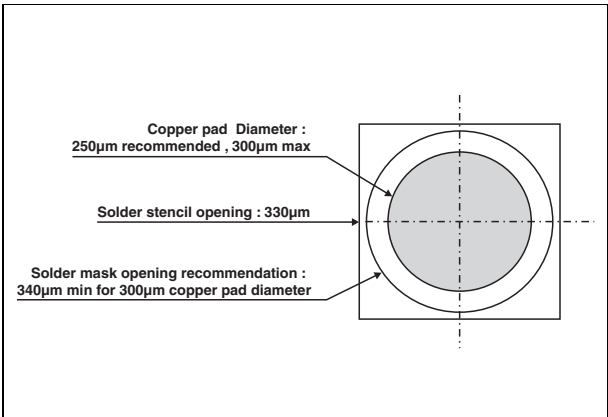
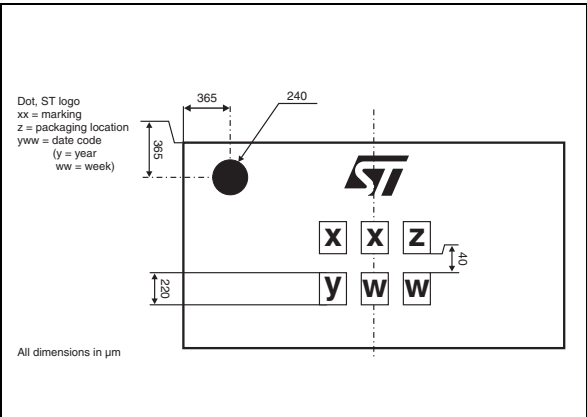


Figure 11: Marking



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