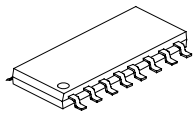
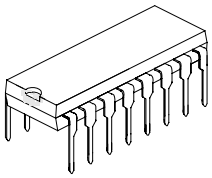
UTC 4052 CMOS

ANALOG MULTIPLEXERS /DEMULTIPLEXERS



SOP-16



DIP-16

DESCRIPTION

The UTC 4052 analog multiplexers is digitally –controlled analog switch. The device feature low ON impedance and very low OFF leakage current. Control of analog signals up to the complete supply voltage range can be achieved.

FEATURES

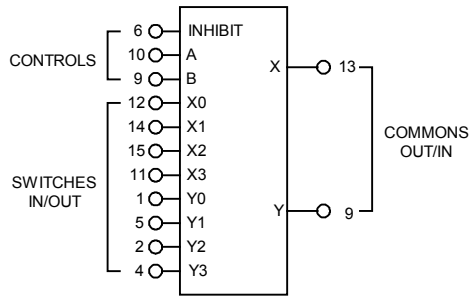
*Triple Diode Protection on Control Inputs
*Switch Function is Break Before Make
*Supply Voltage Range=3.0 Vdc to 18 Vdc
*Analog Voltage Range(VDD-VEE)=3.0 to 18V
Note:VEE must be≤Vss
*Linearized Transfer Characterisstics
*Low-noise-12nV/ $\sqrt{\text{Cycle}}$,f≥1.0kHz Typical

ABSOLUTE MAXIMUM RATINGS*[1]

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage (Referenced to V_{EE},Vss≥V_{EE})	V_{DD}	-0.5 ~ +18.0	V
Input or Output Voltage (DC or Transient) (Referenced to Vss for Control Inputs and V_{EE} for switch I/O)	Vin,Vout	-0.5 ~ V_{DD}+0.5	V
Input Current (DC or Transient) per Control Pin	Iin	±10	mA
Switch Through Current	I_{SW}	±25	mA
Power Dissipation *[2] DIP-16 SOP-16	P_D	 700 500	mW
Ambient Temperature Range	T_A	-55 ~ +125	°C
Storage Temperature Range	Tstg	-65 ~ +150	°C
Lead Temperature (8-Second Soldering)	T_{LEAD}	260	°C

*1. Maximum Ratings are those values beyond which damage to the device may occur.
*2. Temperature Derating : 7.0 mW/℃ From 65℃ ~ 125℃

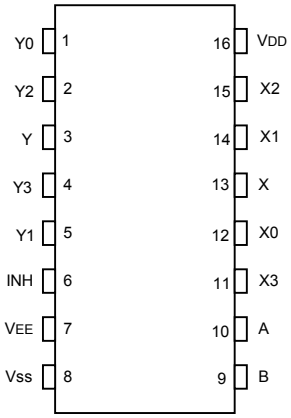
Dual 4-Channel Analog Multiplexer/Demultiplexer



V_{DD}=PIN16, V_{SS}=PIN8, V_{EE}=PIN7

Note: Control Inputs referenced to Vss.
Analog Inputs and Outputs reference to VEE.
VEE must be <Vss.

PIN ASSIGMENT



ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	-55°C		25°C			125°C		UNIT
			MIN	MAX	MIN	TYP*3	MAX	MIN	MAX	
SUPPLY REQUIREMENTS (Voltages Referenced to VEE)										
Power Current Per Range	V_{DD}	V_{DD}-3.0≥Vss≥V_{EE}	3.0	18	3.0		18	3.0	18	V
Quiescent Current Per Package	I_{DD}	Control Inputs: Vin=Vss or V_{DD},Switch I/O : V_{EE}≤$V_{I/O}$≤≤V_{DD}, and△Vswitch≤500mV *4								µA
		V_{DD}=5.0V		5.0		0.005	5.0		150	
		V_{DD}=10V		10		0.010	10		300	
		V_{DD}=15V		20		0.015	20		600	
Total Supply Current (Dynamic Plus Quiescent, Per Package	$I_{D(AV)}$	TA=25℃only (The channel component, (Vin-Vout) /Ron, is not included.)								µA
		V_{DD}=5.0V				(0.07µA/kHz)f+I_{DD}				
		V_{DD}=10V			Typical	(0.20µA/kHz)f+I_{DD}				
		V_{DD}=15V				(0.36µA/kHz)f+I_{DD}				
CONTROL INPUTS-INHIBIT, A, B, C (Voltages Referenced to Vss)										
Low-Level Input Voltage	V_{IL}	Ron=per spec, Ioff=per spec								V
		V_{DD}=5.0V		1.5		2.25	1.5		1.5	
		V_{DD}=10V		3.0		4.50	3.0		3.0	
		V_{DD}=15V		4.0		6.75	4.0		4.0	
High-Level Input Voltage	V_{IH}	Ron=per spec, Ioff=per spec								V
		V_{DD}=5.0V	3.5		3.5	2.75		3.5	-	
		V_{DD}=10V	7.0		7.0	5.50		7.0	-	
		V_{DD}=15V	11		11	8.25		11	-	

PARAMETER	SYMBOL	TEST CONDITIONS	-55°C		25°C			125°C		UNIT
			MIN	MAX	MIN	TYP*3	MAX	MIN	MAX	
Input Leakage Current	Iin	V_{DD}=15V ,Vin=0 or V_{DD}		±0.1		$\pm 10^{-5}$	±0.1		1.0	μA
Input Capacitance	Cin					5.0	7.5			pF
SWITCHES IN/OUT AND COMMONS OUT/IN –X,Y,Z(Voltages Referenced to V_{EE})										
Recommended Peak-to-Peak Voltage Into or Out of the Switch	$V_{I/O}$	Channel On or Off	0	V_{DD}	0		V_{DD}	0	V_{DD}	Vpp
Recommended Static or Dynamic Voltage Across the Switch *4 (Figure 3)	△V_{switch}	Channel On	0	600	0		600	0	300	mV
Output Offset Voltage	Voo	Vin=0V,No Load				10				μV
ON Resistance	Ron	△V_{switch}≤500mV *4 Vin=V_{IL} or V_{IH} (Control), and Vin=0 to V_{DD}(Switch) V_{DD}=5.0V V_{DD}=10V V_{DD}=15V		 800 400 220		 250 120 80	 1050 500 280		 1200 520 300	Ω
△ON Resistance Between Any Two Channels in the Same Package	△Ron	V_{DD}=5.0V V_{DD}=10V V_{DD}=15V		70 50 45		25 10 10	70 50 45		135 95 65	Ω
Off-Channel Leakage Current(Figure 8)	Ioff	V_{DD}=15V ,Vin=VIL or VIH (Control) Channel to Channel or Any One Channel		±100		±0.05	±100		±1000	nA
Capacitance, Switch I/O	$C_{I/O}$	Inhibit=V_{DD}				10				pF
Capacitance, Common O/I	$C_{O/I}$	Inhibit=V_{DD}				32				pF
Capacitance, Feedthrough (Channel Off)	$C_{I/O}$	Pins Not Adjacent Pins Adjacent				0.15 0.47				pF

*3. Data labeled “Typ” is not to be used for design purposes, but is intended as an indication of the IC’s potential performance.

*4. For voltage drops across the switch (△Vswitch) > 600 mV (> 300 mV at high temperature), excessive V_{DD} current may be drawn, i.e. the current out of the switch may contain both V_{DD} and switch input components. The reliability of the device will be unaffected unless the Maximum Ratings are exceeded. (See first page of this data sheet.)

ELECTRICAL CHARACTERISTICS *5 (C_L = 50 pF, T_A = 25℃) (V_{EE} ≤V_{SS} unless otherwise indicated)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP*6	MAX	UNIT
Propagation Delay Times(Figure 4) Switch Input to Switch Output	t_{PLH},t_{PHL}	R_L=10kΩ V_{DD}-V_{EE}= 5.0, t_{PLH},t_{PHL}=(0.17 ns/pF) C_L+21.5 ns V_{DD}-V_{EE}=10, t_{PLH},t_{PHL}=(0.08 ns/pF) C_L+8.0 ns V_{DD}-V_{EE}=15, t_{PLH},t_{PHL}=(0.06 ns/pF) C_L+7.0 ns		30 12 10	75 30 25	ns
Propagation Delay Times(Figure 4) Inhibit to Output	t_{PHZ},t_{PLZ} t_{PZH},t_{PZL}	RL=10kΩ,VEE=Vss Output"1" or "0" to High Impedance, or High Impedance to"1" or "0" Level V_{DD}-V_{EE}= 5.0 V_{DD}-V_{EE}=10 V_{DD}-V_{EE}=15		 300 155 125	 600 310 250	ns
Propagation Delay Times(Figure 4) Control Input to Output	t_{PLN},t_{PHL}	RL=10kΩ,V_{EE}=Vss V_{DD}-V_{EE}= 5.0 V_{DD}-V_{EE}=10 V_{DD}-V_{EE}=15		 325 130 90	 650 260 180	ns
Second Harmonic Distortion		R_L=10kΩ, f=1kHz, V_{in}=5Vpp, V_{DD}-V_{EE}=10		0.07		%
Bandwidth (Figure 5)	BW	R_L=1kΩ, V_{in}=1/2(V_{DD}-V_{EE})p-p, C_L=50pF, 20 Log (V_{out}/V_{in})=-3dB, V_{DD}-V_{EE}=10		17		MHz
Off Channel Feedthrough Attenuation (Figure 5)		R_L=1kΩ, Vin=1/2(V_{DD}-V_{EE})p-p, Fin=30MHz, V_{DD}-V_{EE}=10		-50		dB
Channel Separation (Figure 6)		RL=1kΩ, Vin=1/2(V_{DD}-V_{EE})p-p, fin=3.0MHz, V_{DD}-V_{EE}=10		-50		dB
Crosstalk ,Control Input to Common O/I (Figure 7)		R1=1kΩ, R_L=10kΩ, Control t_{TLH}=t_{THL}=20ns ,Inhibit=Vss), V_{DD}-V_{EE}=10		75		mV

*5. The formulas given are for the typical characteristics only at 25 ℃.

*6. Data labelled "Typ" is not lo be used for design purposes but In intended as an indication of the IC's potential performance.

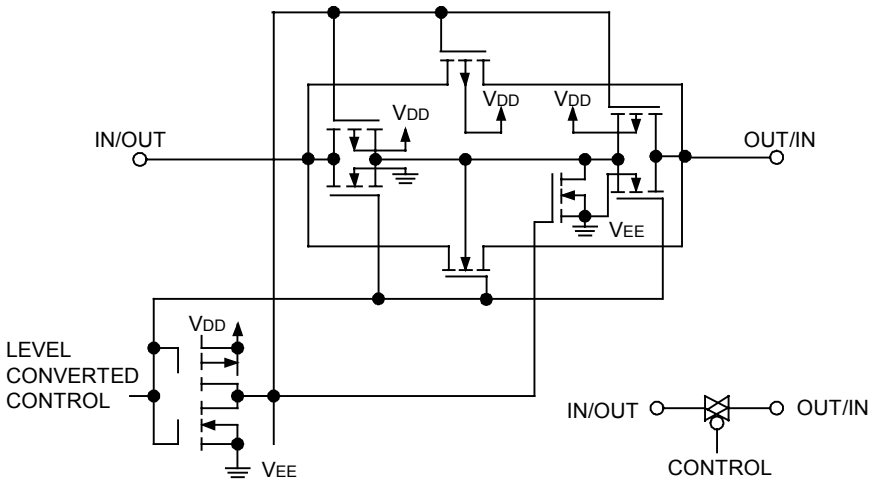


Figure 1.Switch Circuit Schematic

TRUTH TABLE

Control Inputs			ON Switches
	Select		
Inhibit	B	A	
0	0	0	Y0 X0
0	0	1	Y1 X1
0	1	0	Y2 X2
0	1	1	Y3 X3
1	X	X	None

* X=Don't Care

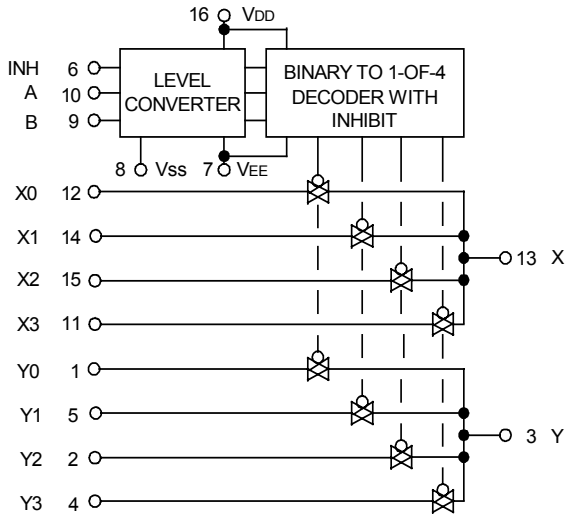


Figure 2. Functional Diagram

TEST CIRCUITS

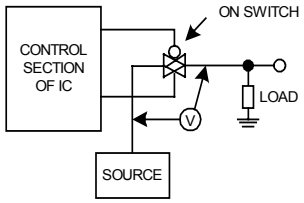


Figure 3.→△V Across Switch

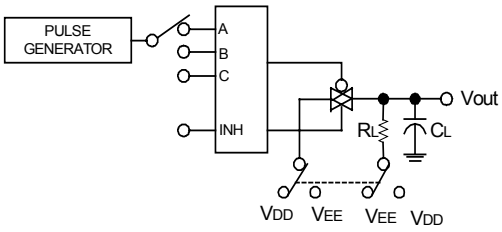


Figure 4. Propagation Delay Times, Control and Inhibit to Output

A,B,and C inputs used to tum ON or OFF the switch under tes.

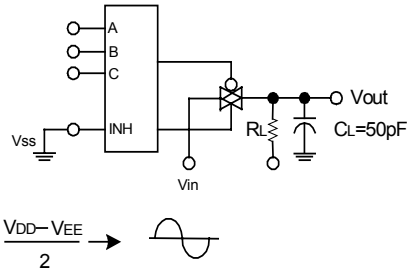


Figure 5. Bandwidth and Off-Channe Feedthrough Attenuation

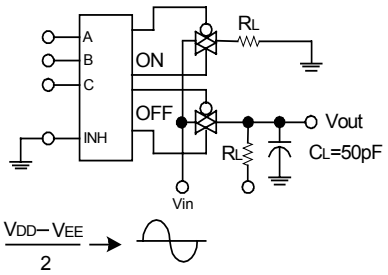


Figure 6. Channel Separation
(Adjacent Channels Used For Setup)

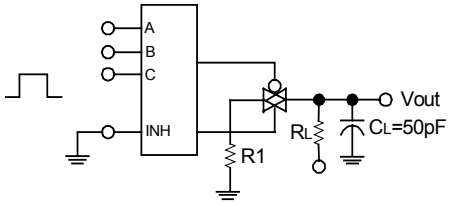


Figure 7. Crosstalk,Control Input to Common O/I

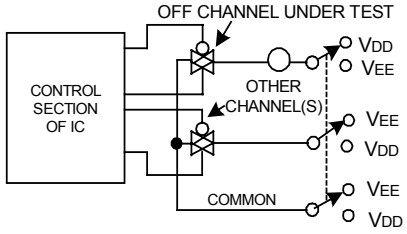


Figure 8. Off Channel Leakage

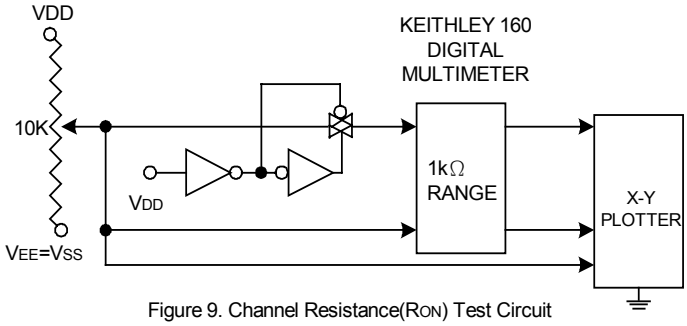


Figure 9. Channel Resistance(R_{ON}) Test Circuit

TYPICAL RESISTANCE CHARACTERISTIS

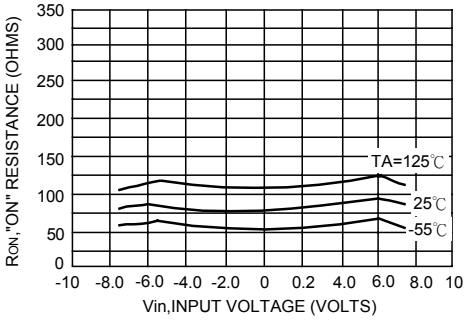


Figure10.V_{DD}=7.5V,V_{EE}=-7.5V

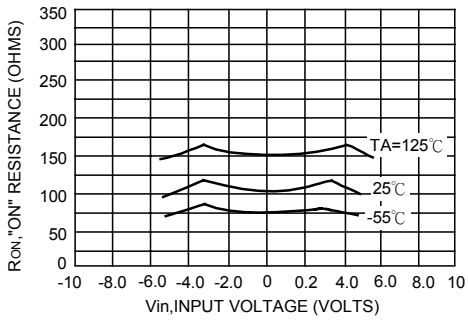


Figure11.V_{DD}=5.0V,V_{EE}=-5.0V

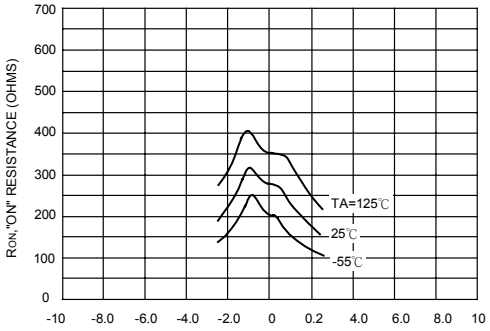


Figure12.VDD=2.5V,VEE=-2.5V

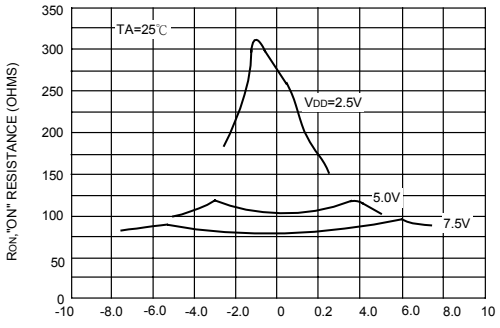


Figure13 Comparison at 25℃,VDD=-VEE

Figure A illustrates use of the on–chip level converter detailed in Figures 2. The 0 ~ 5 V Digital Control signal is used to directly control a 9 Vp–p analog signal.

The digital control logic levels are determined by V_{DD} and V_{SS}. The V_{DD} voltage is the logic high voltage; the V_{SS} voltage is logic low. For the example, V_{DD} = + 5 V = logic high at the control inputs; V_{SS} = GND = 0 V = logic low.

The maximum analog signal level is determined by V_{DD} and V_{EE}. The V_{DD} voltage determines the maximum recommended peak above V_{SS}. The V_{EE} voltage determines the maximum swing below V_{SS}. For the example, V_{DD} – V_{SS} = 5 V maximum swing above V_{SS}; V_{SS} – V_{EE} = 5 V maximum swing below V_{SS}. The example shows a ± 4.5 V signal which allows a 1/2 volt margin at each peak. If voltage transients above V_{DD} and/or below V_{EE} are anticipated on the analog channels, external diodes (Dx) are recommended as shown in Figure B. These diodes should be small signal types able to absorb the maximum anticipated current surges during clipping.

The *absolute* maximum potential difference between V_{DD} and V_{EE} is 18.0 V. Most parameters are specified up to 15 V which is the *recommended* maximum difference between V_{DD} and V_{EE}.

Balanced supplies are not required. However, V_{SS} must be greater than or equal to V_{EE}. For example, V_{DD} = + 10 V, V_{SS} = + 5 V, and V_{EE} – 3 V is acceptable. See the Table below.

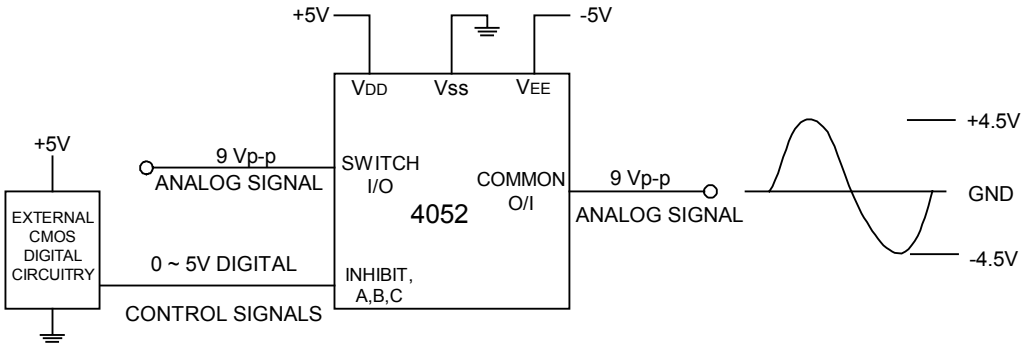


Figure A. Application Example

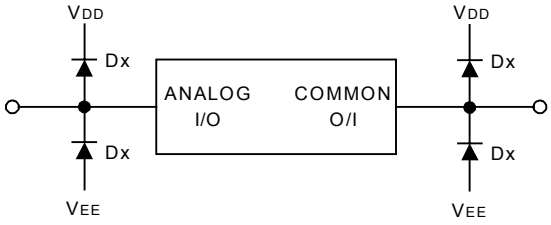


Figure B.External Germanium or Schottky Clipping Diodes

POSSIBLE SUPPLY CONNECTIONS

VDD IN VOLTS	VSS IN VOLTS	VEE IN VOITS	CONTROL INPUTS LOGIC HIGH/LOGIC LOW IN VOLTS	MAXIMUM ANALOG SIGNAL RANGE IN VOLTS
+8	0	-8	+8/0	+8 ~ -8=16Vp-p
+5	0	-12	+5/0	+5 ~–12=17Vp-p
+5	0	0	+5/0	+5 ~ 0=5Vp-p
+5	0	-5	+5/0	+5 ~ -5=10Vp-p
+10	+5	-5	+10/+5	+10 ~ –5=15Vp-p