



N- and P-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

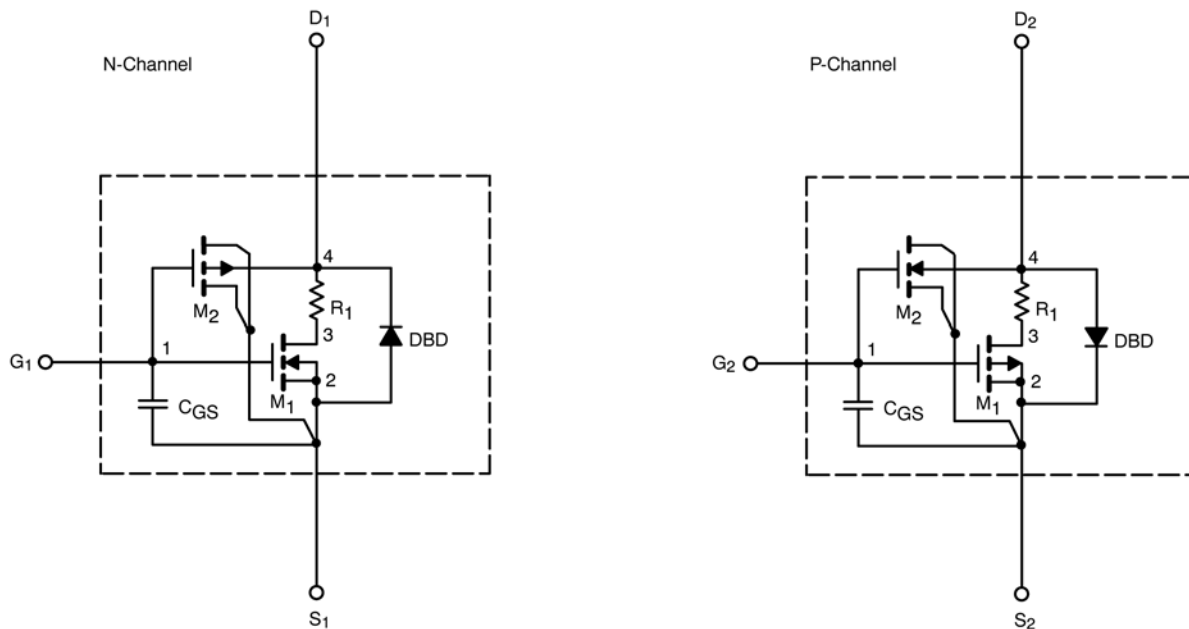
- N- and P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n- and p-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

SPECIFICATIONS (T _J = 25°C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Simulated Data	Measured Data	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	N-Ch	0.50			
		V _{DS} = V _{GS} , I _D = -250 μA	P-Ch	0.80			
On-State Drain Current ^a	I _{D(on)}	V _{DS} < 5 V, V _{GS} = 4.5 V	N-Ch	117		A	
		V _{DS} < -5 V, V _{GS} = -4.5 V	P-Ch	60			
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.4 A	N-Ch	0.032	0.032	Ω	
		V _{GS} = -4.5 V, I _D = -3.3 A	P-Ch	0.063	0.060		
		V _{GS} = 2.5 V, I _D = 4.1 A	N-Ch	0.038	0.037		
		V _{GS} = -2.5 V, I _D = -2.8 A	P-Ch	0.082	0.083		
		V _{GS} = 1.8 V, I _D = 1.8 A	N-Ch	0.046	0.046		
		V _{GS} = -1.8 V, I _D = -0.76 A	P-Ch	0.107	0.108		
Forward Transconductance ^a	g _{fs}	V _{DS} = 10 V, I _D = 4.4 A	N-Ch	23	22	S	
		V _{DS} = -10 V, I _D = -3.3 A	P-Ch	11	9		
Diode Forward Voltage ^a	V _{SD}	I _S = 1.2 A	N-Ch	0.72	0.80	V	
		I _S = -1A	P-Ch	0.78	- 080		
Dynamic ^b							
Input Capacitance	C _{iss}	N-Channel V _{DS} = 10 V, V _{GS} = 0 V, f = 1 MHz P-Channel V _{DS} = -10 V, V _{GS} = 0 V, f = 1 MHz	N-Ch	605	520	pF	
			P-Ch	589	455		
Output Capacitance	C _{oss}		N-Ch	96	100		
			P-Ch	103	105		
Reverse Transfer Capacitance	C _{rss}		N-Ch	62	60		
			P-Ch	57	65		
Total Gate Charge	Q _g	V _{DS} = 10 V, V _{GS} = 8 V, I _D = 4.4 A	N-Ch	8.1	10.5	nC	
		V _{DS} = - 10 V, V _{GS} = -8 V, I _D = -4.6 A	P-Ch	8.4	9.1		
		N-Channel V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 4.4 A P-Channel V _{DS} = -10 V, V _{GS} = -4.5 V, I _D = -1.8 A	N-Ch	5	6		
			P-Ch	5	5.5		
Gate-Source Charge	Q _{gs}		N-Ch	0.91	0.91		
			P-Ch	0.75	0.75		
Gate-Source Charge	Q _{gs}		N-Ch	0.70	0.70		
			P-Ch	1.5	1.5		

Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.

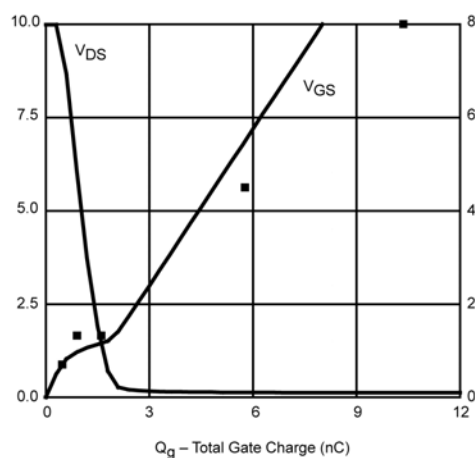
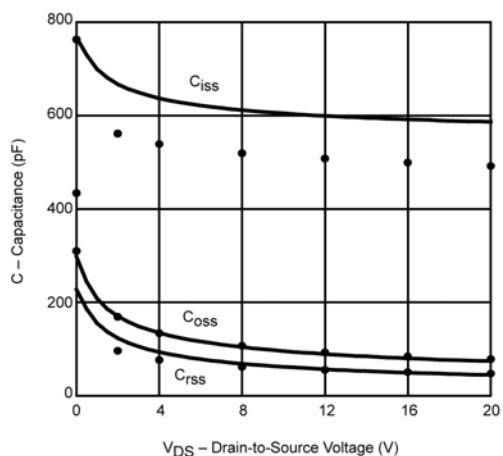
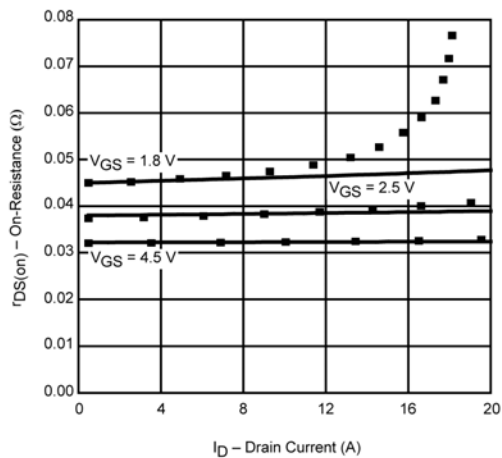
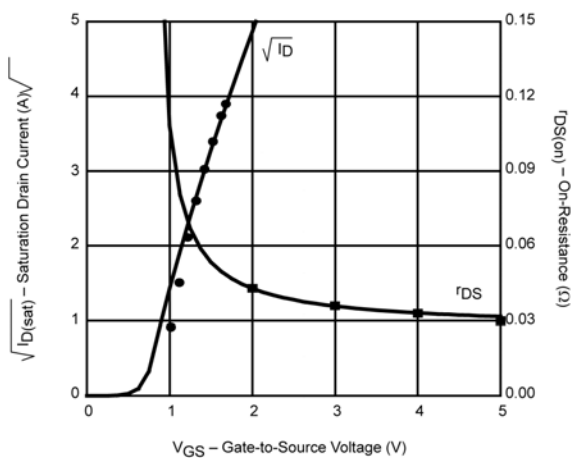
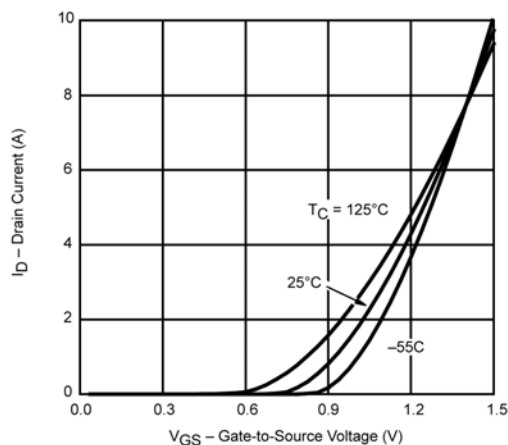
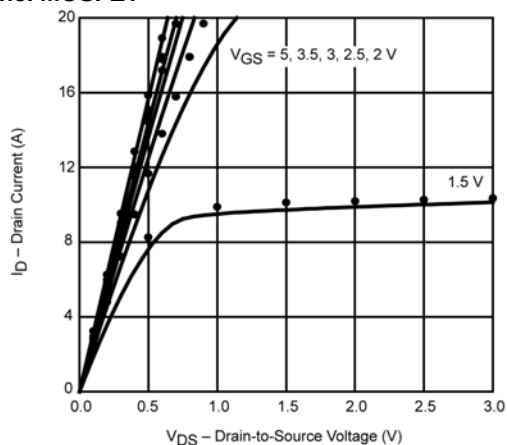


SPICE Device Model Si5517DU

Vishay Siliconix

COMPARISON OF MODEL WITH MEASURED DATA ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

N-Channel MOSFET



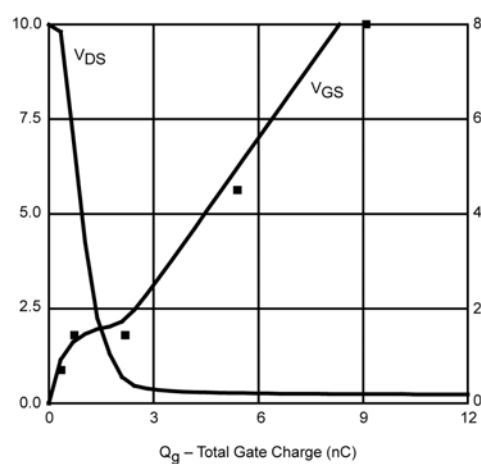
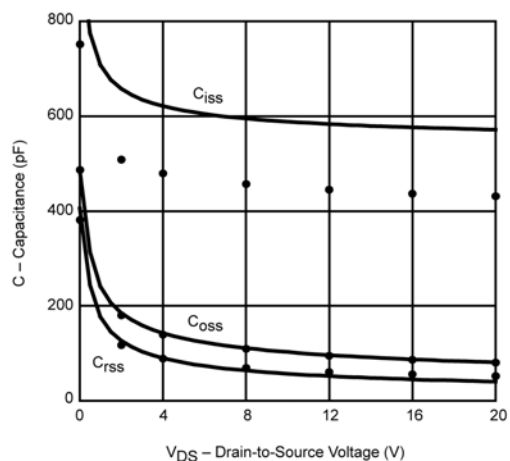
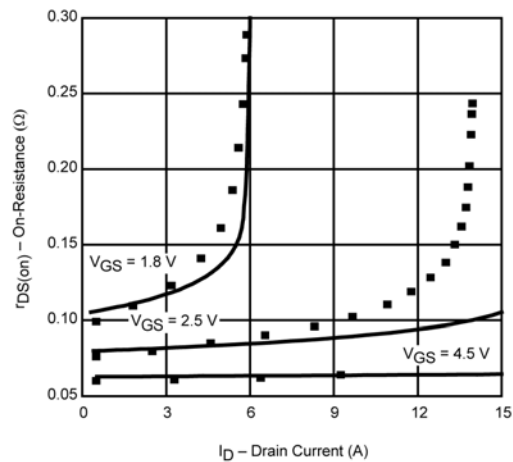
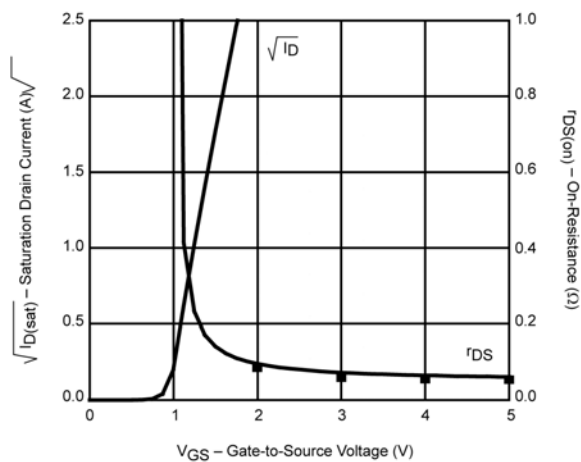
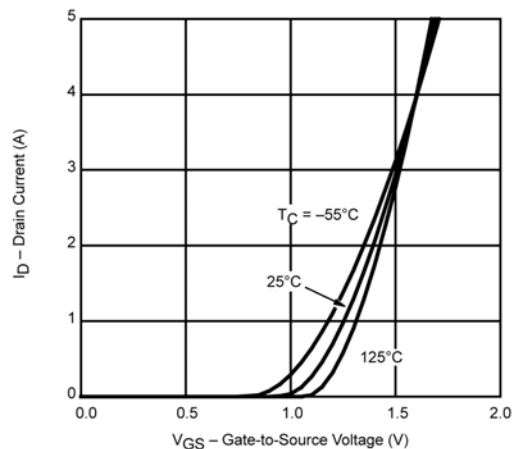
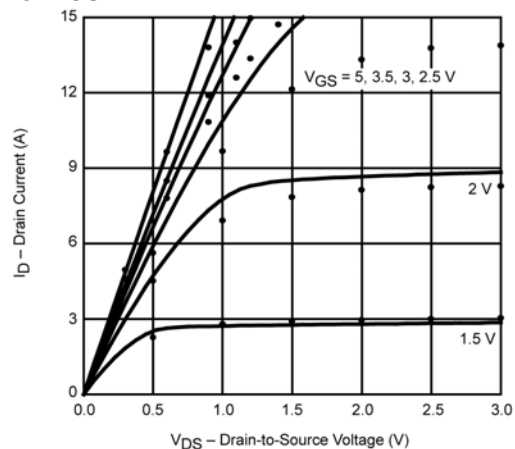
Note: Dots and squares represent measured data.

SPICE Device Model Si5517DU

Vishay Siliconix



P-Channel MOSFET



Note: Dots and squares represent measured data.