CONTENTS

1 FEATURES

- 8-bit CPU, ROM, RAM, I/O in a single 28-lead package
- ROM:
  - 2 kbytes (PCD3344A)
  - 4 kbytes (PCD3349A)
- 224 bytes RAM
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O port lines
- 8-bit programmable Timer/event counter 1
- 2 single-level vectored interrupts:
  - external
  - Timer/event counter 1
- Two test inputs, one of which also serves as the external interrupt input
- DTMF tone generator
- Reference for supply and temperature-independent TONE output
- Filtering for low output distortion (CEPT compatible)
- Power-on-reset
- Stop and Idle modes
- Supply voltage: 1.8 to 6 V (DTMF TONE output from 2.5 V)
- Low standby voltage of 1 V
- Low Stop mode current of 1 μA (typ.)
- Clock frequency: 1 to 16 MHz (3.58 MHz for DTMF suggested)
- Manufactured in silicon gate CMOS process.

2 GENERAL DESCRIPTION

The PCD3344A and the PCD3349A provide 2 kbytes and 4 kbytes respectively of Program Memory, 224 bytes of RAM and 20 I/O lines.

The PCD3344A and PCD3349A are microcontrollers which have been designed primarily for telecom applications. They include an on-chip dual tone multifrequency (DTMF) generator.

The instruction set is based on that of the MAB8048 and is software compatible with the PCD33xxA family. This data sheet details the specific properties of the PCD3351A, PCD3352A and PCD3353A. The shared characteristics of the PCD33XXA family of microcontrollers are described in the:

"PCD33xxA Family" data sheet or

"Data Handbook IC03; Section PCD33xxA Family",

which should be read in conjunction with this publication.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3344AP; PCD3349AP	DIP28	plastic dual in-line package; 28 leads (600 mil)	SOT117-1
PCD3344AT; PCD3349AT	SO28	plastic small outline package; 28 leads; body width 7.5 mm	SOT136-1

4 BLOCK DIAGRAM

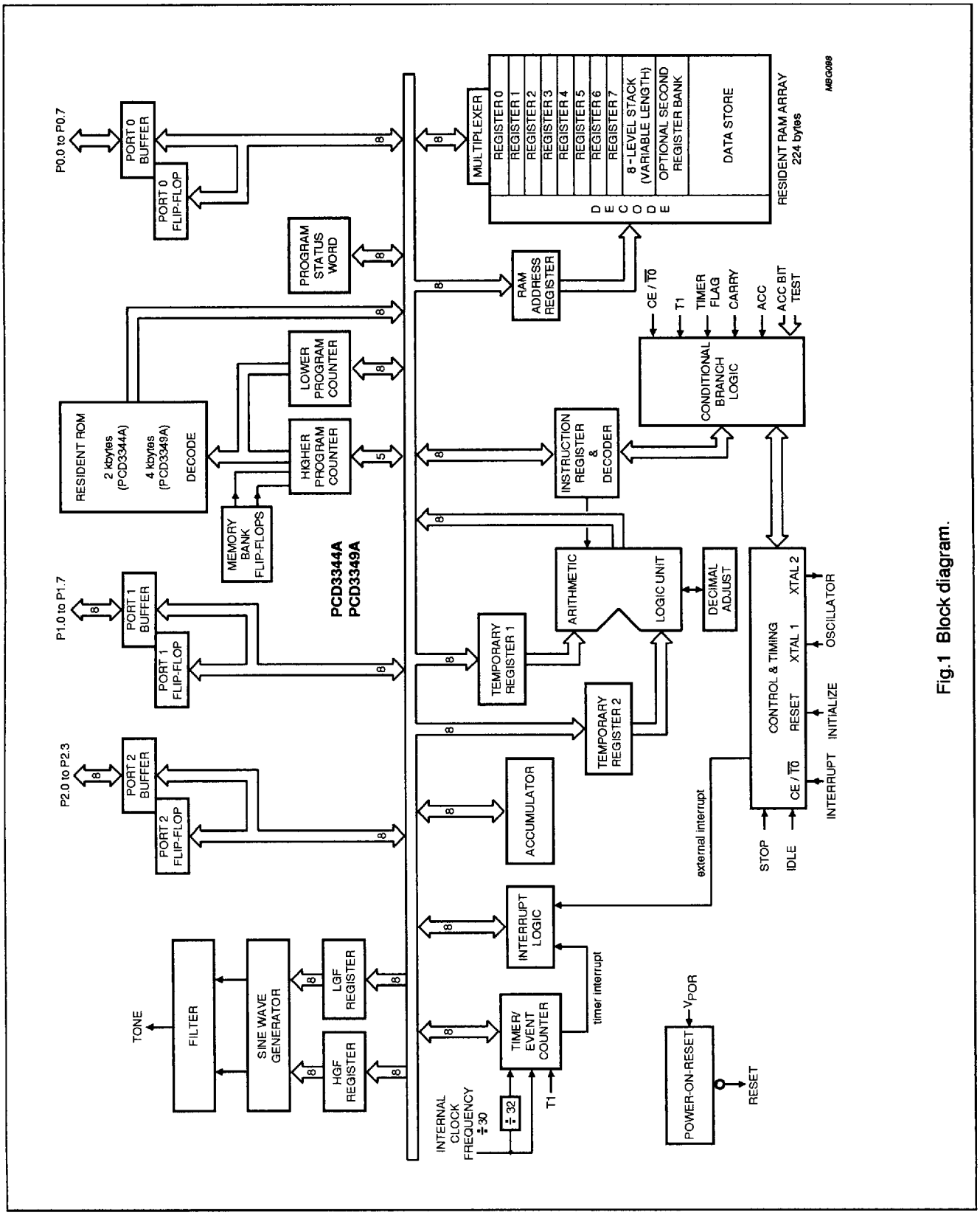


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

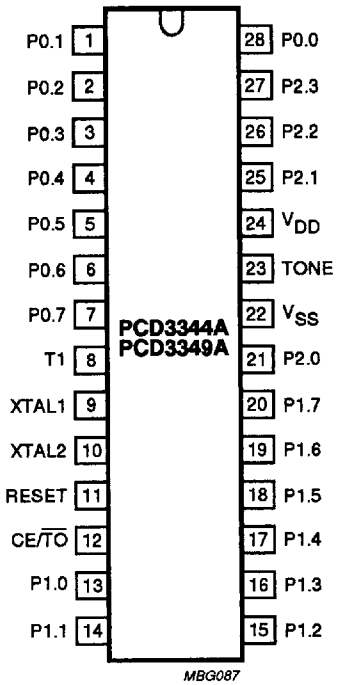


Fig.2 Pin configuration (SOT117-1 and SOT136-1).

5.2 Pin description

Table 1 SOT117-1 and SOT136-1 packages

SYMBOL	PIN	DESCRIPTION
P0.0 to P0.7	28, 1 to 7	Port 0: 8 quasi-bidirectional I/O lines
T1	8	Test 1 or count input of 8-bit timer/event counter 1
XTAL1	9	crystal oscillator or external clock input
XTAL2	10	crystal oscillator output
RESET	11	reset input
CE/$\overline{T0}$	12	Chip Enable or Test 0
P1.0 to P1.7	13 to 20	Port 1: 8 quasi-bidirectional I/O lines
P2.0 to P2.3	21, 25, 26, 27	Port 2: 4 quasi-bidirectional I/O lines
V_{SS}	22	ground
TONE	23	DTMF output
V_{DD}	24	positive supply voltage

6 FREQUENCY GENERATOR

A versatile frequency generator section is provided (see Fig.3). For normal operation, use a 3.58 MHz quartz crystal or PXE resonator. The frequency generator includes precision circuitry for dual tone multifrequency (DTMF) signals, which is typically used for tone dialling telephone sets.

The TONE output can alternatively issue twelve modem frequencies for data rates between 300 and 1200 bits/s.

In addition to DTMF and modem frequencies, two octaves of musical scale in steps of semitones are available.

6.1 Frequency generator derivative registers

Table 2 gives the derivative addresses, mnemonics and access types of the frequency generator derivative registers. The addresses 03H to FFH are not used.

Table 2 Addresses of the frequency generator derivative registers

ADDRESS	REGISTER	7	6	5	4	3	2	1	0
01H	HGF[1]	H7	H6	H5	H4	H3	H2	H1	H0
02H	LGF[2]	L7	L6	L5	L4	L3	L2	L1	L0

Notes

1. HGF = High Group Frequency; access type W.
2. LGF = Low Group Frequency; access type W.

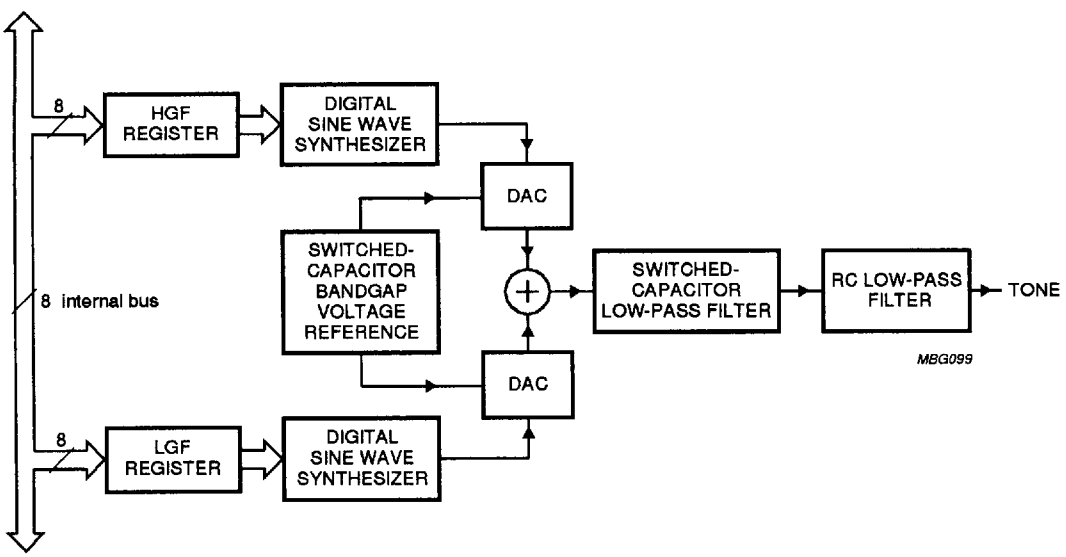


Fig.3 Block diagram of the frequency generator section.

6.2 Frequency registers

The two frequency registers HGF and LGF define two frequencies. From these, the digital sine synthesizers together with the Digital-to-Analog Converters (DACs) construct two sine waves. Their amplitudes are precisely scaled according to the bandgap voltage reference. This ensures TONE output levels independent of supply voltage and temperature. The amplitude of the Low group frequency sine wave is attenuated by 2 dB compared to the amplitude of the High group frequency sine wave.

The two sine waves are summed and then filtered by an on-chip switched capacitor and RC low-pass filters. These guarantee that all DTMF tones generated fulfil the CEPT recommendations with respect to amplitude, frequency deviation, total harmonic distortion and suppression of unwanted frequency components.

The value 00H in a frequency register stops the corresponding digital sine synthesizer. If both frequency registers contain 00H, the whole frequency generator is shut off, resulting in lower power consumption.

The frequency of the sine wave generated is dependent upon the decimal value 'x' held in the frequency registers (HGF and LGF), and this may be calculated as follows:

$$f = \frac{f_{xtal}}{[23\,(x+2)]}; \text{ where } 60 \leq x \leq 255.$$

The frequency limitation given by $x \geq 60$ is due to the low-pass filters which would attenuate higher frequency sine waves.

6.3 DTMF frequencies

Assuming an oscillator frequency f_{xtal} = 3.58 MHz, the DTMF standard frequencies can be implemented as shown in Table 3.

The relationship between telephone keyboard symbols and the frequency register contents are given in Table 4.

Table 3 DTMF standard frequencies and their implementation; value = LGF, HGF contents

VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	STANDARD	GENERATED	(%)	(Hz)
DD	697	697.90	0.13	0.90
C8	770	770.46	0.06	0.46
B5	852	850.45	−0.18	−1.55
A3	941	943.23	0.24	2.23
7F	1209	1206.45	−0.21	−2.55
72	1336	1341.66	0.42	5.66
67	1477	1482.21	0.35	5.21
5D	1633	1638.24	0.32	5.24

Table 4 Dialling symbols, corresponding DTMF frequency pairs and frequency registers content

TELEPHONE KEYBOARD SYMBOLS	DTMF FREQ. PAIRS (Hz)	LGF VALUE (HEX)	HGF VALUE (HEX)
0	(941, 1336)	A3	72
1	(697, 1209)	DD	7F
2	(697, 1336)	DD	72
3	(697, 1477)	DD	67
4	(770, 1209)	C8	7F
5	(770, 1336)	C8	72
6	(770, 1477)	C8	67
7	(852, 1209)	B5	7F
8	(852, 1336)	B5	72
9	(852, 1477)	B5	67
A	(697, 1633)	DD	5D
B	(770, 1633)	C8	5D
C	(852, 1633)	B5	5D
D	(941, 1633)	A3	5D
•	(941, 1209)	A3	7F
#	(941, 1477)	A3	67

6.4 Modem frequencies

Again assuming an oscillator frequency f_{xtal} = 3.58 MHz, the standard modem frequency pairs summarized in Table 5 can be implemented. It is suggested to define the frequency by the HGF register while the LGF register contains 00H, disabling Low group frequency generation.

Table 5 Standard modem frequency pairs and their implementation

HGF VALUE (HEX)	FREQUENCY (Hz)		DEVIATION	
	MODEM	GENERATED	(%)	(Hz)
9D	980[1]	978.82	−0.12	−1.18
82	1180[1]	1179.03	−0.08	−0.97
8F	1070[2]	1073.33	0.31	3.33
79	1270[2]	1265.30	−0.37	−4.70
80	1200[3]	1197.17	−0.24	−2.83
45	2200[3]	2192.01	−0.36	−7.99
76	1300[4]	1296.94	−0.24	−3.06
48	2100[4]	2103.14	0.15	3.14
5C	1650[1]	1655.66	0.34	5.66
52	1850[1]	1852.77	0.15	2.77
4B	2025[2]	2021.20	−0.19	−3.80
44	2225[2]	2223.32	−0.08	−1.68

Notes

1. Standard is V.21.
2. Standard is Bell 103.
3. Standard is Bell 202.
4. Standard is V.23.

6.5 Musical scale frequencies

Finally, two octaves of musical scale in steps of semitones can be realized, again assuming an oscillator frequency f_{xtal} = 3.58 MHz (Table 6). It is suggested to define the frequency by the HGF register while the LGF contains 00H, disabling Low group frequency generation.

Table 6 Musical scale frequencies and their implementation

NOTE	HGF VALUE (HEX)	FREQUENCY (Hz)	
		STANDARD[1]	GENERATED
D#5	F8	622.3	622.5
E5	EA	659.3	659.5
F5	DD	698.5	697.9
F#5	D0	740.0	741.1
G5	C5	784.0	782.1
G#5	B9	830.6	832.3
A5	AF	880.0	879.3
A#5	A5	923.3	931.9
B5	9C	987.8	985.0
C6	93	1046.5	1044.5
C#6	8A	1108.7	1111.7
D6	82	1174.7	1179.0
D#6	7B	1244.5	1245.1
E6	74	1318.5	1318.9
F6	6D	1396.9	1402.1
F#6	67	1480.0	1482.2
G6	61	1568.0	1572.0
G#6	5C	1661.2	1655.7
A6	56	1760.0	1768.5
A#6	51	1864.7	1875.1
B6	4D	1975.5	1970.0
C7	48	2093.0	2103.3
C#7	44	2217.5	2223.3
D7	40	2349.3	2358.1
D#7	3D	2489.0	2470.4

Note

1. Standard scale based on A4 @ 440 Hz.

7 TIMING

Although the PCD3344A and PCD3349A operate over a clock frequency range from 1 to 16 MHz, f_{xtal} = 3.58 MHz will usually be chosen to take full advantage of the frequency generator section.

8 RESET

In addition to the conditions given in the PCD33XXA family data sheet, all derivative registers are cleared in the RESET state.

9 STOP MODE

Since the oscillator is switched off, the frequency generator receives no clock. It is suggested to clear both the HGF and LGF registers before entering Stop mode. This will cut-off the biasing of the internal amplifiers, considerably reducing current requirements.

10 IDLE MODE

In the Idle mode, the frequency generator remains operative.

11 INSTRUCTION SET RESTRICTIONS

Since no serial I/O interface is provided, the serial I/O (Input/Output) instructions are not available. 'Mov Dx, A' is the only applicable derivative instruction because the derivative registers are write-only.

ROM space being restricted to 2 kbytes (PCD3344A) and 4 kbytes (PCD3349A) respectively, SEL MB1 (for PCD3344A) and SEL MB2/3 (for both PCD3344A and PCD3349A) would define non-existing Program Memory banks and should therefore be avoided.

RAM space being restricted to 224 bytes, care should be taken to avoid accesses to non-existing RAM locations.

12 SUMMARY OF MASK OPTIONS

Table 7 Port mask options

PORT NAME	PORT OUTPUT DRIVE[1]			PORT STATE AFTER RESET	
	OPTION 1	OPTION 2	OPTION 3	SET	RESET
Port 0 (P0.0 to P0.7)	X	X	X	X	X
Port 1 (P1.0 to P1.7)	X	X	X	X	X
Port 2 (P2.0 to P2.3)	X	X	X	X	X

Notes

1. Port output drives:
   a) Option 1: standard I/Ot.
   b) Option 2: open-drain I/O.
   c) Option 3: push-pull output. see *"PCD33xxA Family"* data sheet.
2. Port state after reset: S = Set (HIGH) and R = Reset (LOW).

Table 8 Mask options

FEATURE	DESCRIPTION
ROM Code: program/data	Any mix of instructions and data up to ROM size of 2 kbytes (PCD3344A) and 4 kbytes (PCD3349A).
Power-on-reset voltage level: V_{POR}	1.2 to 3.6 V in increments of 100 mV; OFF
Oscillator transconductance: g_m	LOW transconductance: g_{mL}
	MEDIUM transconductance: g_{mM}
	HIGH transconductance: g_{mH}

13 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); see note 1 and 2.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	−0.5	+7.0	V
V_I	all input voltages	−0.5	V_{DD} + 0.5	V
I_I, I_O	DC input or output current	−10	+10	mA
P_{tot}	total power dissipation	−	125	mW
P_O	power dissipation per output	−	30	mW
I_{SS}	ground supply current	−50	+50	mA
T_{stg}	storage temperature	−65	+150	°C
T_j	operating junction temperature	−	90	°C

Notes

1. Stresses above those listed under Limiting Values may cause permanent damage to the device.
2. Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

14 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices (see *"Handling MOS devices"*).

15 DC CHARACTERISTICS

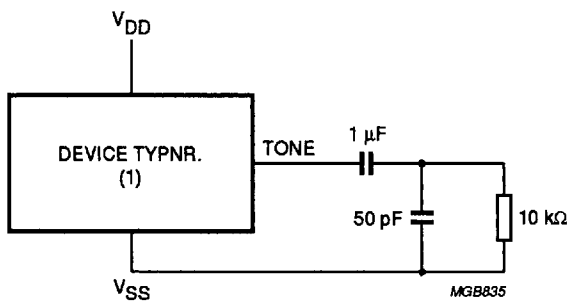
V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; f_{xtal} = 3.58 MHz (g_{mL}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply (see Figs 5 to 9)						
V_{DD}	supply voltage operating; note 1 RAM data retention in Stop mode		 1.8 1.0	 − −	 6 6	 V V
I_{DD}	operating supply current; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	−	0.9	1.8	mA
		V_{DD} = 3 V	−	0.3	0.6	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	−	1.1	3.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	−	1.7	5.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	−	2.5	6.0	mA
$I_{DD(ID)}$	supply current Idle mode; note 2	V_{DD} = 3 V; value HGF ≠ 0 and/or LGF ≠ 0	−	0.7	1.4	mA
		V_{DD} = 3 V; value HGF = LGF =0	−	0.2	0.4	mA
		V_{DD} = 5 V; f_{xtal} = 10 MHz (g_{mL})	−	0.8	1.6	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mM})	−	1.2	4.0	mA
		V_{DD} = 5 V; f_{xtal} = 16 MHz (g_{mH})	−	1.7	5.0	mA
$I_{DD(ST)}$	supply current Stop mode	V_{DD} = 1.8 V; T_{amb} = 25 °C; note 3	−	1.0	2.5	µA
		V_{DD} = 1.8 V; T_{amb} = 70 °C; note 3	−	−	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{IL}	input leakage current	$V_{SS} \leq V_I \leq V_{DD}$	–1	–	+1	µA
Port outputs (see Figs 10 to 12)						
I_{OL}	LOW level port sink current	V_{DD} = 3 V; V_O = 0.4 V	0.7	3.5	–	mA
I_{OH}	HIGH level port pull-up source current	V_O = 2.7 V; V_{DD} = 3 V	–10	–20	–	µA
		V_O = 0 V; V_{DD} = 3 V	–	–100	–300	µA
I_{OH}	HIGH level port push-pull source current	V_{DD} = 3 V; V_O = 2.6 V	–0.7	–4	–	mA
TONE output (see Fig.4; notes 1 and 4)						
V_{HGrms}	HGF voltage (RMS)		158	181	205	mV
V_{LGrms}	LGF voltage (RMS)		125	142	160	mV
$\Delta f/f$	frequency deviation		–0.6	–	0.6	%
V_{DC}	DC voltage level		–	$0.5V_{DD}$	–	V
$\|Z_O\|$	output impedance		–	100	500	Ω
V_G	pre-emphasis of group		1.5	2.0	2.5	dB
THD	total harmonic distortion	T_{amb} = 25 °C; note 5	–	25	–	dB
Power-on-reset						
ΔV_{POR}	Power-on-reset level variation around chosen V_{POR}	note 6	–0.5	0	+0.5	V

Notes

1. TONE output requires $V_{DD} \geq 2.5$ V.
2. $V_{IL} = V_{SS}$; $V_{IH} = V_{DD}$; open-drain outputs connected to V_{SS}; all other outputs open; value HGF = LGF = 0, unless otherwise specified.
3. Crystal connected between XTAL1 and XTAL2; pins T1 and CE/$\overline{T0}$ at V_{SS}; value HGF = LGF = 0.
4. Values are specified for DTMF frequencies only (CEPT).
5. Related to the Low group frequency (LGF) component (CEPT).
6. V_{POR} is an option chosen by the user. Depending on its value, it may restrict the supply voltage range.



(1) Device typenr.: PCD3344A or PCD3349A

Fig.4 TONE output test circuit.

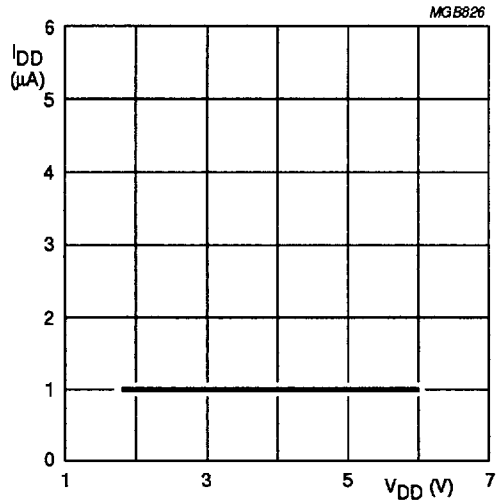
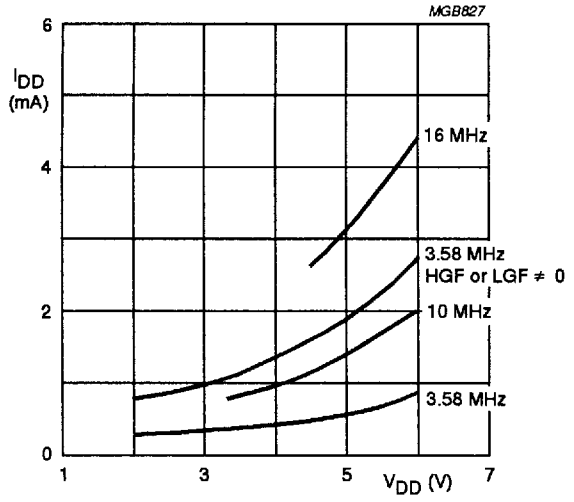
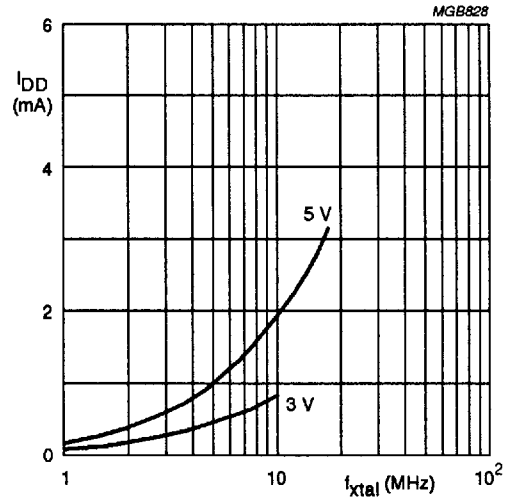


Fig.5 Typical supply current (I_{DD}) in Stop mode as a function of supply voltage (V_{DD}).



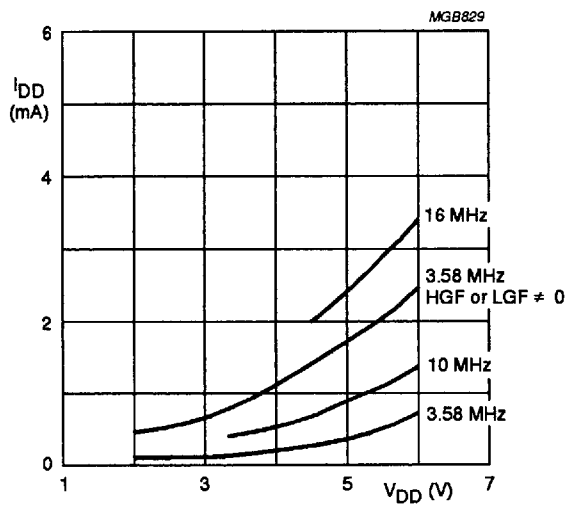
Measured with crystal between XTAL1 and XTAL2.

Fig.6 Typical operating supply current (I_{DD}) as a function of supply voltage (V_{DD}).



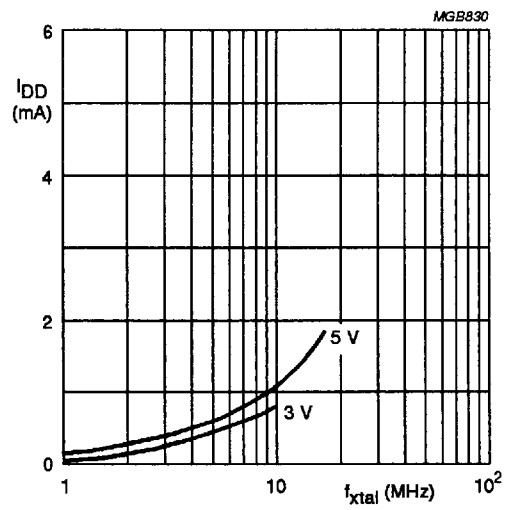
Measured with function generator on XTAL1.

Fig.7 Typical operating supply current (I_{DD}) as a function of clock frequency (f_{xtal}).



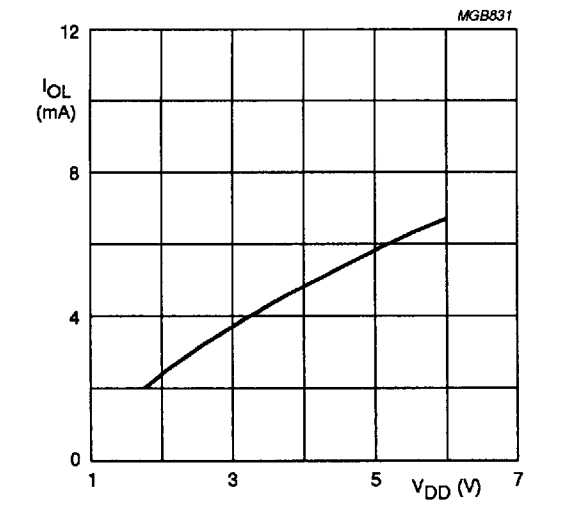
Measured with crystal between XTAL1 and XTAL2.

Fig.8 Typical supply current (I_{DD}) in Idle mode as a function of supply voltage (V_{DD}).



Measured with function generator on XTAL1.

Fig.9 Typical supply current (I_{DD}) in Idle mode as a function of clock frequency (f_{xtal}).



V_O = 0.4 V.

Fig.10 Typical LOW level port output sink current (I_{OL}) as a function of supply voltage (V_{DD}).

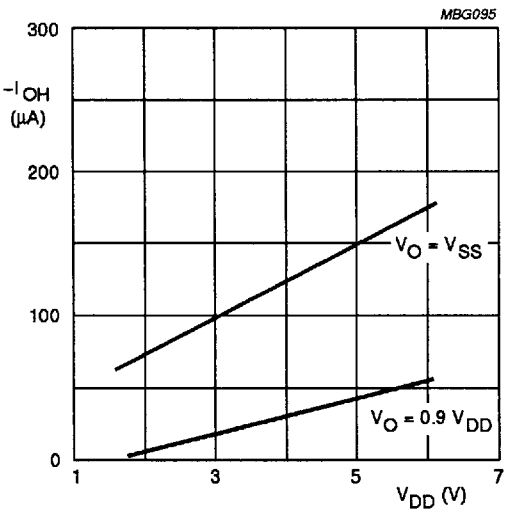
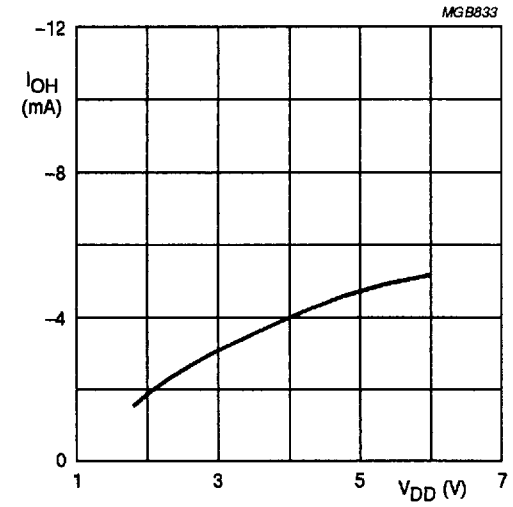


Fig.11 Typical HIGH level output pull-up source current (I_{OH}) as a function of supply voltage (V_{DD}).



$V_O = V_{DD} - 0.4$ V.

Fig.12 Typical HIGH level push-pull output source current (I_{OH}) as a function of supply voltage (V_{DD}).

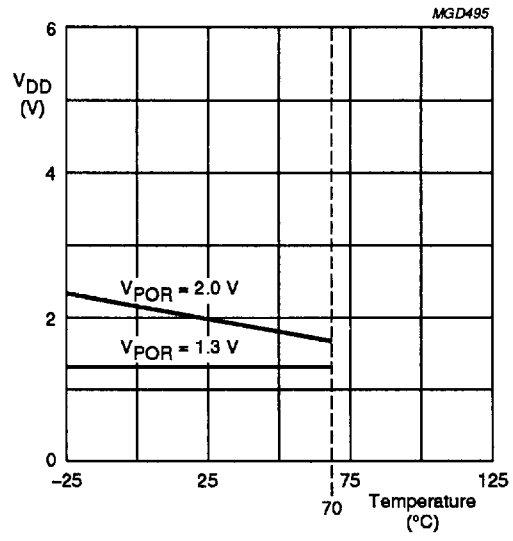


Fig.13 Typical Power-on-reset level (V_{POR}) as function of temperature.

16 AC CHARACTERISTICS

V_{DD} = 1.8 to 6 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_r	rise time all outputs	V_{DD} = 5 V; T_{amb} = 25 °C; C_L = 50 pF	–	30	–	ns
t_f	fall time all outputs		–	30	–	ns
f_{xtal}	clock frequency	see Fig.14	1	–	16	MHz
Oscillator (see Fig.15)						
g_{mL}	LOW transconductance	V_{DD} = 5 V	0.2	0.4	1.0	mS
g_{mM}	MEDIUM transconductance		0.9	1.6	3.2	mS
g_{mH}	HIGH transconductance		3.0	4.5	9.0	mS
R_F	feedback resistor		0.3	1.0	3.0	MΩ

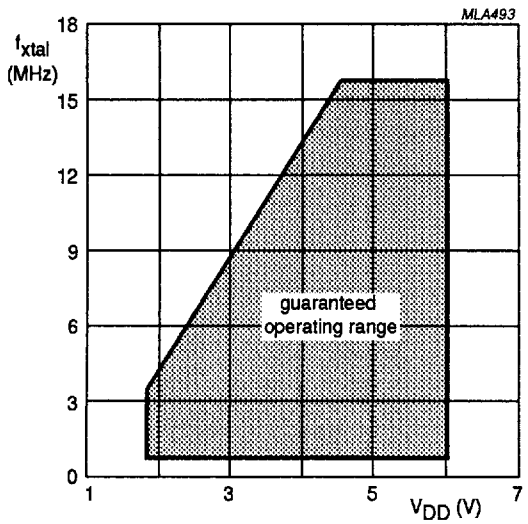


Fig.14 Maximum clock frequency (f_{xtal}) as a function of supply voltage (V_{DD}).

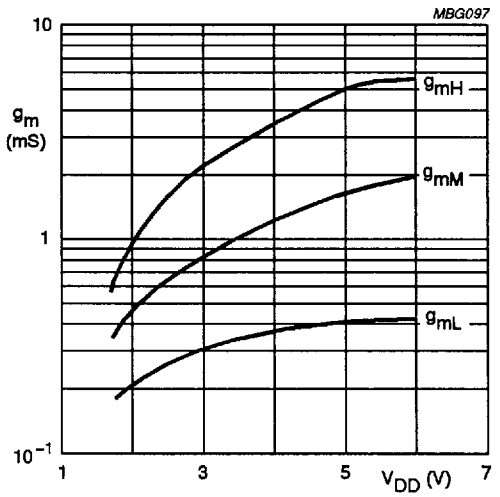
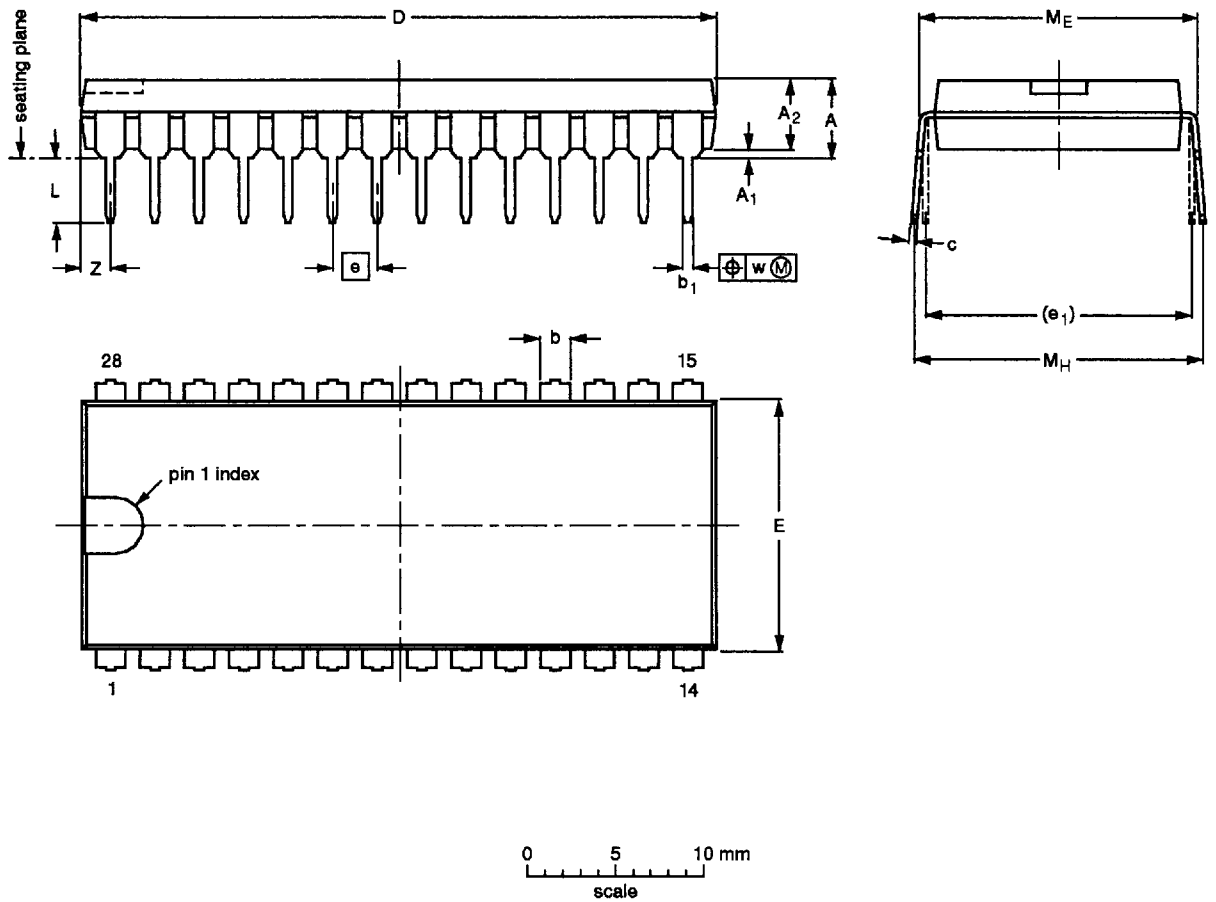


Fig.15 Typical transconductance as a function of supply voltage (V_{DD}).

17 PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil) **SOT117-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

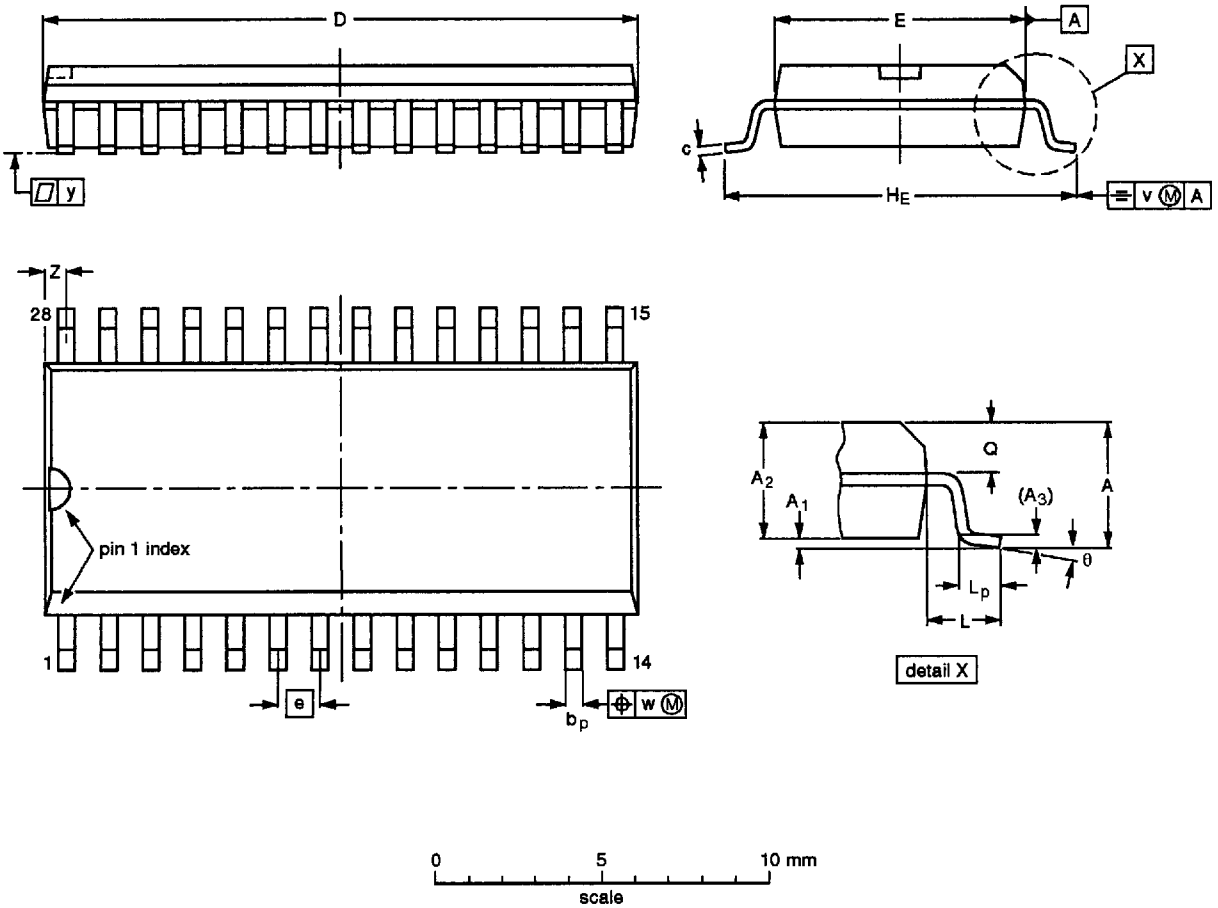
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	36.0 35.0	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	1.7
inches	0.20	0.020	0.16	0.066 0.051	0.020 0.014	0.013 0.009	1.41 1.34	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.067

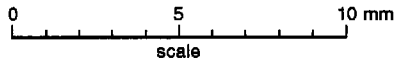
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT117-1	051G05	MO-015AH				~~92-11-17~~ 95-01-14

SO28: plastic small outline package; 28 leads; body width 7.5 mm **SOT136-1**





DIMENSIONS (Inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	18.1 17.7	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.71 0.69	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT136-1	075E06	MS-013AE				~~91-08-13~~ 95-01-24

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

18.2 DIP

18.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

18.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

18.3 SO

18.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

18.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.