National Semiconductor

54LS165/DM74LS165 8-Bit Parallel In/Serial Output Shift Registers

General Description

This device is an 8-bit serial shift register which shifts data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high.

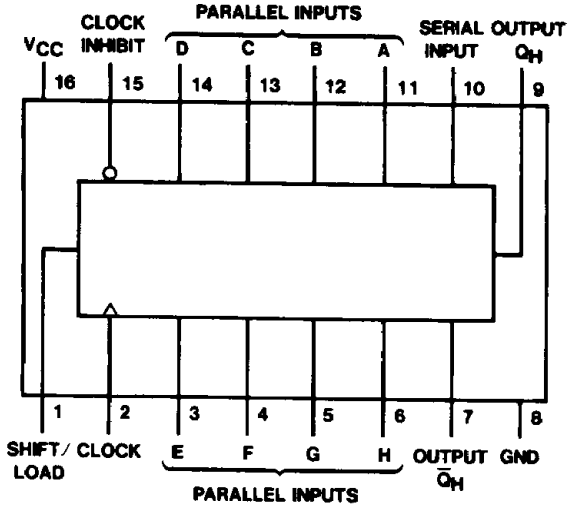
Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

Connection Diagram

Dual-In-Line Package



TL/F/6399–1

Order Number 54LS165DMQB, 54LS165FMQB, DM74LS165WM or DM74LS165N
See NS Package Number J16A, M16B, N16E or W16A

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a...h = The level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		54LS165			DM74LS165			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)				30	0		25	MHz
f_{CLK}	Clock Frequency (Note 2)					0		20	MHz
t_W	Pulse Width (Note 2)	Clock	18			25			ns
		Load	15			15			
t_{SU}	Setup Time (Note 6)	Parallel	10			10			ns
		Serial	10			20			
		Enable	10			30			
		Shift	10			45			
t_H	Hold Time (Note 6)		5			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	54LS	2.5			V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	54LS			0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min			0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V (DM74), V_I = 10V (54LS)	Shift/Load			0.3	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Shift/Load			60	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Shift/Load			−1.2	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	54LS	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			21	36	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 3: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

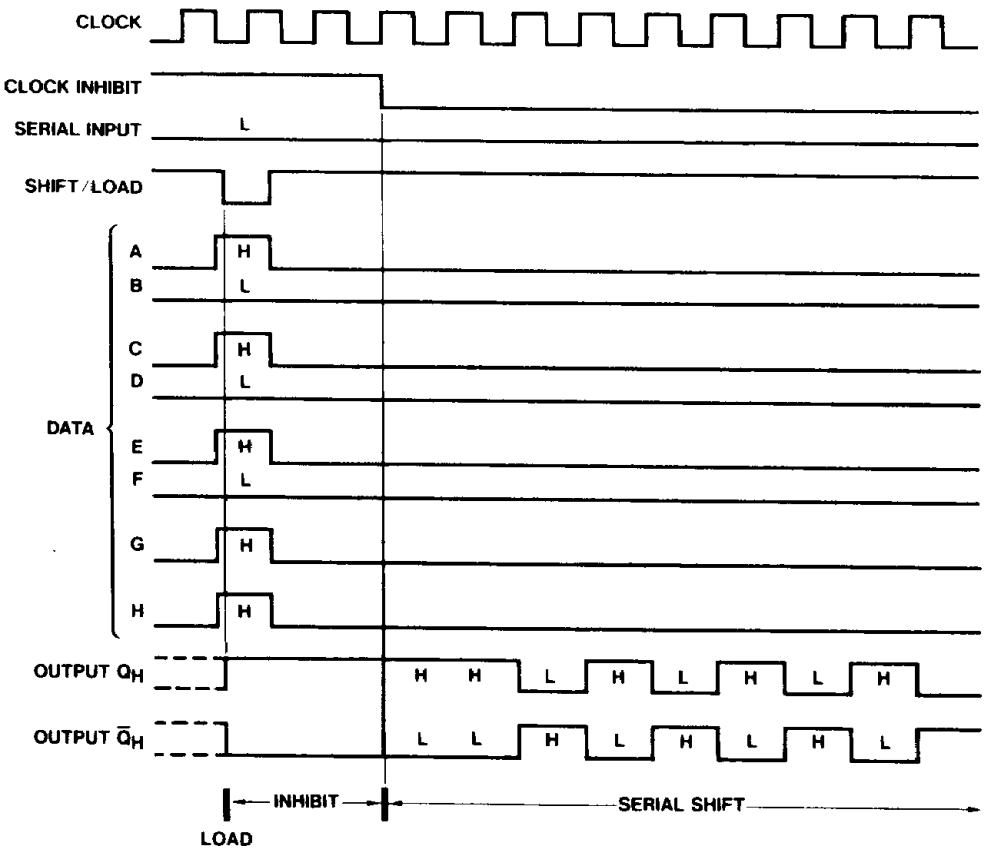
Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	54LS C_L = 15 pF		DM74LS R_L = 2 kΩ C_L = 50 pF		Units
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		30		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		30		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		30		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		30		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to Q_H		20		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to Q_H		30		37	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		25		32	ns

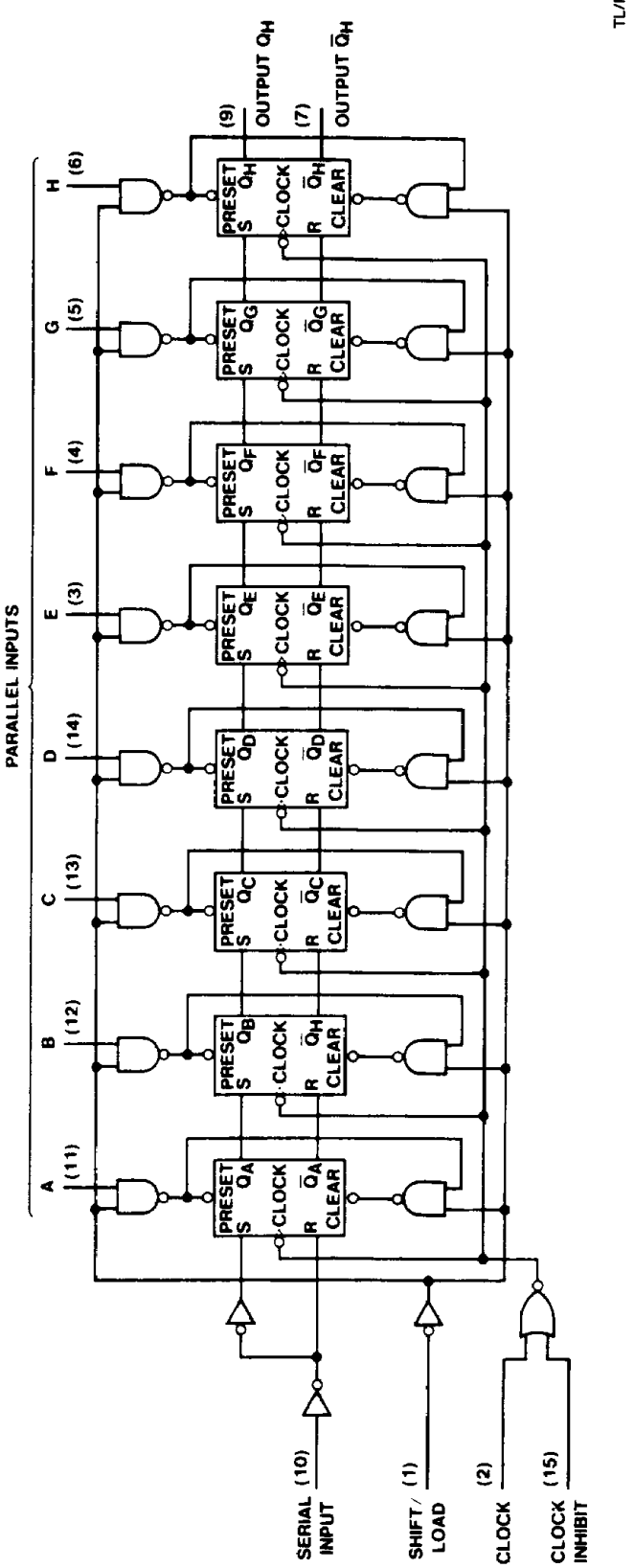
Timing Diagram

Typical Shift, Load, and Inhibit Sequences



TL/F/6399–3

Logic Diagram



TL/F/6399–2