



CY54/74FCT138T

1-of-8 Decoder

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.0 ns max. (Com'l), FCT-A speed at 5.8 ns max. (Com'l)
- Reduced V_{OH} (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V
- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Extended commercial range of -40°C to $+85^{\circ}\text{C}$
- Sink current 64 mA (Com'l), 32 mA (Mil)

Source current 32 mA (Com'l),
12 mA (Mil)

- Dual 1-of-8 decoder with enables

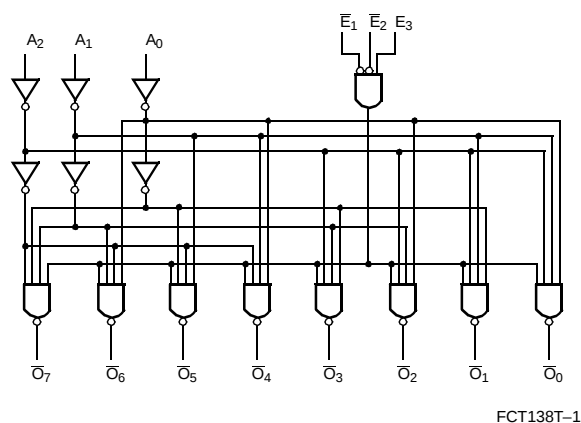
Functional Description

The FCT138T is a 1-of-8 decoder. The FCT138T accepts three binary weighted inputs (A_0 , A_1 , A_2) and, when enabled, provides eight mutually exclusive active LOW outputs ($\bar{O}_0$ – $\bar{O}_7$). The FCT138T features three enable inputs, two active LOW ($\bar{E}_1$, $\bar{E}_2$) and one active HIGH (E_3).

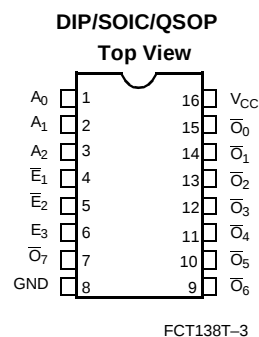
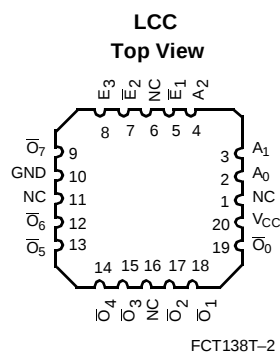
All inputs will be HIGH unless $\bar{E}_1$ and $\bar{E}_2$ are LOW and E_3 is HIGH. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four FCT138T devices and one inverter.

The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram



Pin Configurations



Pin Description

Name	Description
A	Address Inputs
$\bar{E}_1$ – $\bar{E}_2$	Enable Inputs (Active LOW)
E_3	Enable Input (Active HIGH)
O	Outputs

Function Table^[1]

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Maximum Ratings^[2, 3]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with

Power Applied..... -65°C to +135°C

Supply Voltage to Ground Potential -0.5V to +7.0V

DC Input Voltage..... -0.5V to +7.0V

DC Output Voltage..... -0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin)..... 120 mA

Power Dissipation..... 0.5W

Static Discharge Voltage >2001V
(per MIL-STD-883, Method 3015)

Operating Range

Range	Range	Ambient Temperature	V _{CC}
Commercial	All	-40°C to +85°C	5V ± 5%
Military ^[4]	All	-55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-32 mA	2.0			V
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-15 mA	2.4	3.3		V
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-12 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.3	0.55	V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =32 mA		0.3	0.55	V
V _{IH}	Input HIGH Voltage		2.0			V
V _{IL}	Input LOW Voltage				0.8	V
V _H	Hysteresis ^[6]	All inputs		0.2		V
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _I	Input HIGH Current	V _{CC} =Max., V _{IN} =V _{CC}			5	μA
I _{IH}	Input HIGH Current	V _{CC} =Max., V _{IN} =2.7V			±1	μA
I _{IL}	Input LOW Current	V _{CC} =Max., V _{IN} =0.5V			±1	μA
I _{OS}	Output Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =0.0V	-60	-120	-225	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} =4.5V			±1	μA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
2. Unless otherwise noted, these limits are over the operating free-air temperature range.
3. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
4. T_A is the "instant on" case temperature.
5. Typical values are at V_{CC}=5.0V, T_A=+25°C ambient.
6. This parameter is guaranteed but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

Capacitance^[6]

Parameter	Description	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	5	10	pF
C _{OUT}	Output Capacitance	9	12	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Typ. ^[5]	Max.	Unit
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V, V _{IN} ≥V _{CC} -0.2V	0.1	0.2	mA
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs)	V _{CC} =Max., V _{IN} =3.4V, ^[8] f ₁ =0, Outputs Open	0.5	2.0	mA
I _{CCD}	Dynamic Power Supply Current ^[9]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.06	0.12	mA/MHz
I _C	Total Power Supply Current ^[10]	V _{CC} =Max., f ₁ =10 MHz, 50% Duty Cycle, Outputs Open, Toggle E ₁ , E ₂ , or E ₃ , One Output Toggling, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	0.7	1.4	mA
		V _{CC} =Max., f ₁ =10 MHz, 50% Duty Cycle, Outputs Open, Toggle E ₁ , E ₂ , or E ₃ , One Output Toggling, V _{IN} =3.4V or V _{IN} =GND	1.0	2.4	mA

Notes:

8. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.

Switching Characteristics Over the Operating Range

Parameter	Description	FCT138T				FCT138AT				Unit	Fig. No. ^[12]
		Military		Commercial		Military		Commercial			
		Min. ^[11]	Max.	Min. ^[11]	Max.	Min. ^[11]	Max.	Min. ^[11]	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to $\bar{O}$	1.5	12.0	1.5	9.0	1.5	7.8	1.5	5.8	ns	1, 2
t _{PLH} t _{PHL}	Propagation Delay $\bar{E}_1$ or $\bar{E}_2$ to $\bar{O}$	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay E ₃ to $\bar{O}$	1.5	12.5	1.5	9.0	1.5	8.0	1.5	5.9	ns	1, 5

Parameter	Description	FCT138CT				Unit	Fig. No. ^[12]
		Military		Commercial			
		Min. ^[11]	Max.	Min. ^[11]	Max.		
t _{PLH} t _{PHL}	Propagation Delay A to $\overline{O}$	1.5	6.0	1.5	5.0	ns	1, 2
t _{PLH} t _{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}$	1.5	6.1	1.5	5.0	ns	1, 5
t _{PLH} t _{PHL}	Propagation Delay E ₃ to $\overline{O}$	1.5	6.1	1.5	5.0	ns	1, 5

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.0	CY74FCT138CTQC	Q1	16-Lead (150-Mil) QSOP	Commercial
	CY74FCT138CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
5.8	CY74FCT138ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT138ATQC	Q1	16-Lead (150-Mil) QSOP	
	CY74FCT138ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
6.0	CY54FCT138CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT138CTLMB	L61	20-Pin Square Leadless Chip Carrier	
9.0	CY74FCT138TSOC	S1	16-Lead (300-Mil) Molded SOIC	Commercial

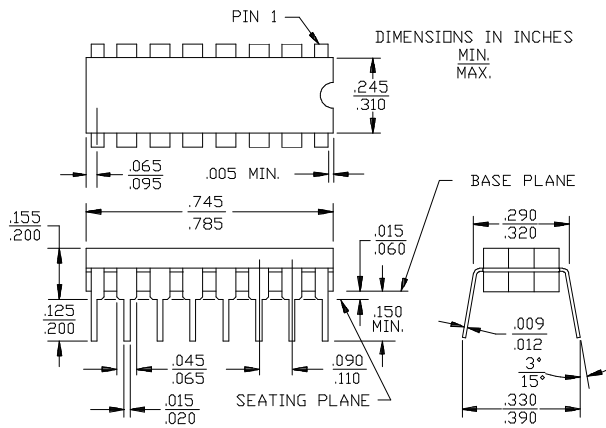
Notes:

11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. See "Parameter Measurement Information" in the General Information Section.

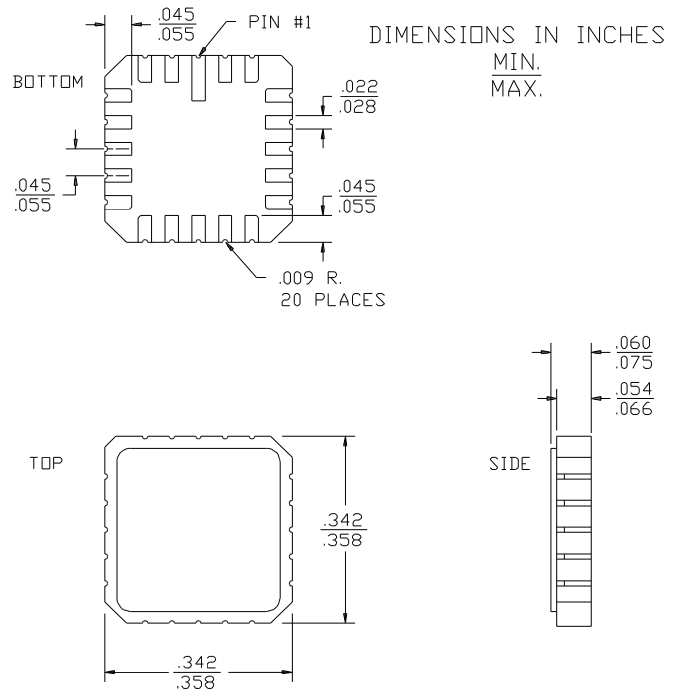
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Package Diagrams

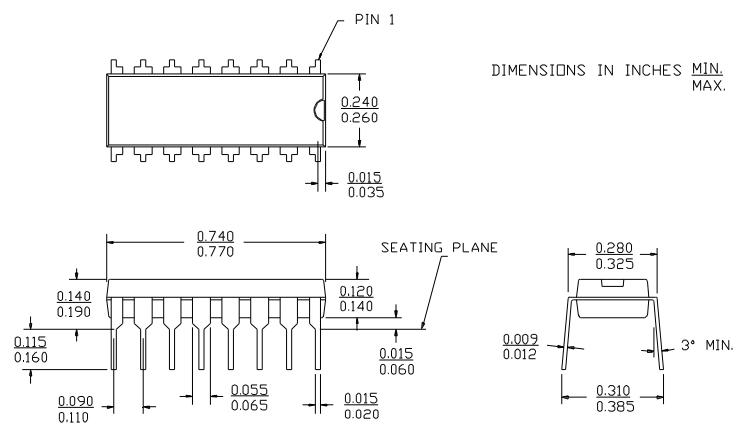
16-Lead (300-Mil) CerDIP D2
MIL-STD-1835 D-2 Config.A

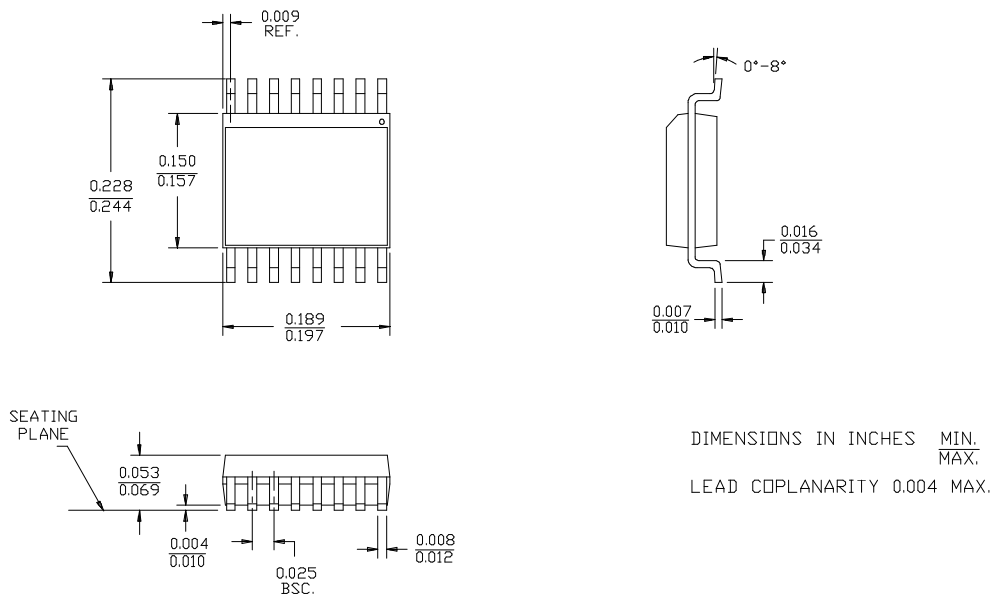


20-Pin Square Leadless Chip Carrier L61
MIL-STD-1835 C-2A



16-Lead (300-Mil) Molded DIP P1



Package Diagrams (continued)
16-Lead Quarter Size Outline Q1

16-Lead Molded SOIC S1
