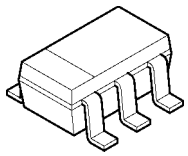
Under Development

RF AMPLIFIER FOR VHF/UHF(LOW) BAND

■ GENERAL DESCRIPTION

The **NJM2275** is a low current, low voltage RF amplifier, especially designed for VHF/UHF(low) band.
The center frequency of this narrow band amplifier is changed by external components.

■ PACKAGE OUTLINE

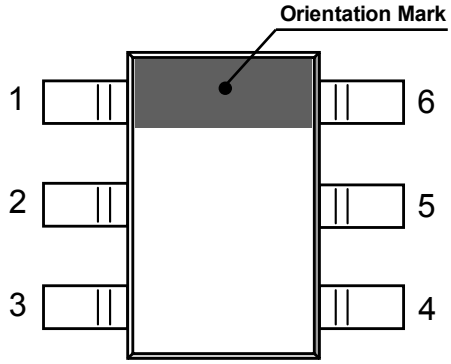


NJM2275F

■ FEATURES

- Wide Operating Voltage 1.8V to 6V
- Low Operating Current 0.8mA type. at V^+ =1.9V, 400MHz input
- High Gain
  - Power Gain 15dB (1.9V, 400MHz input)
  - Voltage Gain 30dB (1.9V, 400MHz input, 1kΩ load)
- Operating Frequency band VHF to UHF(Low)
- High Isolation 26dB(OUT to IN, 400MHz)
- Bipolar Technology
- Package Outline MTP6

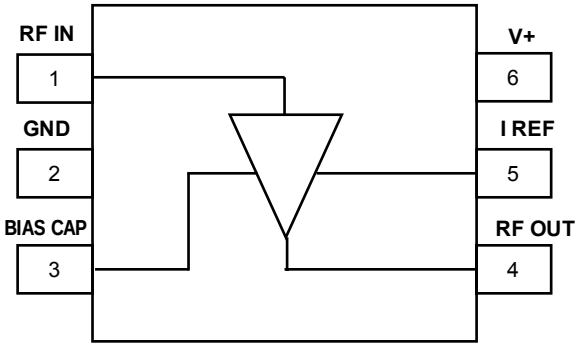
■ PIN CONFIGULATION



Top View

Pin Function
1. RF IN
2. GND
3. BIAS CAP
4. RF OUT
5. IREF
6. V+

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	10.0	V
Power Dissipation	P d	200	mW
Operating Temperature	T o p r	- 40 to +85	°C
Storage Temperature	T s t g	- 40 to +125	°C

■ RECOMMENDED OPERATING CONDITION (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V^+		1.8	1.9	6.0	V

■ ELECTRICAL CHARACTERISTICS

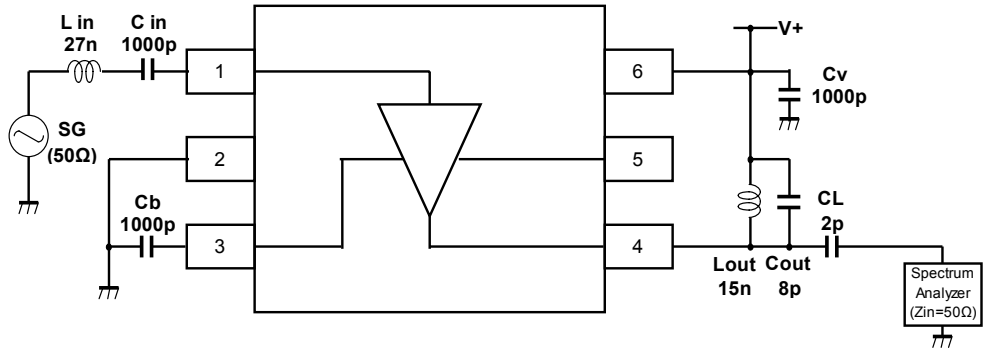
(Ta=25°C, V^+=1.9V, fin=400MHz, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Current Consumption	I c c	No signal	-	0.8	1.0	mA
Power Gain	PG	Pin= - 40dBm Test circuit1	-	15	-	dB
Voltage Gain	VG	Pin= - 40dBm Test circuit2	-	30	-	dB
Noise Figure	NF	Test Circuit1	-	2.2	-	dB
Input Return Loss	$\|S11\|^2$	Pin= - 40dBm Test Circuit1	-	- 7	-	dB
Output Return Loss	$\|S22\|^2$	Pin= - 40dBm Test Circuit1	-	- 7	-	dB
RF OUT - RF IN Isolation	ISL	Pin= - 40dBm Test Circuit1	-	26	-	dB
Power Input at 1dB compression Point	P–1dB	Test Circuit1	-	- 28	-	dBm

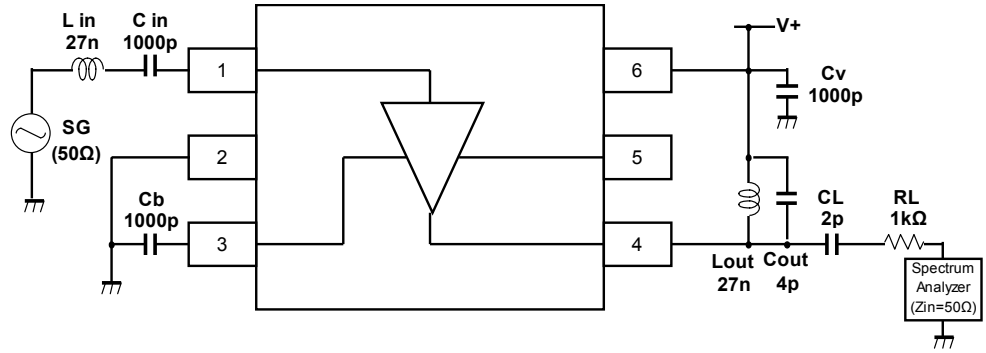
■ TEST CIRCUIT

This test circuit allows the measurement of all parameters described in “ELECTRICAL CHARACTERISTICS”.

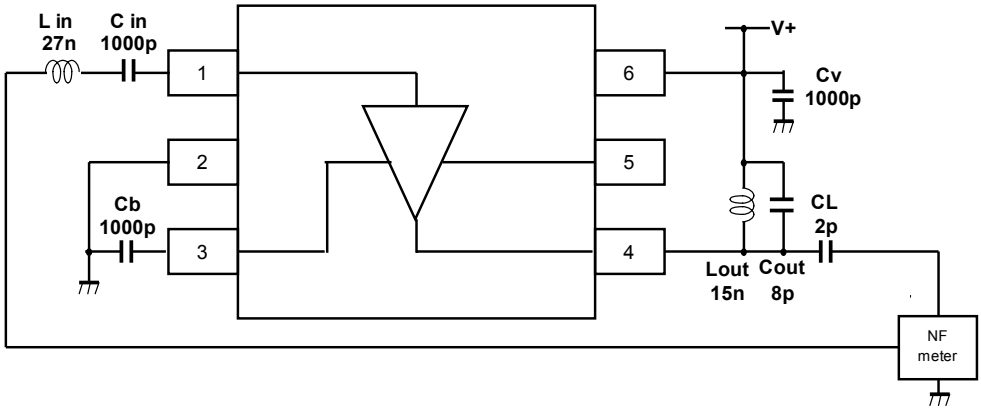
- **Test Circuit 1** : PG , $IS11I^2$, $IS22I^2$, P–1dB , Output Level versus Input Level



- **Test Circuit 2** : VG , Output Level versus Input Level



- **Test Circuit 3 :** Power Gain versus Input signal Frequency



PG and PG shown in “Output level versus Input Level” are given by ,

PG = Pout – Pin

VG = (Pout + Prl) – Pin

Prl is caused by the voltage drop of RL. RL is 1000 Ω. The input impedance of spectrum analyzer Zin is 50Ω. Prl is calculated from

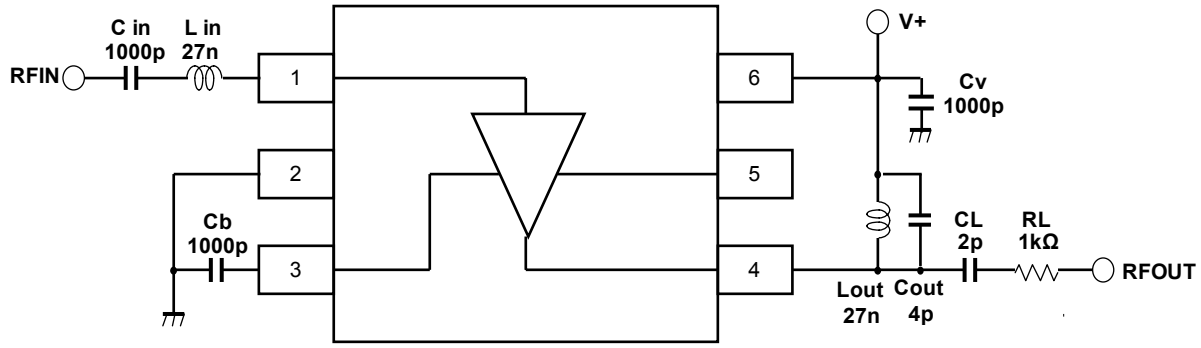
Prl = 20log ((RL + Zin) / RL)

Prl = 20 log (1050 / 50)

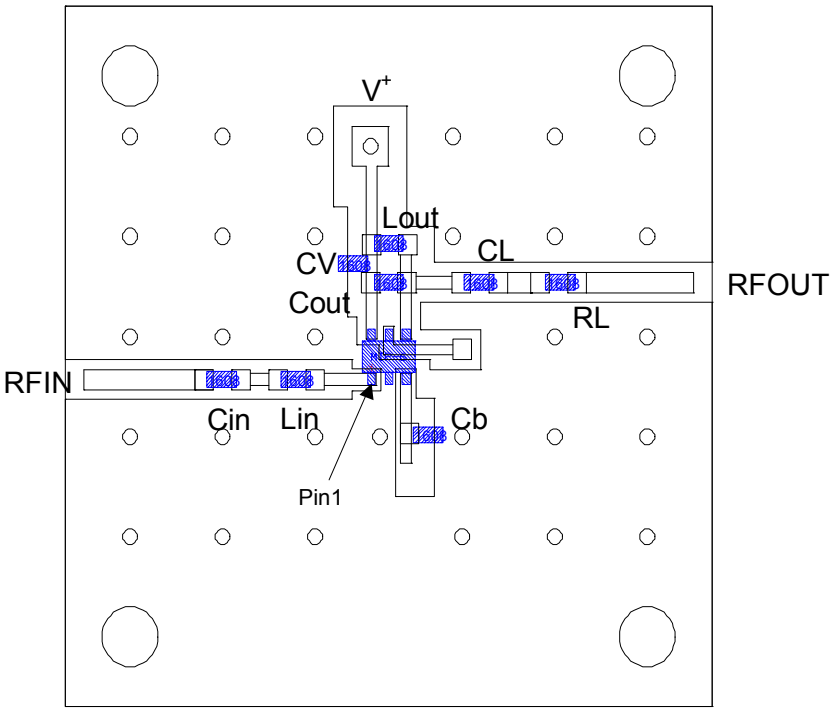
■ EVALUATION PC BOARD

The evaluation board is useful for your design and to have more understanding of the usage and performance of this device. This circuit is the same as TEST CIRCUIT. Note that this board is not prepared to show the recommendation of pattern and parts layout.

● Circuit Diagram



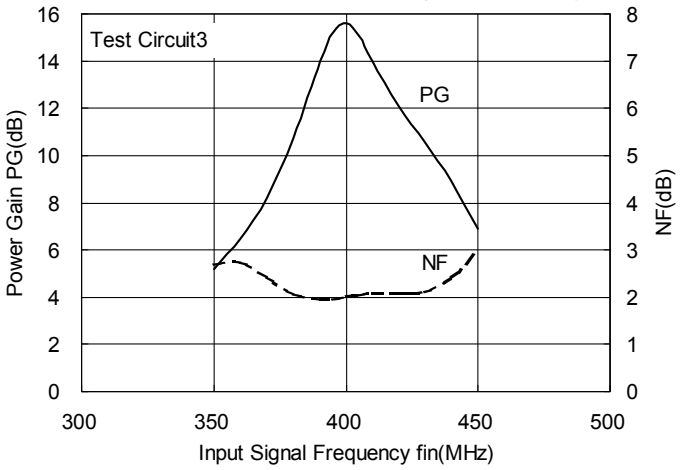
● Evaluation PC Board



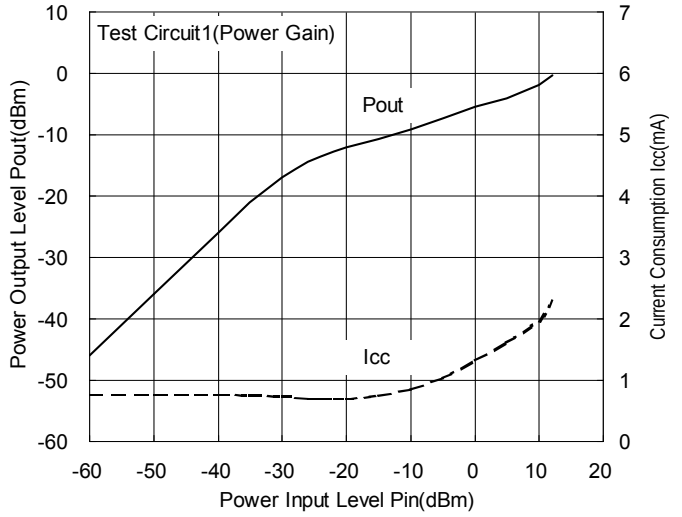
This evaluation board is designed to have the maximum value of VG at 400MHz.
By using the value of Test Circuit1, this board can be changed to have the maximum value of PG at 400MHz.
If NF is not so good, Pin 5 may have a noisy signal. In such cases, it may be effective to connect a capacitor between Pin 5 and ground. However, if the ground has a large noisy signal, NF may become worse.

■ TYPICAL CHARACTERISTICS (Ta=25°C, V^+=2.0V, unless otherwise noted)

Power Gain/NF versus Input Signal Frequency



Pout/Icc versus Pin



Pout / Icc versus Pin