

HIGH-VOLTAGE MONOLITHIC IC

ECN30601

<<Description>>

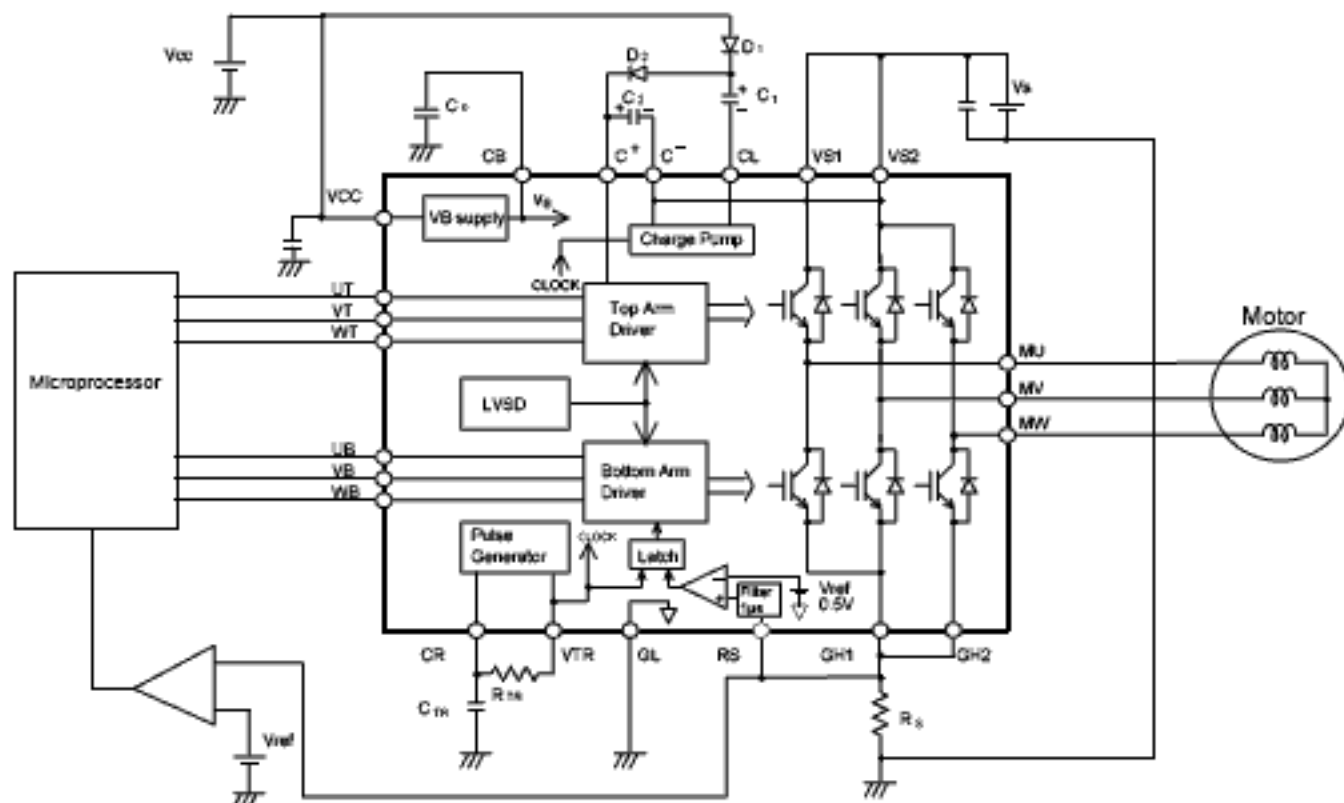
- *Rated 500V/1.5A.
- *Best for variable speed control of three-phase brush-less DC and induction motor at AC 200 to 230V.
- *High efficiency controlling with high voltage PWM operation is realized to energy saving.
- *Latch-up free monolithic IC realized by unique dielectric isolation technology.
- *IGBT (Insulated Gate Bipolar Transistor) applied as 3-phase bridge output and free wheeling diodes integrated.
- *Circuits for over current and under voltage detection integrated.
- *Easy designing of motor-integrated solution with single chip IC.
- *Drive by high and low voltage power supply one for each.
- *Terminal layout compatible with ECN3064.

<<Functions and Features>>

- *Circuits for over current and VCC under voltage detection integrated.
- *Power supplied for upper arm supplied by integrated charge pump circuit
- *Constructs three-phase bridge output with six IGBTs and Free wheeling diodes.
- *Six IGBTs can operate in 20kHz chopping frequency.
- *PWM control possible with six inputs' microprocessor control.
- *Six logic inputs are compatible with 5V CMOS or LSTTL outputs.

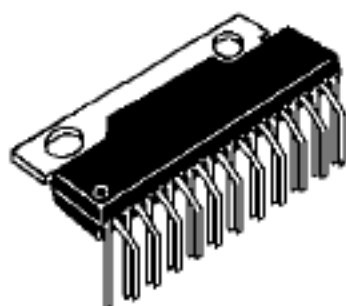
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<<Block Diagram>>
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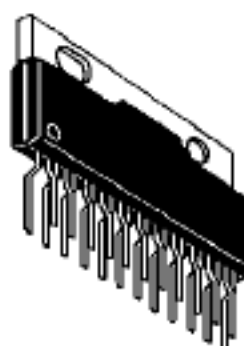


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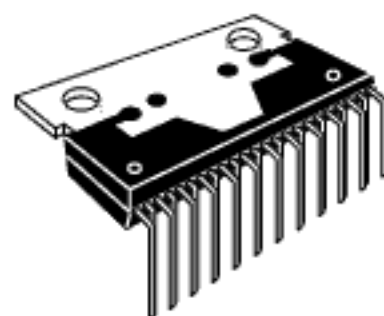
<<Part names and Packages>>



ECN30601SP
(Package Type:SP-23TA)



ECN30801SPV
(Package Type:SP-23TB)



ECN30601SPR
(Package Type:SP-23TR)

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1. Maximum allowable ratings

Ta = 25 °C

No.	Items	Symbols	Terminals	Ratings	Unit	Condition
1	Output Device Breakdown Voltage	VSM	VS1,VS2 MU,MV,MW	500	V	
2	Supply voltage	VCC	VCC	18	V	
3	Input voltage	VIN	VSP,RS HU,HV,HW	-0.5~VB+0.5	V	
4	Output current	Pulse	MU,MV,MW	1.5	A	Note 1
5		DC		0.7		
6	VB supply current	IBMAX	CB	50	mA	
7	Operating junction temperature	Tjop	-	-20~+135	°C	Note 2
8	Storage temperature	Tstg	-	-40~+150	°C	

Note Determine the derating degree for absolute maximum ratings.

Please refer to "High-Voltage Monolithic ICs " for other precautions.

Note 1 Output device can cut OFF under this value in Tj = 25 °C.

Note 2 Thermal resistance

1) Between junction to IC case : Rj-c = 4 °C/W

2) Between junction to air : Rj-a = 40 °C/W

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2. Electrical characteristics

Suffix (T ; Top arm, B ; Bottom arm)

Ta = 25 °C

No.	Items	Symbols	Terminals	MIN	TYP	MAX	Unit	Conditions
1	Supply Voltage	VSop	VS1,VS2	20	325	450	V	
2		VCCop	VCC	13.5	15	16.5	V	
3	Standby Current	ISH	VS1,VS2	-	0.5	1.5	mA	UT,VT,WT,UB,VB,WB=0V VS=325V
4		ICC	VCC	-	10	20	mA	UT,VT,WT,UB,VB,WB=0V VCC=15V,IB=0A
5	IGBT Forward Voltage	VONT	MU,MV,MW	-	2.2	3.0	V	I=0.35A,VCC=15V
6	Drop	VONB		-	2.2	3.0	V	I=0.35A,VCC=15V
7	Output Delay Time	TdONT		0.5	1.0	2.5	μs	VS=325V,VCC=15V I=0.35A Resistive Load
8		TdONB		1.0	2.0	3.0	μs	
9		TdOFFT		1.0	2.0	3.0	μs	
10		TdOFFB		1.0	2.0	3.0	μs	
11	Free wheel Diode	VFDT		-	2.2	2.8	V	I=0.35A
12	Forward Voltage Drop	VFDB		-	2.4	3.0	V	
13	Reference voltage	Vref	RS	0.45	0.5	0.55	V	VCC=15V
14	UT,VT, WT	Voltage	UT,VT,WT	3.5	-	-	V	VCC=15V
15		VIL		-	-	1.5	V	
16	UB,VB, WB	Current	UB,VB,WB	-10	-	-	μA	Input=0V VCC=15V Pull down resistance Note 1
17		IIH		-	-	100	μA	
18	VB supply Output	Voltage	CB	6.8	7.5	8.2	V	VCC=15V,IB=0A
19		Current		-	-	25	mA	VCC=15V
20	LVSD	Detect voltage	VCC, MU,MV, MW	10.0	11.5	12.9	V	Note 2
21		Recover Voltage	MU,MV, MW	10.1	12.0	13.0	V	
22		Hysteresis		0.1	0.5	0.9	V	
23	RS terminal input current	IILRS	RS	-100	-	-	μA	VCC=15V, RS=0V, UT,VT,WT,UB,VB,WB=0V

Note 1 Pull down resistance are typically 200 kΩ.

Note 2 LVSD (Low voltage shut down) : Detect and shut down at lower VCC.

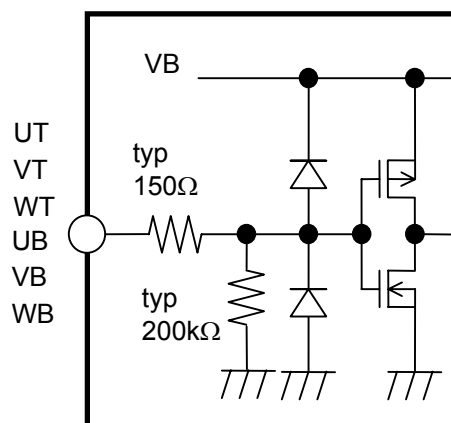


Fig1. Equivalent circuit of UT,VT,WT,UB,VB,WB terminals

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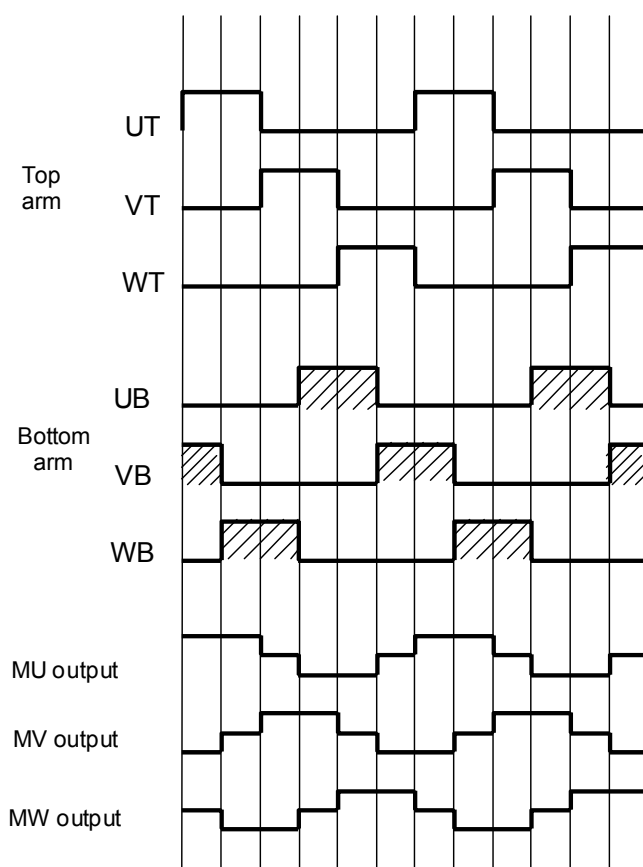
3.Functions

3.1 Truth table

Terminals	Input	Output
UT, VT, WT, UB, VB, WB	L	OFF
	H	ON
UT, UB	UT & UB = H	OFF
VT, VB	VT & VB = H	OFF
WT, WB	WT & WB = H	OFF

3.2 Timing chart

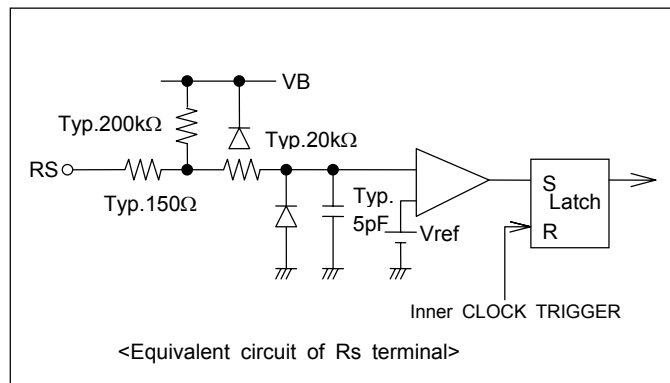
Example of inverter controlled 120° commutation mode.



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3.3 Over current limiting operation

This IC detects over current using external resistance R_S . When R_S input voltage exceeds inner reference voltage V_{ref} (0.5V typical), this IC turns off all the bottom output IGBTs. After over current detection, reset operation is done at each inner clock signal period. In case of not using this function, please connect R_S terminal to GL terminal less than 100Ω impedance.



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4. Standard application

4.1 External components

Components	Standard value	Usage	Remarks
Co	0.22 $\mu\text{F} \pm 20\%$	For inner power supply(VB)	Stress voltage is VB(=8.2V)
C1,C2	1.0 $\mu\text{F} \pm 20\%$	For charge pump	Stress voltage is VCC
D1,D2	Hitachi DFG1C6 (Glass mold type), DFM1F6 (Resin mold type) or considerable parts	For charge pump	600V, 1A trr $\leq 100\text{ns}$
Rs	Note 1	For current limit	
CTR	1800 pF $\pm 5\%$	For clock frequency	Stress voltage is VB(=8.2V) Note2
RTR	22 k $\Omega \pm 5\%$	For clock frequency	Stress voltage is VB(=8.2V) Note2

Note 1 Over current detection is determined approximately by next equation.

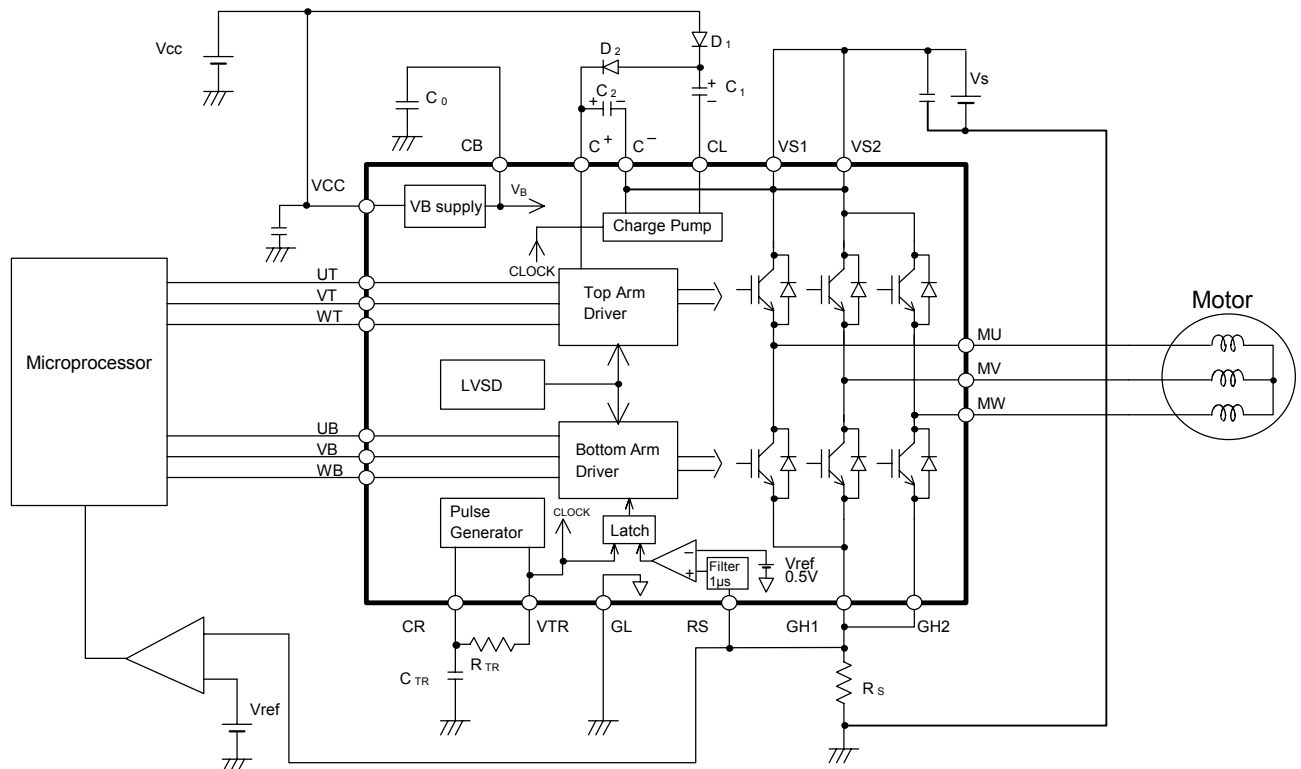
$$I_O = V_{\text{ref}} / R_s \quad (\text{A})$$

I_O should be determined less than IDC of maximum allowable ratings.

To determine sense resistance R_s , refer above comment and appendix 1.2 and 1.3 on pp.12-13 of this document.

Note 2. Clock frequency is determined by next equation.

$$f_{\text{clock}} \approx 0.494 / (CTR \times RTR) \quad (\text{Hz})$$



note; Inside of bold line shows ECN30601

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4.2 Input terminals (UB, VB, WB, UT, VT, WT)

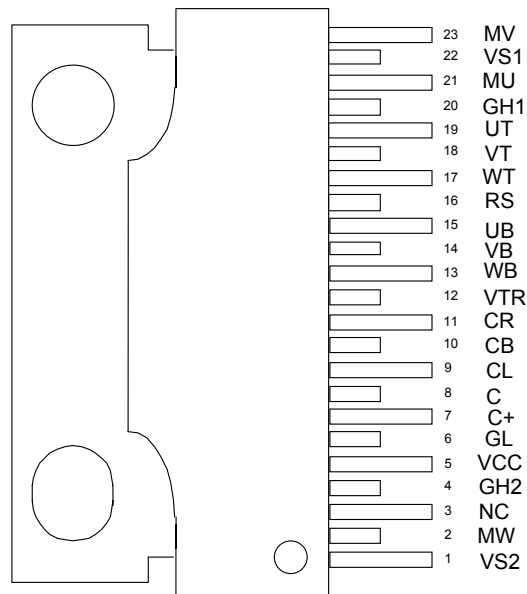
Input terminals have a possibility to get an influence from some noise because of their high Impedance. In this case, add resistance and/or capacitance.

Resistance : Add pull down resistance to GL terminals, $5.6 \text{ k}\Omega \pm 5\%$

Capacitance : Add ceramic capacitance near the terminals. $500 \text{ pF} \pm 20\%$

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5. Terminal layout



(Marking side)

6. Terminal definition

Terminal No.	Symbol	Definition	Remarks
1	VS2	Power supply for upper IGBT of U and V phase	Note1,Note2
2	MW	W phase output	Note1
3	NC	Non connected terminal	Note4
4	GH2	W phase emitter of IGBT and anode of FWD. Connect Rs.	Note3
5	VCC	Logic power supply	
6	GL	Logic ground	
7	C+	For Charge pump circuit, power supply for top arm drive circuit	Note1
8	C-	For Charge pump circuit	Note1, Note2
9	CL	For Charge pump circuit	Note1
10	CB	Inner VB power supply	
11	CR	Connect resistance and capacitance for clock frequency	
12	VTR	Connect resistance for clock frequency	
13	WB	Input control signal for W phase bottom arm	
14	VB	Input control signal for V phase bottom arm	
15	UB	Input control signal for U phase bottom arm	
16	RS	RS voltage detect for over current limitation	
17	WT	Input for W phase top arm control signal	
18	VT	Input for V phase top arm control signal	
19	UT	Input for U phase top arm control signal	
20	GH1	U and V phase emitter of IGBT and anode of FWD. Connect Rs.	Note3
21	MU	U phase output	Note1
22	VS1	Power supply for upper IGBT of U phase	Note1,Note2
23	MV	V phase output	Note1

Note1 High voltage terminal.

Note2 VS1, VS2 and C- terminals are connected in IC, but should be connect in external circuit between VS1 and VS2.

Note3 GH1 and GH2 are not connected in IC, so should be connect in external circuit between GH1 and GH2

Note4 not connected to inner chip.

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7. Quality Assurance

7.1 Appearance and dimension

ANSI Z1.4-1993 General inspection levels II AQL 1.0%

7.2 Electrical characteristics

ANSI Z1.4-1993 General inspection levels II AQL 0.65%

8. Does and Don'ts

8.1 Tightening torque at 0.39 to 0.78 N-m should be applied for device to attach to heat sink.

8.2 Tab should not be soldered.

8.3 How to protect semiconductor from electrical static discharge (ESD).

- a) Material of container or any device to carry semiconductor devices should be free from ESD which may be caused by vibration while transportation. To use electric-conductive container or aluminum sheet is recommended as an effective countermeasure.
- b) Those what touch semiconductor devices such as work platform, machine and measuring and test equipment should be grounded.
- c) Workers should be grounded connecting with high impedance around 100kΩ to 1MΩ while dealing with semiconductor to avoid electric static discharge which destroying IC.
- d) Friction with other materials such as a high polymer should not be caused.
- e) Attention is needed so that electric potential will be kept on the same level by short circuit terminals when IC is mounted and carried on PC board in addition to that vibration or friction might not occur.
- f) Air conditioning is needed so that humidity should not drop.
- g) To prevent IC broken by ESD, it should be taken the precautions.

8.4 Applying molding or resin coating is recommended for below mentioned pin-to-pin insulation;

1-2, 2-4, 6-7, 8-9, 9-10, 20-21, 21-22, 22-23

8.5 Protective function against short circuit (ex. load short, line-to-ground short or top/bottom arm short) is not built in this IC. External protection needs to prevent IC breakdown.

8.6 Hitachi high voltage IC is not under screening or process where extremely high reliability is assured. In cases where extremely high reliability is required (such as nuclear power control, aerospace and aviation, traffic equipment, life-support-related medical equipment, fuel control equipment and various kinds of safety equipment) safety should be ensured by customers' own responsibility. See to it that IC's breakdown should not damage one's property or human life. Users should follow the following ;

- a) Enough deratings degree should be taken in order to minimize failure ratio against maximum ratings considering temperature and operating stress.
- b) Redundancy design should be applied depending on IC's importance in a system so that application's performance will achieve even in a case of IC's breakdown.
- c) Reliability design should be implemented on the system, that is fail-safe design to protect property and human life, and foolproof design for users are not very familiar with the system operation.

Refer to "Precautions for Use of High-Voltage Monolithic ICs" for more details.

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◆ Supplementary and Reference Data

Refer to the below data before handling Hitachi semiconductor device.
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1. Area of Safety Operation (ASO) and derating

1.1 ASO

Use under ASO region of figure2 of voltage and current at output terminals of IC, while switching.

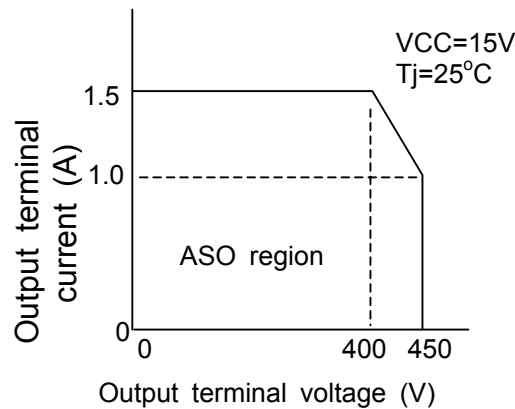
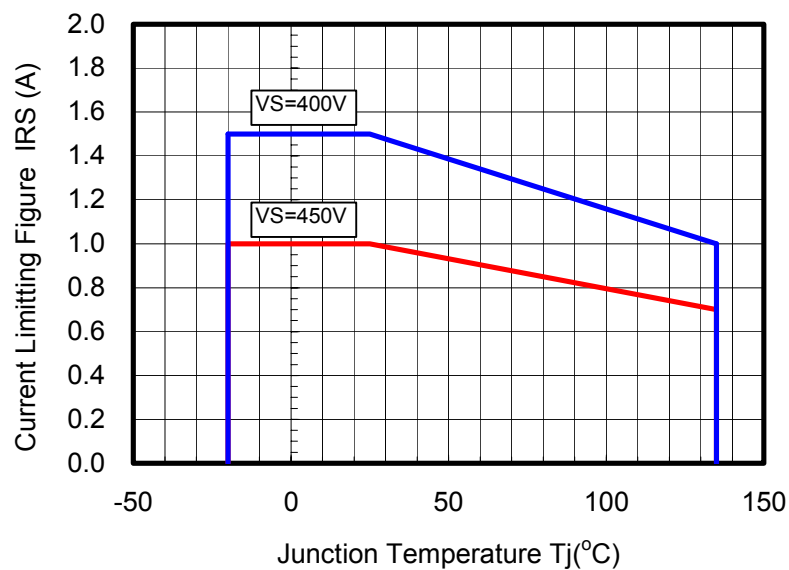


Fig2. ASO

1.2 Derating design about temperature

ASO has dependence on temperature. Determine RS value according derating curve of figure3, including maximum value of reference voltage(Vref) and resistance's tolerance.



< Fig.3 Derating Curve >

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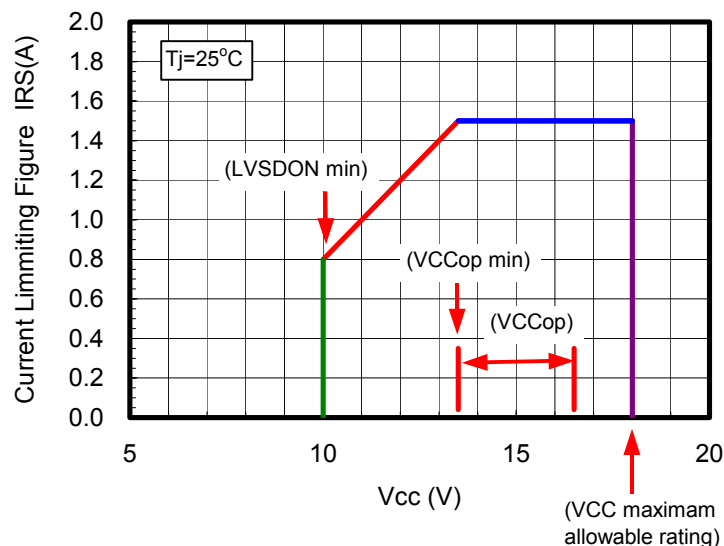
1.3 Power supply sequence and derating for VCC

Power supply sequence of power on should be VCC on, VS on and control signals (UB,VB,WB,UT,VT,WT) on. For power off, it should be controlled signal off, VS off and VCC off. If the control signals UB, VB and WB are all low, the power supply sequence is free.

In case of above sequence can not control such as suddenly stopped the power supply, It should be taken the following.

When IGBTs operated with lower gate voltage, it will be occurred the thermal failure because IGBT saturation voltage increases rapidly, especially VCC voltage period is VCCop minimum value to LVSDON minimum value, that is 13.5V to 10V.

To avoid this mode, refer derating curve of VCC in figure 4.



< Fig4. Derating Curve of terminal current to Vcc >

1.4 Derating for maximum allowable ratings

Derating design standards is below.

- Temperature ; Junction temperature must be keep under 110 °C.
- Voltage ; VS power supply voltage must be keep under 450V.

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