FAIRCHILD SEMICONDUCTOR®

February 2005

# FDS8962C

## Dual N & P-Channel PowerTrench® MOSFET

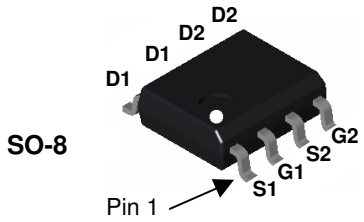
### General Description

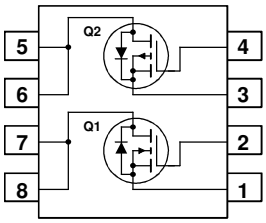
These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state ressitance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

### Features

- **Q1**: N-Channel
  7.0A, 30V $R_{DS(on)}$ = 0.030Ω @ $V_{GS}$ = 10V
  $R_{DS(on)}$ = 0.044Ω @ $V_{GS}$ = 4.5V
- **Q2**: P-Channel
  -5A, -30V $R_{DS(on)}$ = 0.052Ω @ $V_{GS}$ = -10V
  $R_{DS(on)}$ = 0.080Ω @ $V_{GS}$ = -4.5V
- Fast switching speed
- High power and handling capability in a widely used surface mount package




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Q1 | Q2 | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | 30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | ±20 | V |
| $I_D$ | Drain Current - Continuous | (Note 1a) | 7 | -5 | A |
| | - Pulsed | | 20 | -20 | |
| $P_D$ | Power Dissipation for Dual Operation | | 2 | | W |
| | Power Dissipation for Single Operation | (Note 1a) | 1.6 | | |
| | | (Note 1b) | 1 | | |
| | | (Note 1c) | 0.9 | | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | | °C |

## Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 78 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 40 | °C/W |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| FDS8962C | FDS8962C | 13" | 12mm | 2500 units |

## Electrical Characteristics

$T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA<br>$V_{GS}$ = 0 V, $I_D$ = -250 µA | Q1<br>Q2 | 30<br>-30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C<br>$I_D$ = -250 µA, Referenced to 25°C | Q1<br>Q2 | | 25<br>-23 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = -24 V, $V_{GS}$ = 0 V | Q1<br>Q2 | | | 1<br>-1 | µA |
| $I_{GSSF}$ | Gate-Body Leakage, Forward | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | All | | | 100 | nA |
| $I_{GSSR}$ | Gate-Body Leakage, Reverse | $V_{GS}$ = -20 V, $V_{DS}$ = 0 V | All | | | -100 | nA |
| **On Characteristics** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA<br>$V_{DS}$ = $V_{GS}$, $I_D$ = -250 µA | Q1<br>Q2 | 1<br>-1 | 1.9<br>-1.7 | 3<br>-3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = 250 µA, Referenced to 25°C<br>$I_D$ = -250 µA, Referenced to 25°C | Q1<br>Q2 | | -4.5<br>4.5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = 10 V, $I_D$ = 7 A<br>$V_{GS}$ = 10 V, $I_D$ = 7 A, $T_J$ = 125°C<br>$V_{GS}$ = 4.5 V, $I_D$ = 6 A | Q1 | | 21<br>29<br>26 | 30<br>46<br>44 | mΩ |
| | | $V_{GS}$ = -10 V, $I_D$ = -5 A<br>$V_{GS}$ = -10 V, $I_D$ = -5 A, $T_J$ = 125°C<br>$V_{GS}$ = -4.5 V, $I_D$ = -4 A | Q2 | | 42<br>57<br>65 | 52<br>78<br>80 | |
| $I_{D(on)}$ | On-State Drain Current | $V_{GS}$ = 10 V, $V_{DS}$ = 5 V<br>$V_{GS}$ = -10 V, $V_{DS}$ = -5 V | Q1<br>Q2 | 20<br>-20 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 7 A<br>$V_{DS}$ = -5 V, $I_D$ =-5 A | Q1<br>Q2 | | 25<br>10 | | S |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ | Input Capacitance | Q1<br>$V_{DS}$ = 15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | Q1<br>Q2 | | 575<br>528 | | pF |
| $C_{oss}$ | Output Capacitance | Q2<br>$V_{DS}$ = -15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | Q1<br>Q2 | | 145<br>132 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | | 65<br>70 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15 mV, f = 1.0 MHz | Q1<br>Q2 | | 2.1<br>6.0 | | Ω |

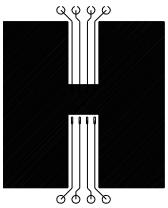
## Electrical Characteristics (continued)

$T_A$ = 25°C unless otherwise noted

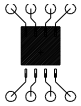
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Switching Characteristics** (Note 2) | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | Q1<br>$V_{DD}$ = 15 V, $I_D$ = 1 A,<br>$V_{GS}$ = 10V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 8<br>7 | 16<br>14 | ns |
| $t_r$ | Turn-On Rise Time | | Q1<br>Q2 | | 5<br>13 | 10<br>24 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | Q2<br>$V_{DD}$ = -15 V, $I_D$ = -1 A,<br>$V_{GS}$ = -10V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 23<br>14 | 37<br>25 | ns |
| $t_f$ | Turn-Off Fall Time | | Q1<br>Q2 | | 3<br>9 | 6<br>17 | ns |
| $Q_g$ | Total Gate Charge | Q1<br>$V_{DS}$ = 15 V, $I_D$ = 7 A, $V_{GS}$ = 10 V | Q1<br>Q2 | | 10.7<br>9.6 | 26<br>13 | nC |
| $Q_{gs}$ | Gate-Source Charge | Q2 | Q1<br>Q2 | | 1.7<br>2.2 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | $V_{DS}$ = -15 V, $I_D$ = -5 A,$V_{GS}$ = -10 V | Q1<br>Q2 | | 2.1<br>1.7 | | nC |
| **Drain–Source Diode Characteristics and Maximum Ratings** | | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | Q1<br>Q2 | | | 1.3<br>-1.3 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = -1.3 A (Note 2) | Q1<br>Q2 | | 0.75<br>-0.88 | 1.2<br>-1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | Q1<br>$I_F$ = 7 A, $d_{iF}/d_t$ = 100 A/µs | Q1<br>Q2 | | 19<br>19 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | Q2<br>$I_F$ = -5 A, $d_{iF}/d_t$ = 100 A/µs | Q1<br>Q2 | | 9<br>6 | | nC |

**Notes:**

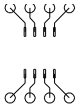
**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°/W when mounted on a 0.5 $in^2$ pad of 2 oz copper



b) 125°/W when mounted on a .02 $in^2$ pad of 2 oz copper



c) 135°/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics: Q1 (N-Channel)

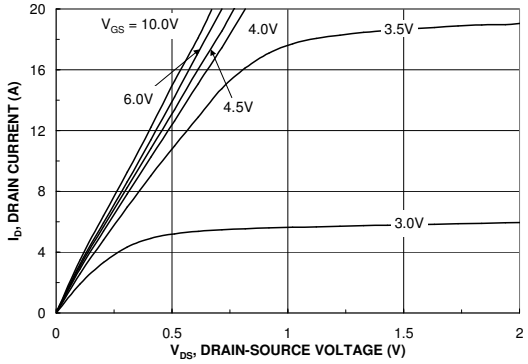



**Figure 1. On-Region Characteristics.**

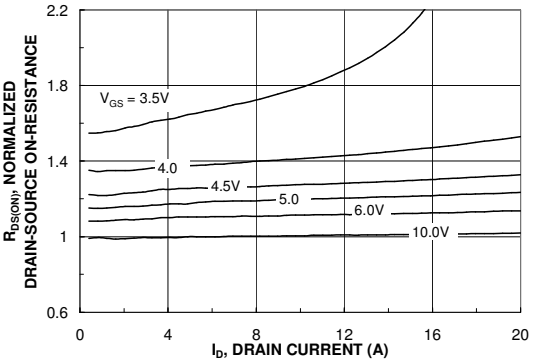



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

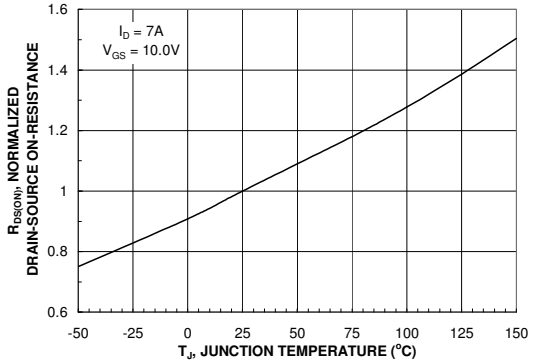



**Figure 3. On-Resistance Variation with Temperature.**

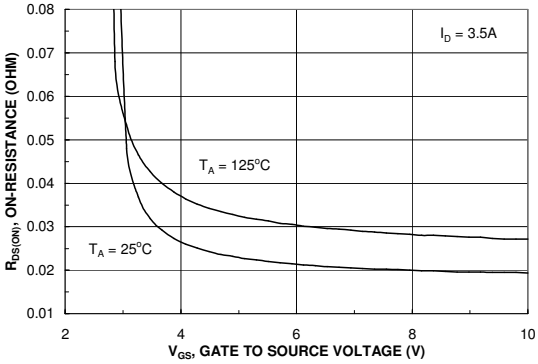



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

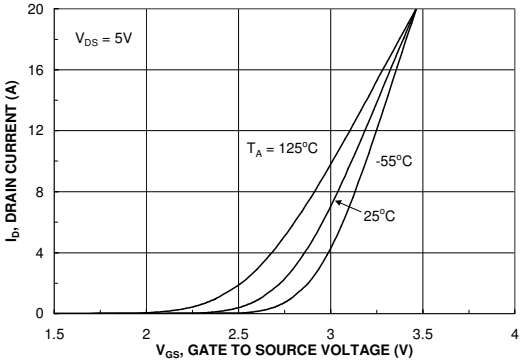



**Figure 5. Transfer Characteristics.**

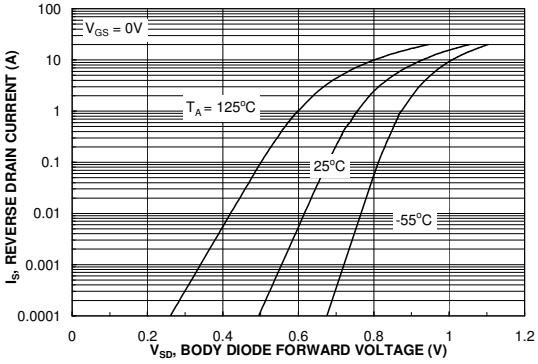



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics: Q1 (N-Channel)

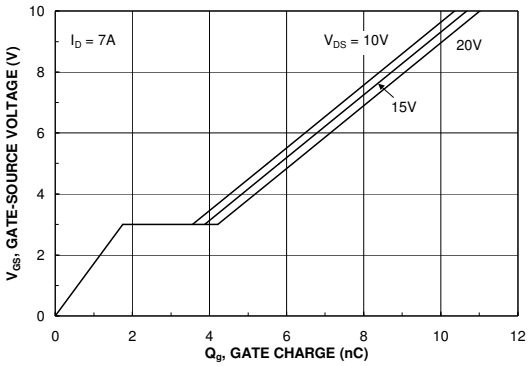



**Figure 7. Gate Charge Characteristics.**

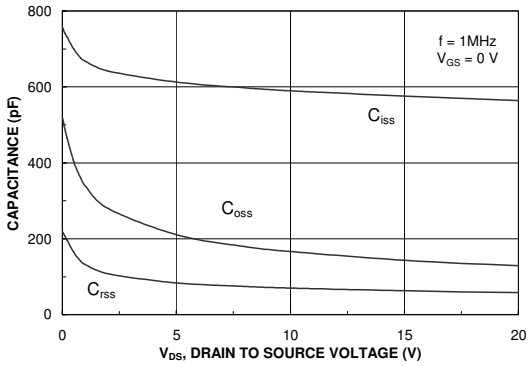



**Figure 8. Capacitance Characteristics.**

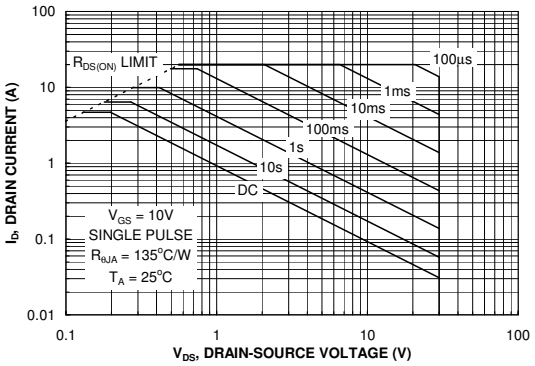



**Figure 9. Maximum Safe Operating Area.**

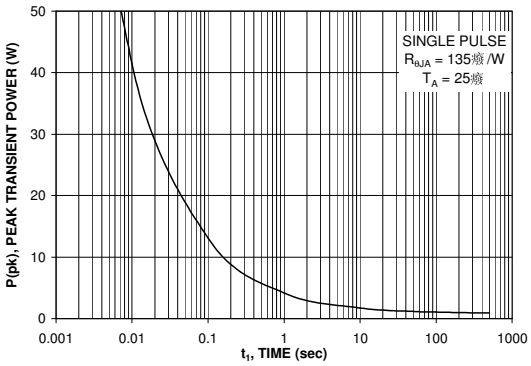



**Figure 10. Single Pulse Maximum Power Dissipation.**

## Typical Characteristics: Q2 (P-Channel)

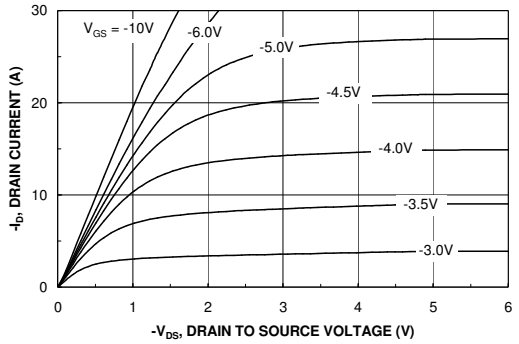



**Figure 11. On-Region Characteristics.**

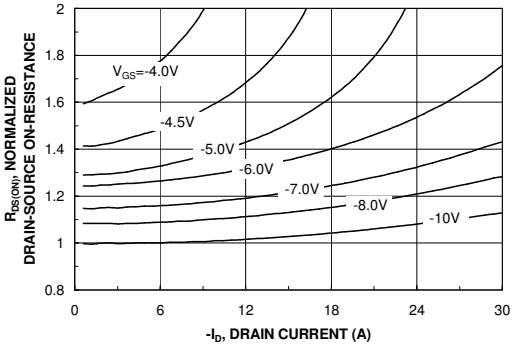



**Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.**

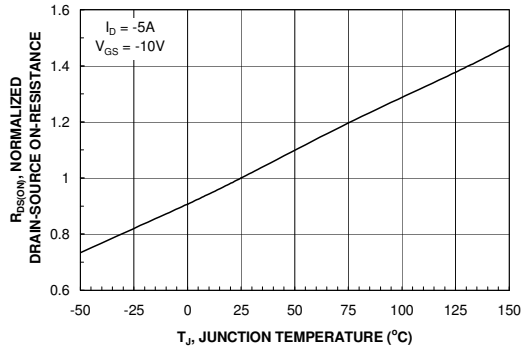



**Figure 13. On-Resistance Variation with Temperature.**

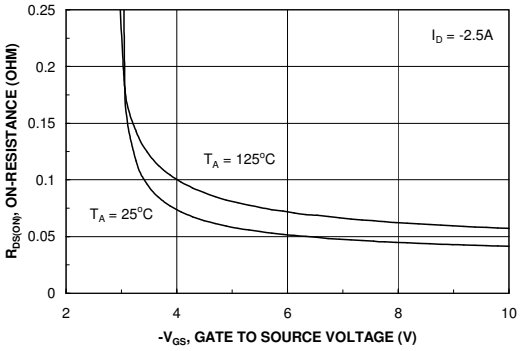



**Figure 14. On-Resistance Variation with Gate-to-Source Voltage.**

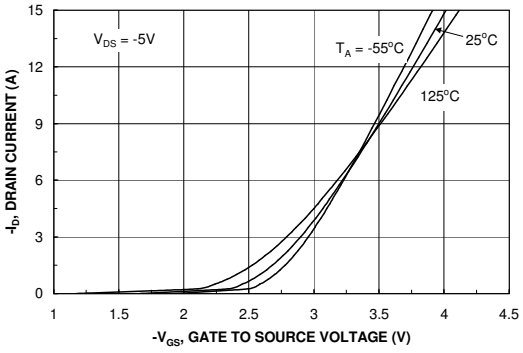



**Figure 15. Transfer Characteristics.**

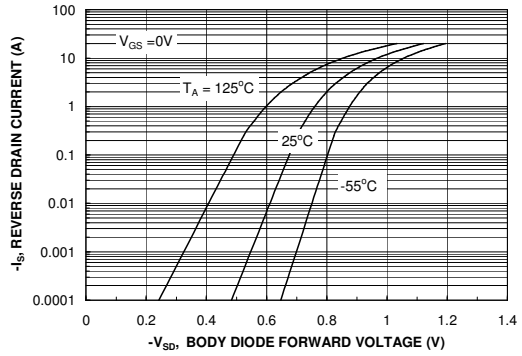



**Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics: Q2 (P-Channel)

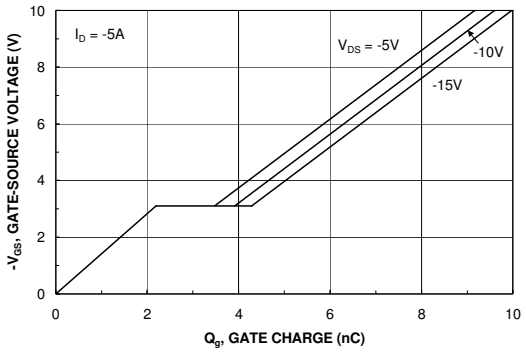



**Figure 17. Gate Charge Characteristics.**

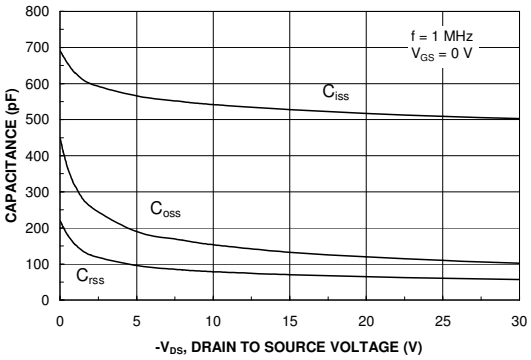



**Figure 18. Capacitance Characteristics.**

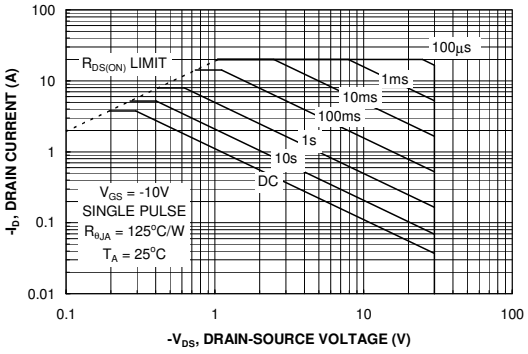



**Figure 19. Maximum Safe Operating Area.**

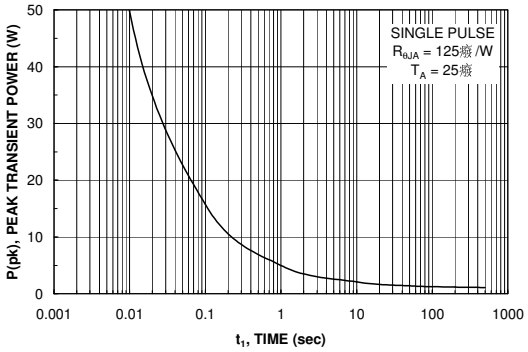



**Figure 20. Single Pulse Maximum Power Dissipation.**

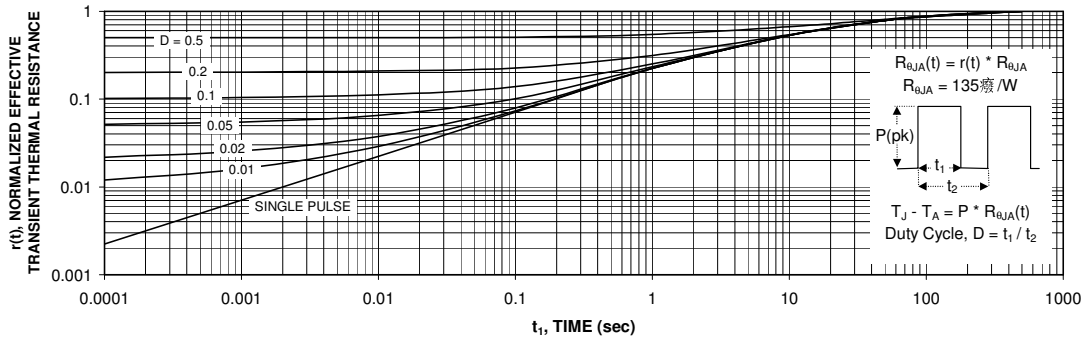



**Figure 21. Transient Thermal Response Curve.**

**Thermal characterization performed using the conditions described in Note 1c.**
**Transient thermal response will change depending on the circuit board design.**

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