

# MM54HCT190/MM74HCT190 Synchronous Decade Up/Down Counters with Mode Control. MM54HCT191/MM74HCT191 Synchronous Binary Up/Down Counters with Mode Control

## General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. These circuits are synchronous, reversible, up/down counters. The MM54HCT191/MM74HCT191 are 4-bit binary counters and the MM54HCT190/MM74HCT190 are BCD counters.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as divide by N dividers by simply modifying the count length with the preset inputs.

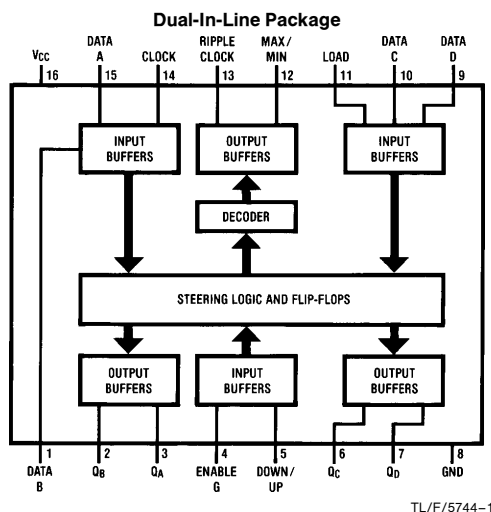
Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices can be used to reduce power consumption in existing designs.

## Features

- Level changes on Enable or Down/Up can be made regardless of the level of the clock.
- Low quiescent supply current: 80  $\mu$ A maximum (74HCT Series)
- Low input current: 1  $\mu$ A maximum
- TTL compatible inputs

## Connection Diagram



## Truth Table

Load	Enable G	Down/Up	Clock	Function
H	L	L	$\uparrow$	Count Up
H	L	H	$\uparrow$	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Order Number MM54HCT190/191  
or MM74HCT190/191

**Absolute Maximum Ratings** (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	−0.5V to + 7.0V
DC Input Voltage ( $V_{IN}$ )	−1.5V to $V_{CC}$ + 1.5V
DC Output Voltage ( $V_{OUT}$ )	−0.5V to $V_{CC}$ + 0.5V
Clamp Diode Current ( $I_{IK}$ , $I_{OK}$ )	± 20 mA
DC Output Current, per Pin ( $I_{OUT}$ )	± 25 mA
DC $V_{CC}$ or GND Current, per Pin ( $I_{CC}$ )	± 50 mA
Storage Temperature Range ( $T_{STG}$ )	−65°C to + 150°C
Power Dissipation ( $P_D$ )	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

**Operating Conditions**

	Min	Max	Units
Supply Voltage ( $V_{CC}$ )	4.5	5.5	V
DC Input or Output Voltage ( $V_{IN}$ , $V_{OUT}$ )	0	$V_{CC}$	V
Operating Temp. Range ( $T_A$ )			
MM74HCT	−40	+ 85	°C
MM54HCT	−55	+ 125	°C
Input Rise or Fall Times ( $t_r$ , $t_f$ )		500	ns

**DC Electrical Characteristics**  $V_{CC} = 5V \pm 10\%$  unless otherwise specified

Symbol	Parameter	Conditions	T <sub>A</sub> = 25°C		74HCT	54HCT	Units
					T <sub>A</sub> = −40°C to 85°C	T <sub>A</sub> = −55°C to 125°C	
			Typ	Guaranteed Limits			
V <sub>IH</sub>	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V <sub>IL</sub>	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V <sub>OH</sub>	Minimum High Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>OUT</sub>   = 20 μA	V <sub>CC</sub>	V <sub>CC</sub> −0.1	V <sub>CC</sub> −0.1		
		I <sub>OUT</sub>   = 4.0 mA, V <sub>CC</sub> = 4.5V	4.2	3.98	3.84	3.7	
		I <sub>OUT</sub>   = 4.8 mA, V <sub>CC</sub> = 5.5V	5.2	4.98	4.84	4.7	V
V <sub>OL</sub>	Maximum Low Level Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>					
		I <sub>OUT</sub>   = 20 μA	0	0.1	0.1	0.1	V
		I <sub>OUT</sub>   = 4.0 mA, V <sub>CC</sub> = 4.5V	0.2	0.26	0.33	0.4	V
		I <sub>OUT</sub>   = 4.8 mA, V <sub>CC</sub> = 5.5V	0.2	0.26	0.33	0.4	V
I <sub>IN</sub>	Maximum Input Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, V <sub>IH</sub> or V <sub>IL</sub>		± 0.1	± 1.0	± 1.0	μA
I <sub>CC</sub>	Maximum Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0 μA		8	80	160	μA
		V <sub>IN</sub> = 2.4V or 0.5V (Note 4)		1.0	1.2	1.3	mA

**Note 1:** Absolute Maximum Ratings are those values beyond which damage to the device may occur.

**Note 2:** Unless otherwise specified all voltages are referenced to ground.

**Note 3:** Power dissipation temperature derating—plastic “N” package: −12 mW/°C from 65°C to 85°C; ceramic “J” package: −12 mW/°C from 100°C to 125°C.

**Note 4:** Measured per pin, all other inputs held at  $V_{CC}$  or GND.

# **AC Electrical Characteristics** $T_A = 25^{\circ}\text{C}$ , $V_{CC} = 5.0\text{V}$ , $t_r = t_f = 6\text{ ns}$ , $C_L = 15\text{ pF}$ unless otherwise specified

Symbol	Parameter	From Input	To Output	Conditions	Typ	Guaranteed Limits	Units
$f_{\text{MAX}}$	Maximum Clock Frequency				40		MHz
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay Time	Load	$Q_A$ , $Q_B$ $Q_C$ , $Q_D$		30		ns
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay Time	Data A, B, C, D	$Q_A$ , $Q_B$ $Q_C$ , $Q_D$		27		ns
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay Time	Clock	Ripple Clock		16		ns
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay Time	Clock	$Q_A$ , $Q_B$ $Q_C$ , $Q_D$		24		ns
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay Time	Clock	Max/Min		30		ns
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay Time	Down/Up	Ripple Clock		29		ns
$t_{\text{PLH}}$ , $t_{\text{PHL}}$	Maximum Propagation Delay Time	Down/Up	Max/Min		22		ns
$t_{\text{PHL}}$ , $t_{\text{PLH}}$	Maximum Propagation Delay Time	Enable	Ripple Clock		22		ns
$t_w$	Minimum Clock or Load Input Pulse Width				10		ns

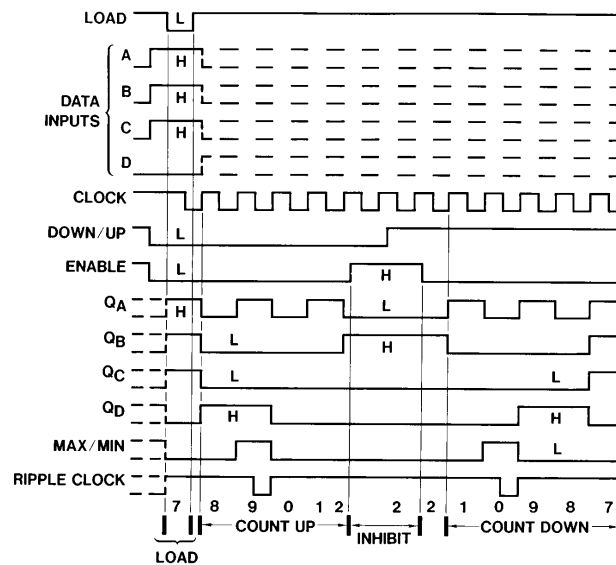
# AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$ , $C_L = 50\text{ pF}$ , $t_r = t_f = 6\text{ ns}$ unless otherwise specified

Symbol	Parameter	From Input	To Output	Conditions	T <sub>A</sub> = 25°C		74HCT T <sub>A</sub> = −40°C to 85°C	54HCT T <sub>A</sub> = −55°C to 125°C	Units
					Typ	Guaranteed Limits			
f <sub>MAX</sub>	Maximum Clock Frequency				28	20	16	13	MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay Time	Load	Q <sub>A</sub> , Q <sub>B</sub> Q <sub>C</sub> , Q <sub>D</sub>		31	44	55	66	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay Time	Data A, B, C, D	Q <sub>A</sub> , Q <sub>B</sub> Q <sub>C</sub> , Q <sub>D</sub>		30	40	50	60	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay Time	Clock	Ripple Clock		24	30	38	45	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay Time	Clock	Q <sub>A</sub> , Q <sub>B</sub> Q <sub>C</sub> , Q <sub>D</sub>		32	43	54	65	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay Time	Clock	Max/Min		45	55	69	83	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay Time	Down/Up	Ripple Clock		42	50	63	75	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay Time	Down/Up	Max/Min		30	45	56	68	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time	Enable	Ripple Clock		26	33	41	50	ns
t <sub>W</sub>	Minimum Clock Pulse Width				15	25	31	38	ns
t <sub>S</sub>	Minimum Set-Up Time	Data	Load		10	20	25	30	ns
t <sub>H</sub>	Minimum Hold Time	Load	Data		−3	5	6	8	ns
t <sub>S</sub>	Minimum Set-Up Time	Down/Up	Clock		23	30	38	45	ns
t <sub>H</sub>	Minimum Hold Time	Clock	Down/Up		−7	0	0	0	ns
t <sub>S</sub>	Minimum Set-Up Time	Enable	Clock		13	20	25	30	ns
t <sub>H</sub>	Minimum Hold Time	Clock	Enable		−5	0	0	0	ns
t <sub>THL</sub> , t <sub>TLH</sub>	Maximum Output Rise and Fall Time				10	15	19	22	ns
C <sub>IN</sub>	Maximum Input Capacitance				5				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)				35				pF

**Note 5:**  $C_{PD}$  determines the no load dynamic power consumption,  $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$ , and the no load dynamic current consumption,  $I_S = C_{PD} V_{CC} f + I_{CC}$ .

## Timing Diagrams

**'HCT190 Synchronous Decade Counters**  
Typical Load, Count, and Inhibit Sequences

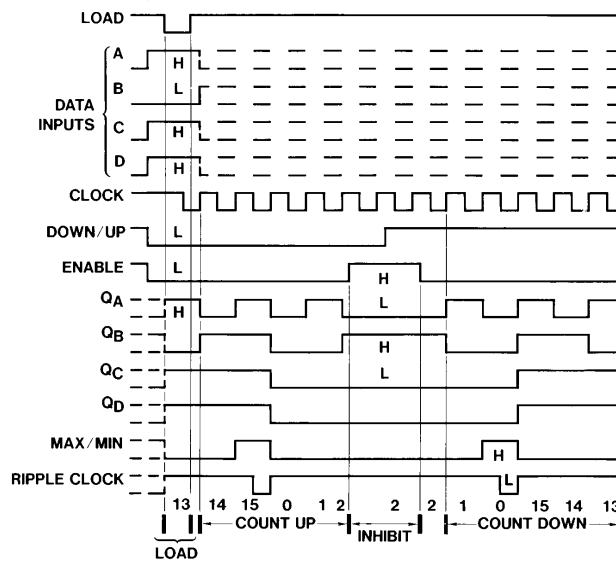


TL/F/5744-5

**Sequence:**

- (1) Load (preset) to BCD seven
- (2) Count up to eight, nine, zero, one and two
- (3) Inhibit
- (4) Count down to one, zero, nine, eight and seven

**'HCT191 Synchronous Binary Counters**  
Typical Load, Count, and Inhibit Sequence

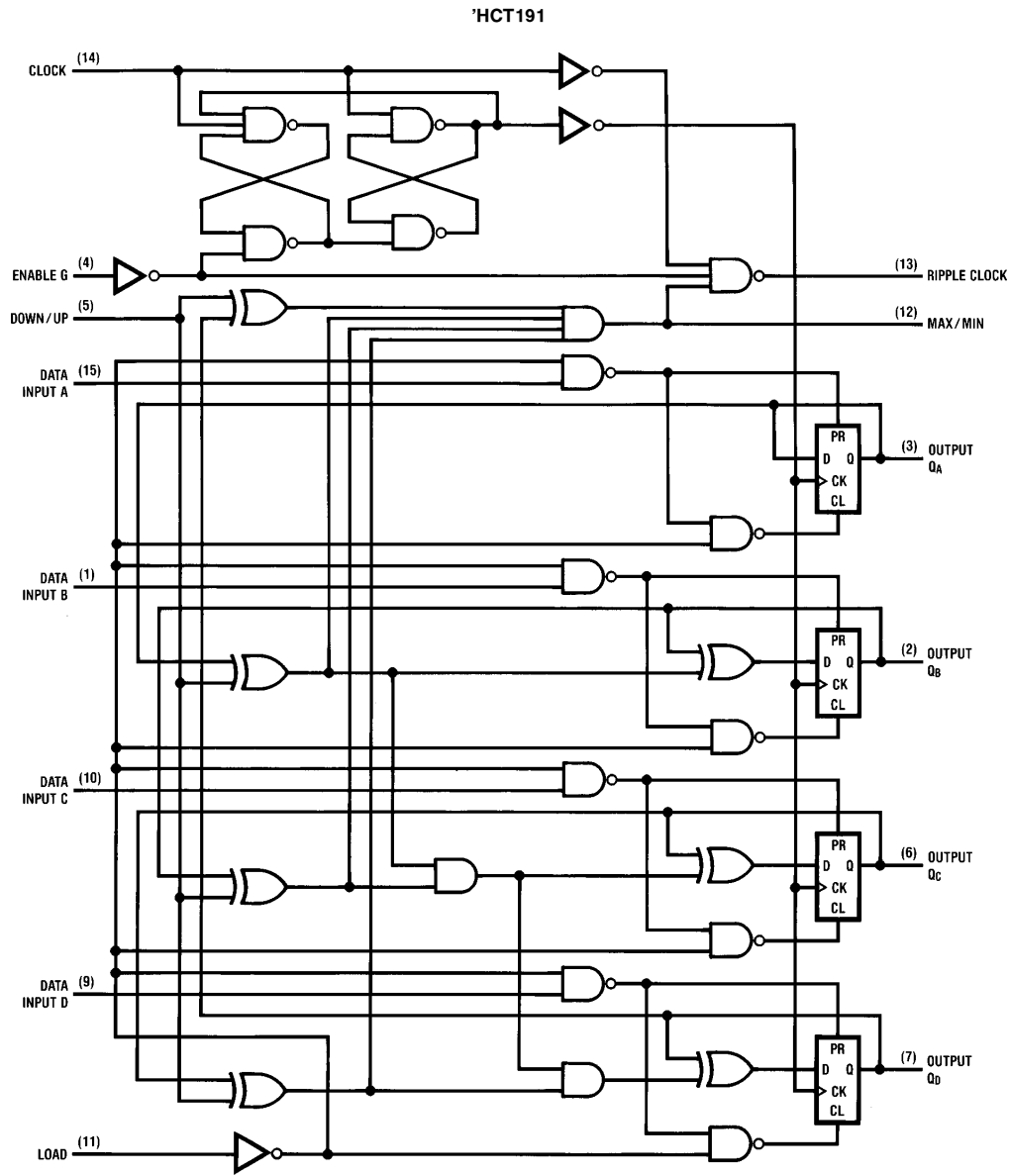


TL/F/5744-6

**Sequence:**

- (1) Load (preset) to binary thirteen
- (2) Count up to fourteen, fifteen, zero, one and two
- (3) Inhibit
- (4) Count down to one, zero, fifteen, fourteen and thirteen

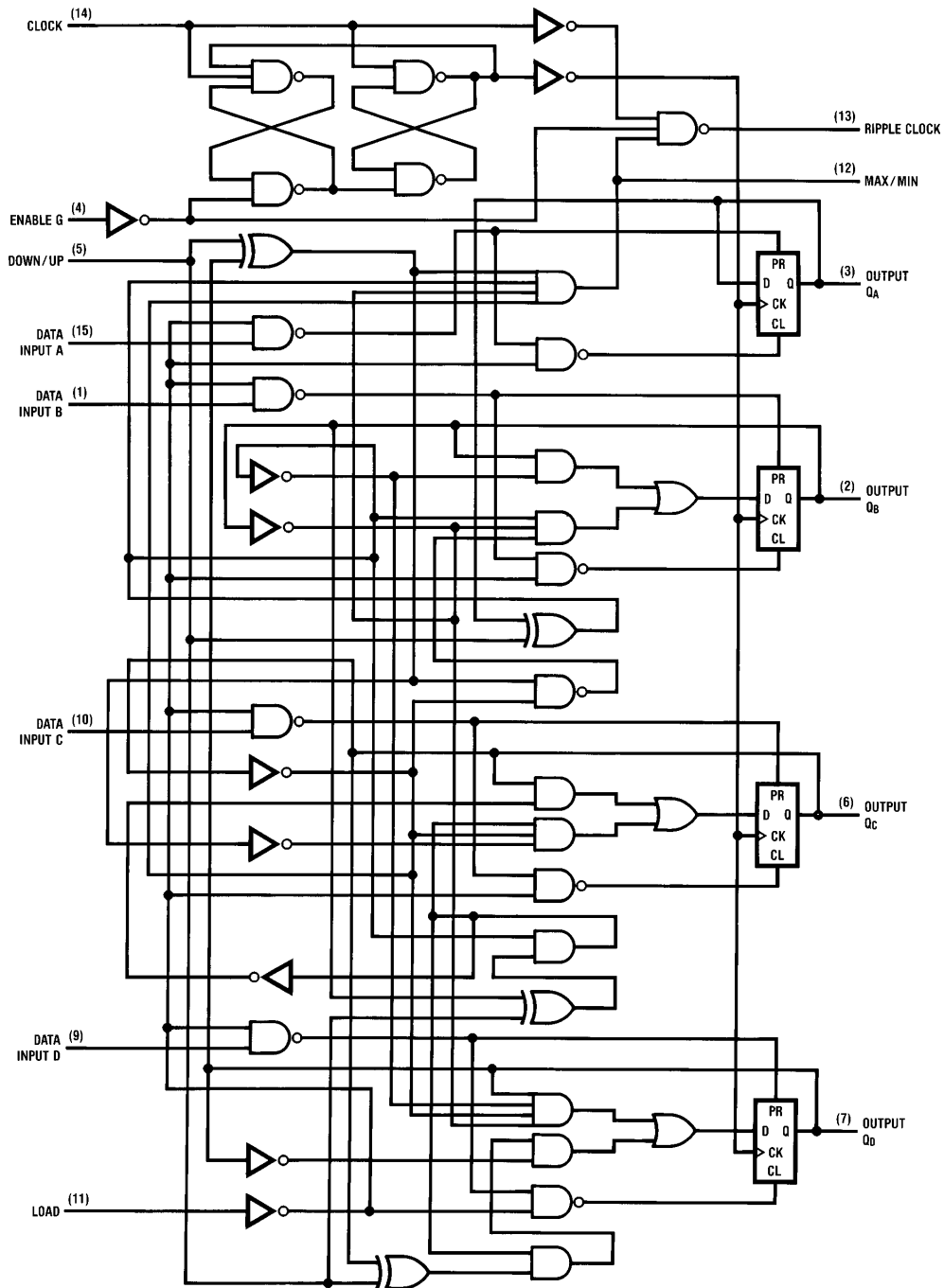
# Logic Diagram



TL/F/5744-3

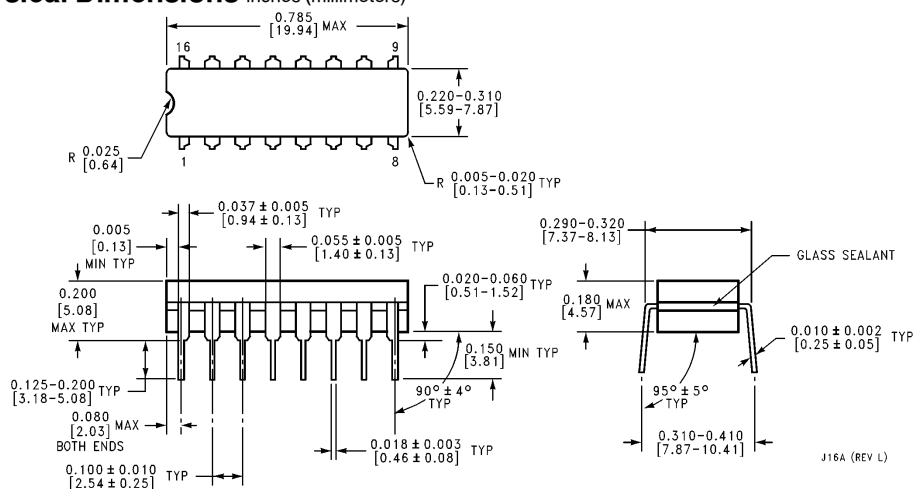
# Logic Diagram (Continued)

## 'HCT190 Decade Counters

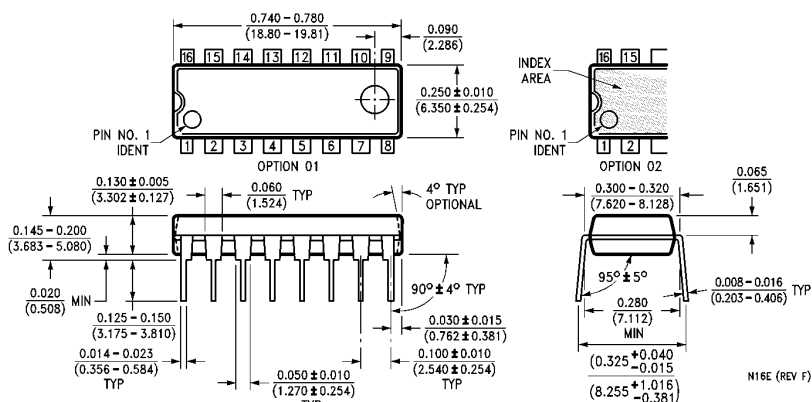


TL/F/5744-7

### Physical Dimensions inches (millimeters)



**Order Number MM54HCT191J or MM74HCT191J**  
**NS Package J16A**



**Order Number MM74HCT191N**  
**NS Package N16E**

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