

- **High-Performance Floating-Point Digital Signal Processor (DSP):**
 - SM/SMJ320VC33-150
 - 13-ns Instruction Cycle Time
 - 150 Million Floating-Point Operations Per Second (MFLOPS)
 - 75 Million Instructions Per Second (MIPS)
- **34K × 32-Bit (1.1-Mbit) On-Chip Words of Dual-Access Static Random-Access Memory (SRAM) Configured in 2 × 16K plus 2 × 1K Blocks to improve Internal Performance**
- **x5 Phase-Locked Loop (PLL) Clock Generator**
- **Very Low Power: < 200 mW @ 150 MFLOPS**
- **32-Bit High-Performance CPU**
- **16-/32-Bit Integer and 32-/40-Bit Floating-Point Operations**
- **Four Internally Decoded Page Strokes to Simplify Interface to I/O and Memory Devices**
- **Boot-Program Loader**
- **EDGEMODE Selectable External Interrupts**
- **32-Bit Instruction Word, 24-Bit Addresses**
- **Eight Extended-Precision Registers**
- **Fabricated Using the 0.18-μm (I_{eff} -Effective Gate Length) Timeline™ Technology by Texas Instruments (TI)**
- **On-Chip Memory-Mapped Peripherals:**
 - One Serial Port
 - Two 32-Bit Timers
 - Direct Memory Access (DMA) Coprocessor for Concurrent I/O and CPU Operation
- **164-Pin Low-Profile Quad Flatpack (HFG Suffix)**
- **144-Pin Non-hermetic Ceramic Ball Grid Array (CBGA) (GNM Suffix)**
- **Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **Two Low-Power Modes**
- **Two- and Three-Operand Instructions**
- **Parallel Arithmetic/Logic Unit (ALU) and Multiplier Execution in a Single Cycle**
- **Block-Repeat Capability**
- **Zero-Overhead Loops With Single-Cycle Branches**
- **Conditional Calls and Returns**
- **Interlocked Instructions for Multiprocessing Support**
- **Bus-Control Registers Configure Strobe-Control Wait-State Generation**
- **1.8-V (Core) and 3.3-V (I/O) Supply Voltages**

description

The SM/SMJ320VC33 DSP is a 32-bit, floating-point processor manufactured in 0.18-μm four-level-metal CMOS (Timeline) technology. The SM/SMJ320VC33 is part of the SM320C3x™ generation of DSPs from Texas Instruments.

The SM320C3x internal busing and special digital-signal-processing instruction set have the speed and flexibility to execute up to 150 million floating-point operations per second (MFLOPS). The SM/SMJ320VC33 optimizes speed by implementing functions in hardware that other processors implement through software or microcode. This hardware-intensive approach provides performance previously unavailable on a single chip.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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description (continued)

The SM/SMJ320VC33 can perform parallel multiply and ALU operations on integer or floating-point data in a single cycle. Each processor also possesses a general-purpose register file, a program cache, dedicated ARAUs, internal dual-access memories, one DMA channel supporting concurrent I/O, and a short machine-cycle time. High performance and ease of use are the results of these features.

General-purpose applications are greatly enhanced by the large address space, multiprocessor interface, internally and externally generated wait states, one external interface port, two timers, one serial port, and multiple-interrupt structure. The SM320C3x supports a wide variety of system applications from host processor to dedicated coprocessor. High-level-language support is easily implemented through a register-based architecture, large address space, powerful addressing modes, flexible instruction set, and well-supported floating-point arithmetic.

JTAG scan-based emulation logic

The 320VC33 contains a JTAG port for CPU emulation within a chain of any number of other JTAG devices. The JTAG port on this device does not include a pin-by-pin boundary scan for point-to-point board level test. The Boundary Scan tap input and output is internally connected with a single dummy register allowing loop back tests to be performed through that JTAG domain.

The JTAG emulation port of this device also includes two additional pins, EMU0 and EMU1, for global control of multiple processors conforming to the TI emulation standard. These pins are open collector-type outputs which are wire ORed and tied high with a pullup. Non-TI emulation devices should not be connected to these pins.

The VC33 instruction register is 8 bits long. Table 1 shows the instructions code. The uses of SAMPLE and HIGHZ opcodes, though defined, have no meaning for the SM/SMJ320VC33, which has no boundary scan. For example, HIGHZ will affect only the dummy cell (no meaning) and will not put the device pins in a high-impedance state.

Table 1. Boundary-Scan Instruction Code

| INSTRUCTION NAME | INSTRUCTION CODE |
|------------------------|------------------|
| EXTEST | 00000000 |
| BYPASS | 11111111 |
| SAMPLE | 00000010 |
| HIGHZ | 00000110 |
| PRIVATE1 [†] | 00000011 |
| PRIVATE2 [†] | 00100000 |
| PRIVATE3 [†] | 00100001 |
| PRIVATE4 [†] | 00100010 |
| PRIVATE5 [†] | 00100011 |
| PRIVATE6 [†] | 00100100 |
| PRIVATE7 [†] | 00100101 |
| PRIVATE8 [†] | 00100110 |
| PRIVATE9 [†] | 00100111 |
| PRIVATE10 [†] | 00101000 |
| PRIVATE11 [†] | 00101001 |

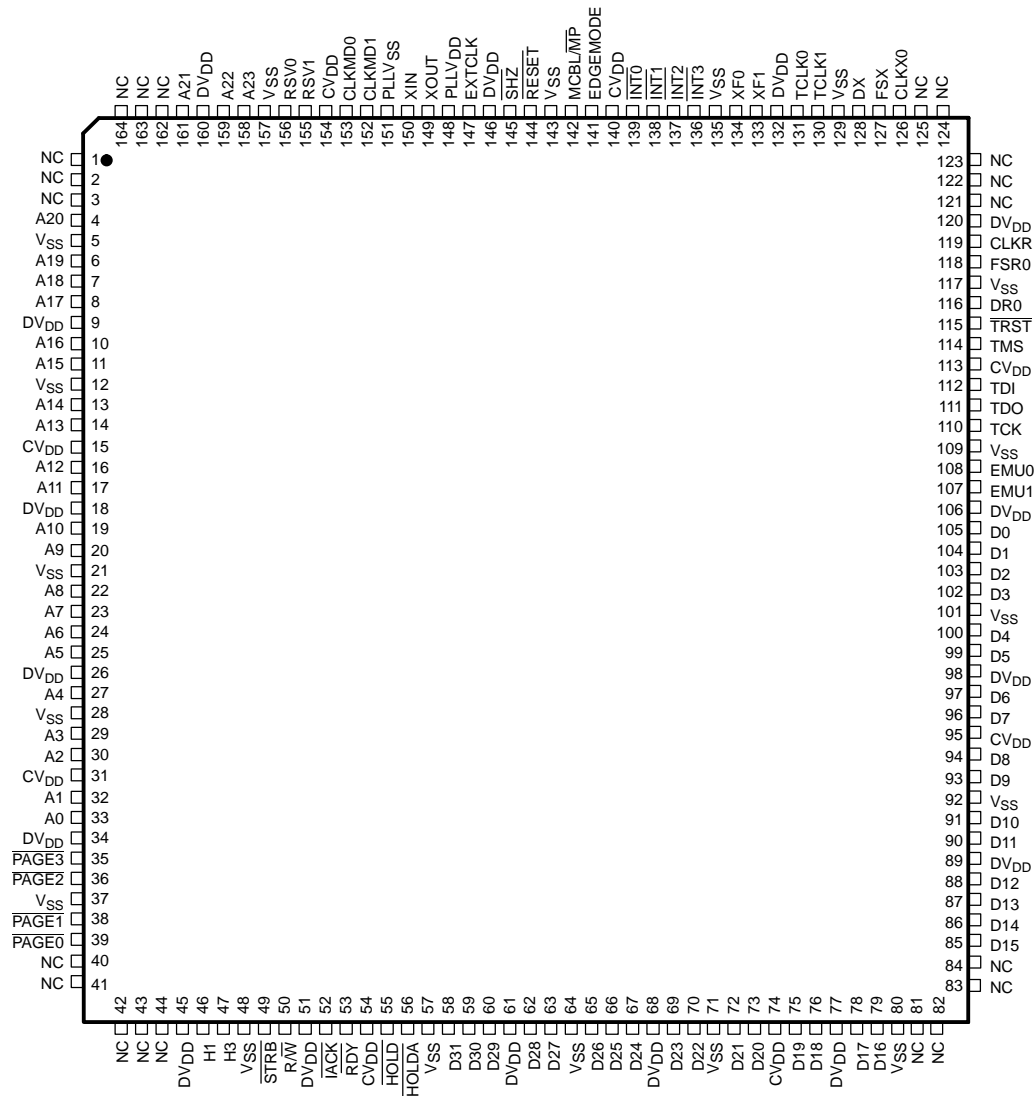
Boundry is only one dummy cell

Boundry is only one dummy cell

[†] Use of Private opcodes could cause the device to operate in an unexpected manner.

pinout

HFG PACKAGE†‡ (TOP VIEW)



NC - No internal connection

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

‡ PLLV_{DD} and PLLV_{SS} are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

The SM/SMJ320VC33 device is packaged in 164-pin low-profile quad flatpacks (HFG Suffix) and in 144-ball fine pitch ball grid arrays (GNL and GNM Suffix).

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GNM Terminal Assignments† (Sorted by Signal Name)

| SIGNAL NAME | PIN NUMBER | SIGNAL NAME | PIN NUMBER | SIGNAL NAME | PIN NUMBER | SIGNAL NAME | PIN NUMBER |
|------------------|------------|------------------|------------|-----------------------|------------|-----------------|------------|
| A0 | J2 | D0 | G12 | DV _{DD} | M1 | R/W | L4 |
| A1 | K2 | D1 | G10 | | N1 | RDY | M5 |
| A2 | K1 | D2 | F13 | | N4 | RESET | B7 |
| A3 | J4 | D3 | G11 | | N7 | RSV0 | B4 |
| A4 | H4 | D4 | H10 | | M8 | RSV1 | D5 |
| A5 | H3 | D5 | H13 | | N12 | SHZ | D7 |
| A6 | H1 | D6 | H12 | | L13 | STRB | M4 |
| A7 | G4 | D7 | J10 | | H11 | TCK | F10 |
| A8 | G1 | D8 | J11 | | F11 | TCLK0 | C10 |
| A9 | G2 | D9 | J12 | | B12 | TCLK1 | A11 |
| A10 | F3 | D10 | K13 | | A10 | TDI | E11 |
| A11 | F4 | D11 | K12 | | A6 | TDO | D13 |
| A12 | F2 | D12 | K10 | | A1 | TMS | E10 |
| A13 | E1 | D13 | M13 | DX0 | A12 | TRST | C13 |
| A14 | E2 | D14 | L11 | EDGEMODE | A7 | V _{SS} | B1 |
| A15 | E4 | D15 | L12 | EMU0 | F12 | | D1 |
| A16 | C1 | D16 | M12 | EMU1 | E12 | | G3 |
| A17 | C2 | D17 | L10 | EXTCLK | C6 | | J1 |
| A18 | D3 | D18 | K9 | FSR0 | C12 | | L2 |
| A19 | C3 | D19 | N11 | FSX | D10 | | M3 |
| A20 | B2 | D20 | M11 | H1 | L3 | | M6 |
| A21 | D4 | D21 | M10 | H3 | N2 | | L7 |
| A22 | A2 | D22 | K8 | HOLD | N5 | | N10 |
| A23 | B3 | D23 | N9 | HOLDA | K5 | | N13 |
| CLKMD0 | C5 | D24 | M9 | IACK | K4 | | K11 |
| CLKMD1 | B5 | D25 | L8 | INT0 | C8 | | G13 |
| CLKR0 | B13 | D26 | N8 | INT1 | B9 | | E13 |
| CLKX0 | B11 | D27 | M7 | INT2 | D8 | | A13 |
| CV _{DD} | E3 | D28 | K7 | INT3 | A9 | | C11 |
| | J3 | D29 | L6 | MCBL/MP | B8 | | C9 |
| | L5 | D30 | N6 | PAGE0 | M2 | | C7 |
| | L9 | D31 | K6 | PAGE1 | N3 | | C4 |
| | J13 | DR0 | D11 | PAGE2 | L1 | XF0 | B10 |
| | D12 | DV _{DD} | D2 | PAGE3 | K3 | XF1 | D9 |
| | A8 | | F1 | PLLVD _{DD} ‡ | A5 | XIN | B6 |
| | A3 | | H2 | PLLVS _{SS} ‡ | A4 | XOUT | D6 |

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

‡ PLLV_{DD} and PLLV_{SS} are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.



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GNM Terminal Assignments† (Sorted by Pin Number)

| PIN NUMBER | SIGNAL NAME | PIN NUMBER | SIGNAL NAME | PIN NUMBER | SIGNAL NAME | PIN NUMBER | SIGNAL NAME |
|------------|--------------------|------------|------------------|------------|------------------|------------|------------------|
| A1 | DV _{DD} | C11 | V _{SS} | G10 | D1 | L4 | R/W |
| A2 | A22 | C12 | FSR0 | G11 | D3 | L5 | CV _{DD} |
| A3 | CV _{DD} | C13 | TRST | G12 | D0 | L6 | D29 |
| A4 | PLL _{VSS} | D1 | V _{SS} | G13 | V _{SS} | L7 | V _{SS} |
| A5 | PLL _{VDD} | D2 | DV _{DD} | H1 | A6 | L8 | D25 |
| A6 | DV _{DD} | D3 | A18 | H2 | DV _{DD} | L9 | CV _{DD} |
| A7 | EDGEMODE | D4 | A21 | H3 | A5 | L10 | D17 |
| A8 | CV _{DD} | D5 | RSV1 | H4 | A4 | L11 | D14 |
| A9 | INT3 | D6 | XOUT | H10 | D4 | L12 | D15 |
| A10 | DV _{DD} | D7 | SHZ | H11 | DV _{DD} | L13 | DV _{DD} |
| A11 | TCLK1 | D8 | INT2 | H12 | D6 | M1 | DV _{DD} |
| A12 | DX | D9 | XF1 | H13 | D5 | M2 | PAGE0 |
| A13 | V _{SS} | D10 | FSX | J1 | V _{SS} | M3 | V _{SS} |
| B1 | V _{SS} | D11 | DR0 | J2 | A0 | M4 | STRB |
| B2 | A20 | D12 | CV _{DD} | J3 | CV _{DD} | M5 | RDY |
| B3 | A23 | D13 | TDO | J4 | A3 | M6 | V _{SS} |
| B4 | RSV0 | E1 | A13 | J10 | D7 | M7 | D27 |
| B5 | CLKMD1 | E2 | A14 | J11 | D8 | M8 | DV _{DD} |
| B6 | XIN | E3 | CV _{DD} | J12 | D9 | M9 | D24 |
| B7 | RESET | E4 | A15 | J13 | CV _{DD} | M10 | D21 |
| B8 | MCBL/MP | E10 | TMS | K1 | A2 | M11 | D20 |
| B9 | INT1 | E11 | TDI | K2 | A1 | M12 | D16 |
| B10 | XF0 | E12 | EMU1 | K3 | PAGE3 | M13 | D13 |
| B11 | CLKX0 | E13 | V _{SS} | K4 | IACK | N1 | DV _{DD} |
| B12 | DV _{DD} | F1 | DV _{DD} | K5 | HOLDA | N2 | H3 |
| B13 | CLKR | F2 | A12 | K6 | D31 | N3 | PAGE1 |
| C1 | A16 | F3 | A10 | K7 | D28 | N4 | DV _{DD} |
| C2 | A17 | F4 | A11 | K8 | D22 | N5 | HOLD |
| C3 | A19 | F10 | TCK | K9 | D18 | N6 | D30 |
| C4 | V _{SS} | F11 | DV _{DD} | K10 | D12 | N7 | DV _{DD} |
| C5 | CLKMD0 | F12 | EMU0 | K11 | V _{SS} | N8 | D26 |
| C6 | EXTCLK | F13 | D2 | K12 | D11 | N9 | D23 |
| C7 | V _{SS} | G1 | A8 | K13 | D10 | N10 | V _{SS} |
| C8 | INT0 | G2 | A9 | L1 | PAGE2 | N11 | D19 |
| C9 | V _{SS} | G3 | V _{SS} | L2 | V _{SS} | N12 | DV _{DD} |
| C10 | TCLK0 | G4 | A7 | L3 | H1 | N13 | V _{SS} |

† DV_{DD} is the power supply for the I/O pins while CV_{DD} is the power supply for the core CPU. V_{SS} is the ground for both the I/O pins and the core CPU.

‡ PLL_{VDD} and PLL_{VSS} are isolated PLL supply pins that should be externally connected to CV_{DD} and V_{SS}, respectively.

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Terminal Functions

| TERMINAL NAME | QTY | TYPE† | DESCRIPTION | CONDITIONS WHEN SIGNAL IS Z TYPE‡ |
|-----------------------|-----|-------|--|---|
| PRIMARY-BUS INTERFACE | | | | |
| D31- D0 | 32 | I/O/Z | 32-bit data port Data port bus keepers. (See Figure 9) | S H R S |
| A23- A0 | 24 | O/Z | 24-bit address port | S H R |
| R/W | 1 | O/Z | Read/write. R/W is high when a read is performed and low when a write is performed over the parallel interface. | S H R |
| STRB | 1 | O/Z | Strobe. For all external-accesses | S H |
| PAGE0 - PAGE3 | 1 | O/Z | Page strobes. Four decoded page strobes for external access | S H R |
| RDY | 1 | I | Ready. RDY indicates that the external device is prepared for a transaction completion. | |
| HOLD | 1 | I | Hold. When HOLD is a logic low, any ongoing transaction is completed. A23- A0, D31-D0, STRB, and R/W are placed in the high-impedance state and all transactions over the primary-bus interface are held until HOLD becomes a logic high or until the NOHOLD bit of the primary-bus-control register is set. | |
| HOLDA | 1 | O/Z | Hold acknowledge. HOLDA is generated in response to a logic-low on HOLD. HOLDA indicates that A23-A0, D31-D0, STRB, and R/W are in the high-impedance state and that all transactions over the bus are held. HOLDA is high in response to a logic-high of HOLD or the NOHOLD bit of the primary-bus-control register is set. | S |
| CONTROL SIGNALS | | | | |
| RESET | 1 | I | Reset. When RESET is a logic low, the device is in the reset condition. When RESET becomes a logic high, execution begins from the location specified by the reset vector. | |
| EDGEMODE | 1 | I | Edge mode. Enables interrupt edge mode detection. | |
| INT3- INT0 | 4 | I | External interrupts | |
| IACK | 1 | O/Z | Internal acknowledge. IACK is generated by the IACK instruction. IACK can be used to indicate when a section of code is being executed. | S |
| MCBL/MP | 1 | I | Microcomputer Bootloader/microprocessor mode-select | |
| SHZ | 1 | I | Shutdown high impedance. When active, SHZ places all pins in the high-impedance state. SHZ can be used for board-level testing or to ensure that no dual-drive conditions occur. CAUTION: A low on SHZ corrupts the device memory and register contents. Reset the device with SHZ high to restore it to a known operating condition. | |
| XF1, XF0 | 2 | I/O/Z | External flags. XF1 and XF0 are used as general-purpose I/Os or to support interlocked processor instruction. | S R |
| SERIAL PORT 0 SIGNALS | | | | |
| CLKR0 | 1 | I/O/Z | Serial port 0 receive clock. CLKR0 is the serial shift clock for the serial port 0 receiver. | S R |
| CLKX0 | 1 | I/O/Z | Serial port 0 transmit clock. CLKX0 is the serial shift clock for the serial port 0 transmitter. | S R |
| DR0 | 1 | I/O/Z | Data-receive. Serial port 0 receives serial data on DR0. | S R |
| DX0 | 1 | I/O/Z | Data-transmit output. Serial port 0 transmits serial data on DX0. | S R |
| FSR0 | 1 | I/O/Z | Frame-synchronization pulse for receive. The FSR0 pulse initiates the data-receive process using DR0. | S R |
| FSX0 | 1 | I/O/Z | Frame-synchronization pulse for transmit. The FSX0 pulse initiates the data-transmit process using DX0. | S R |

† I = input, O = output, Z = high-impedance state

‡ S = SHZ active, H = HOLD active, R = RESET active

§ Recommended decoupling. Four 0.1 µF for CV_{DD} and eight 0.1 µF for DV_{DD}.



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Terminal Functions (Continued)

| TERMINAL NAME | QTY | TYPE† | DESCRIPTION | CONDITIONS WHEN SIGNAL IS Z TYPE‡ |
|--------------------------------------|-----|-------|---|---|
| TIMER SIGNALS | | | | |
| TCLK0 | 1 | I/O/Z | Timer clock 0. As an input, TCLK0 is used by timer 0 to count external pulses. As an output, TCLK0 outputs pulses generated by timer 0. | S R |
| TCLK1 | 1 | I/O/Z | Timer clock 1. As an input, TCLK1 is used by timer 1 to count external pulses. As an output, TCLK1 outputs pulses generated by timer 1. | S R |
| SUPPLY AND OSCILLATOR SIGNALS | | | | |
| H1 | 1 | O/Z | External H1 clock | S |
| H3 | 1 | O/Z | External H3 clock | S |
| CV _{DD} | 8 | I | +V _{DD} . Dedicated 1.8-V power supply for the core CPU. All must be connected to a common supply plane.§ | |
| DV _{DD} | 16 | I | +V _{DD} . Dedicated 3.3-V power supply for the I/O pins. All must be connected to a common supply plane.§ | |
| V _{SS} | 18 | I | Ground. All grounds must be connected to a common ground plane. | |
| PLL _{VDD} | 1 | I | Internally isolated PLL supply. Connect to CV _{DD} (1.8 V) | |
| PLL _{VSS} | 1 | I | Internally isolated PLL ground. Connect to V _{SS} | |
| EXTCLK | 1 | I | External clock. Logic level compatible clock input. If the XIN/XOUT oscillator is used, tie this pin to ground. | |
| XOUT | 1 | O | Clock out. Output from the internal-crystal oscillator. If a crystal is not used, XOUT should be left unconnected. | |
| XIN | 1 | I | Clock in. Internal-oscillator input from a crystal. If EXTCLK is used, tie this pin to ground. | |
| CLKMD0, CLKMD1 | 2 | I | Clock mode select pins | |
| RSV0 - RSV1 | 2 | I | Reserved. Use individual pullups to DV _{DD} . | |
| JTAG EMULATION | | | | |
| EMU1- EMU0 | 2 | I/O | Emulation pins 0 and 1, use individual pullups to DV _{DD} | |
| TDI | 1 | I | Test data input | |
| TDO | 1 | O | Test data output | |
| TCK | 1 | I | Test clock | |
| TMS | 1 | I | Test mode select | |
| TRST | 1 | I | Test reset | |

† I = input, O = output, Z = high-impedance state

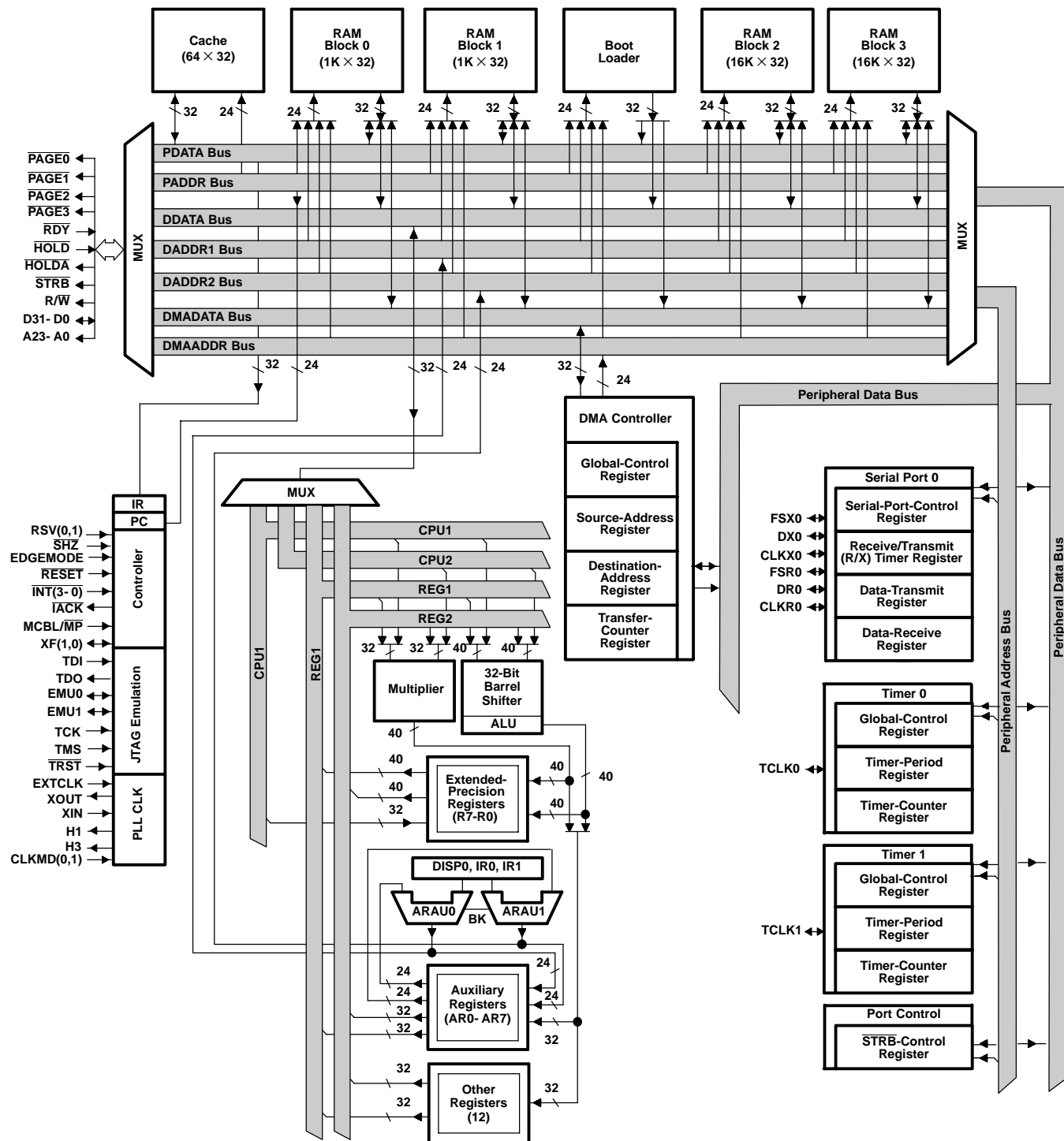
‡ S = $\overline{\text{SHZ}}$ active, H = $\overline{\text{HOLD}}$ active, R = $\overline{\text{RESET}}$ active

§ Recommended decoupling. Four 0.1 μF for CV_{DD} and eight 0.1 μF for DV_{DD}.

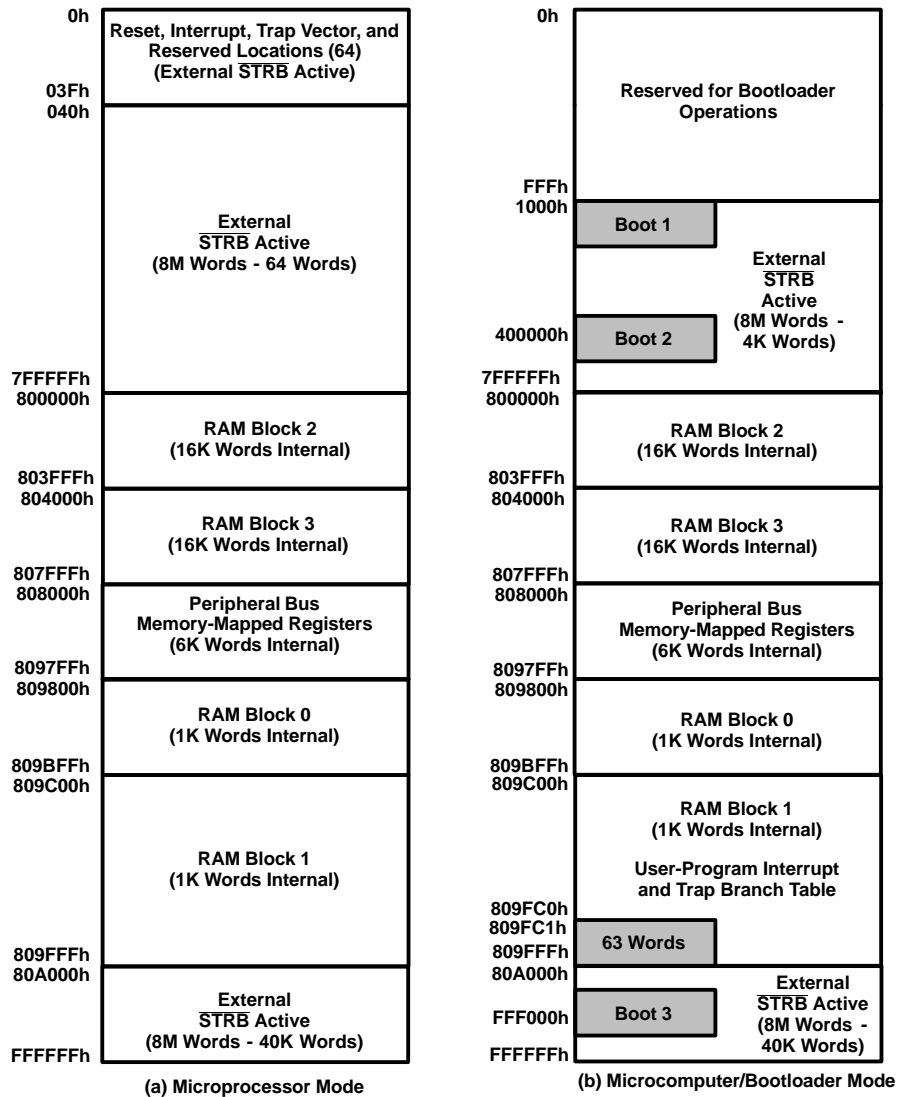
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functional block diagram



memory map



NOTE A: $\overline{\text{STRB}}$ is active over all external memory ranges. $\overline{\text{PAGE0}}$ to $\overline{\text{PAGE3}}$ are configured as external bus strobes. These are simple decoded strobes that have no configuration registers and are active only during external bus activity over the following ranges:

| Name | Active range |
|---------------------------|----------------------|
| $\overline{\text{PAGE0}}$ | 0000000h – 03FFFFFFh |
| $\overline{\text{PAGE1}}$ | 0400000h – 07FFFFFFh |
| $\overline{\text{PAGE2}}$ | 0800000h – 0BFFFFFFh |
| $\overline{\text{PAGE3}}$ | 0C00000h – 0FFFFFFFh |
| $\overline{\text{STRB}}$ | 0000000h – 0FFFFFFFh |

Figure 1. SM/SMJ320VC33 Memory Maps

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memory map (continued)

| | |
|-----|----------|
| 00h | Reset |
| 01h | INT0 |
| 02h | INT1 |
| 03h | INT2 |
| 04h | INT3 |
| 05h | XINT0 |
| 06h | RINT0 |
| 07h | Reserved |
| 08h | |
| 09h | TINT0 |
| 0Ah | TINT1 |
| 0Bh | DINT |
| 0Ch | Reserved |
| 1Fh | |
| 20h | TRAP 0 |
| | • |
| | • |
| | • |
| 3Bh | TRAP 27 |
| 3Ch | Reserved |
| 3Fh | |

(a) Microprocessor Mode

| | |
|---------|----------|
| 809FC1h | INT0 |
| 809FC2h | INT1 |
| 809FC3h | INT2 |
| 809FC4h | INT3 |
| 809FC5h | XINT0 |
| 809FC6h | RINT0 |
| 809FC7h | Reserved |
| 809FC8h | |
| 809FC9h | TINT0 |
| 809FCAh | TINT1 |
| 809FCBh | DINT |
| 809FCCh | Reserved |
| 809FDFh | |
| 809FE0h | TRAP 0 |
| | • |
| | • |
| | • |
| 809FFBh | TRAP 27 |
| 809FFCh | Reserved |
| 809FFFh | |

(b) Microcomputer/Bootloader Mode

Figure 2. Reset, Interrupt, and Trap Vector/Branches Memory-Map Locations

memory map (continued)

| | |
|---------|----------------------------------|
| 808000h | DMA Global Control |
| 808004h | DMA Source Address |
| 808006h | DMA Destination Address |
| 808008h | DMA Transfer Counter |
| 808020h | Timer 0 Global Control |
| 808024h | Timer 0 Counter |
| 808028h | Timer 0 Period Register |
| 808030h | Timer 1 Global Control |
| 808034h | Timer 1 Counter |
| 808038h | Timer 1 Period Register |
| 808040h | Serial Global Control |
| 808042h | FSX/DX/CLKX Serial Port Control |
| 808043h | FSR/DR/CLKR Serial Port Control |
| 808044h | Serial R/X Timer Control |
| 808045h | Serial R/X Timer Counter |
| 808046h | Serial R/X Timer Period Register |
| 808048h | Data-Transmit |
| 80804Ch | Data-Receive |
| 808064h | Primary-Bus Control |

NOTE A: Shading denotes reserved address locations.

Figure 3. Peripheral Bus Memory-Mapped Registers

clock generator

The clock generator provides clocks to the VC33 device, and consists of an internal oscillator and a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which can be provided by using a crystal resonator with the internal oscillator, or from an external clock source. The PLL circuit generates the device clock by multiplying the reference clock frequency by a x5 scale factor, allowing use of a clock source with a lower frequency than that of the CPU. The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal.

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PLL and clock oscillator control

The clock mode control pins are decoded into four operational modes as shown in Figure 4. These modes control clock divide ratios, oscillator, and PLL power (see Table 2).

When an external clock input or crystal is connected, the opposite unused input is simply grounded. An XOR gate then passes one of the two signal sources to the PLL stage. This allows the direct injection of a clock reference into EXTCLK, or 1-20 MHz crystals and ceramic resonators with the oscillator circuit. The two clock sources include:

- A crystal oscillator circuit, where a crystal or ceramic resonator is connected across the XOUT and XIN pins and EXTCLK is grounded.
- An external clock input, where an external clock source is directly connected to the EXTCLK pin, and XOUT is left unconnected and XIN is grounded.

When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. The PLL is a simple x5 reference multiplier with bypass and power control.

The clock divider, under CPU control, reduces the clock reference by 1 (MAXSPEED), 1/16 (LOWPOWER), or clock stop (IDLE2). Wake-up from the IDLE2 state is accomplished by a RESET or interrupt pin logic-low state.

A divide-by-two TMS320C31 equivalent mode of operation is also provided. In this case, the clock output reference is further divided by two with clock synchronization being determined by the timing of RESET falling relative to the present H1/H3 state.

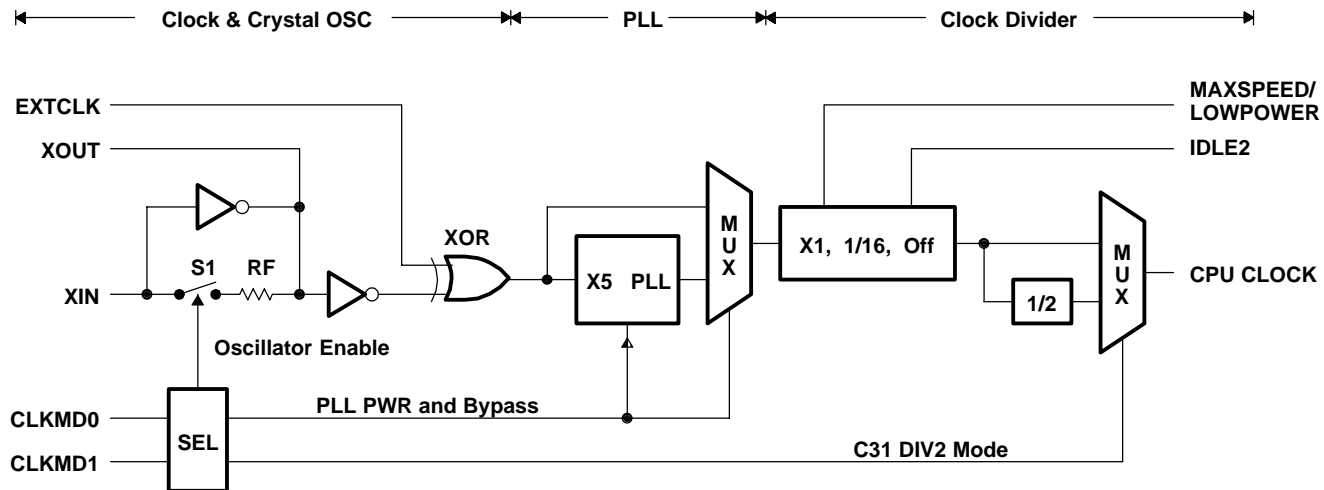


Figure 4. Clock Generation

Table 2. Clock Mode Select Pins

| CLKMD0 | CLKMD1 | FEEDBACK | PLLPWR | RATIO | NOTES |
|--------|--------|----------|--------|-------|--|
| 0 | 0 | Off | Off | 1 | Fully static, very low power |
| 0 | 1 | On | Off | 1/2 | Oscillator enabled |
| 1 | 0 | On | Off | 1 | Oscillator enabled |
| 1 | 1 | On | On | 5 | 2 mA @ 60 MHz, 1.8 V PLL power. Oscillator enabled |

PLL and clock oscillator control (continued)

Typical crystals in the 8-30 MHz range have a series resistance of 25 Ω , which increases below 8 MHz. To maintain proper filtering and phase relationships, R_d and Z_{out} of the oscillator circuit should be 10x-40x that of the crystal. A series compensation resistor (R_d), shown in Figure 5, is recommended when using lower frequency crystals. The XOUT output, the square wave inverse of XIN, is then filtered by the XOUT output impedance, C1 load capacitor, and R_d (if present). The crystal and C2 input load capacitor then refilters this signal, resulting in a XIN signal that is 75-85% of the oscillator supply voltage.

NOTE: Some ceramic resonators are available in a low-cost, three-terminal package that includes C1 and C2 internally. Typically, ceramic resonators do not provide the frequency accuracy of crystals.

NOTE: Better PLL stability can be achieved using the optional power supply isolation circuit shown in Figure 5. A similar filter can be used to isolate the PLLV_{SS}, as shown in Figure 6. PLLV_{DD} can also be directly connected to CV_{DD}.

Table 3. Typical Crystal Circuit Loading

| FREQUENCY (MHz) | R_d (Ω) | C1 (pF) | C2 (pF) | CL [†] (pF) | RL [†] (Ω) |
|-----------------|--------------------|---------|---------|----------------------|------------------------------|
| 2 | 4.7k | 18 | 18 | 12 | 200 |
| 5 | 2.2k | 18 | 18 | 12 | 60 |
| 10 | 470 | 15 | 15 | 12 | 30 |
| 15 | 0 | 15 | 12 | 12 | 25 |
| 20 | 0 | 9 | 9 | 10 | 25 |

[†] CL and RL are typical internal series load capacitance and resistance of the crystal.

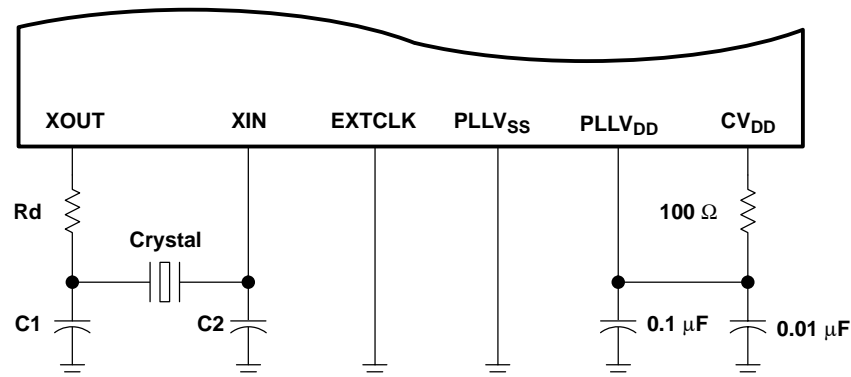


Figure 5. Self-Oscillation Mode

PLL isolation

The internal PLL supplies can be directly connected to CV_{DD} and V_{SS} (0 Ω case) or fully isolated as shown in Figure 6. The RC network prevents the PLL supplies from turning high frequency noise in the CV_{DD} and V_{SS} supplies into jitter.

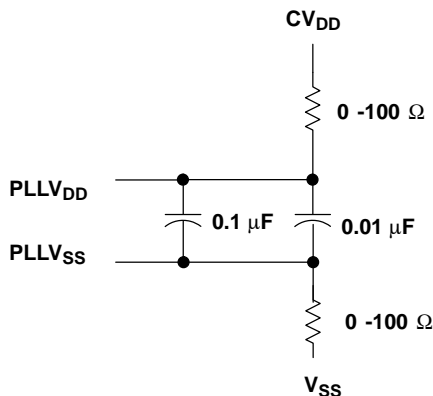


Figure 6. PLL Isolation Circuit Diagram

clock and PLL considerations on initialization

On power up, the CPU clock divide mode can be in MAXSPEED, LOPOWER or IDLE2, or the PLL could be in an undefined mode. RESET falling in the presence of a valid CPU clock is used to clear this state, after which the device will synchronously terminate any external activity.

The 5x Fclk_{in} PLL of the 320VC33 contains an 8-bit PLL-LOCK counter that will cause the PLL to output a frequency of Fclk_{in}/2 during the initial ramp. This counter, however, does not increment while RESET is low or in the absence of an input clock. A minimum of 256 input clocks are required before the first falling edge of reset for the PLL to output to clear this counter. The setup and behavior that is seen is as follows.

Power is applied to the DSP with RESET low and the input clock high or low. A clock is applied (RESET is still low) and the PLL appears to lock on to the input clock, producing the expected x5 output frequency. RESET is driven high and the PLL output immediately drops to Fclk_{in}/2 for up to 256 input cycles or 128 of the Fclk_{in}/2 output cycles. The PLL/CPU clock then switches to x5 mode.

The switch over is synchronous and does not create a clock glitch, so the only effect is that the CPU will run slow for up to the first 128 cycles after reset goes high. Once the PLL has stabilized, the counter will remain cleared and subsequent resets will not exhibit this condition.

power sequencing considerations

Though an internal ESD and CMOS latchup protection diode exists between CV_{DD} and DV_{DD} , it should not be considered a current-carrying device on power up. An external Schottky diode should be used to prevent CV_{DD} from exceeding DV_{DD} by more than 0.7 V. The effect of this diode during power up is that if CV_{DD} is powered up first, DV_{DD} will follow by one diode drop even when the DV_{DD} supply is not active.

Typical systems using LDOs of the same family type for both DV_{DD} and CV_{DD} will track each other during power up. In most cases, this is acceptable; but if a high-impedance pin state is required on power up, the SHZ pin can be used to asynchronously disable all outputs. RESET should not be used in this case since some signals require an active clock for RESET to have an effect and the clock may not yet be active. The internal core logic becomes functional at approximately 0.8 V while the external pin IO becomes active at about 1.5 V.

EDGEMODE

When EDGEMODE = 1, a sampled digital delay line is decoded to generate a pulse on the falling edge of the interrupt pin. To ensure interrupt recognition, input signal logic-high and logic-low states must be held longer than the synchronizer delay of one CPU clock cycle. Holding these inputs to no less than two cycles in both the logic-low and logic-high states is sufficient.

When EDGEMODE = 0, a logic-low interrupt pin will continually set the corresponding interrupt flag. The CPU or DMA can clear this flag within two cycles of it being set. This is the maximum interrupt width that can be applied if only one interrupt is to be recognized. The CPU can manually clear IF bits within an interrupt service routine (ISR), effectively lengthening the maximum ISR width.

After reset, EDGEMODE is temporarily disabled, allowing logic-low INT pins to be detected for bootstrap operation.

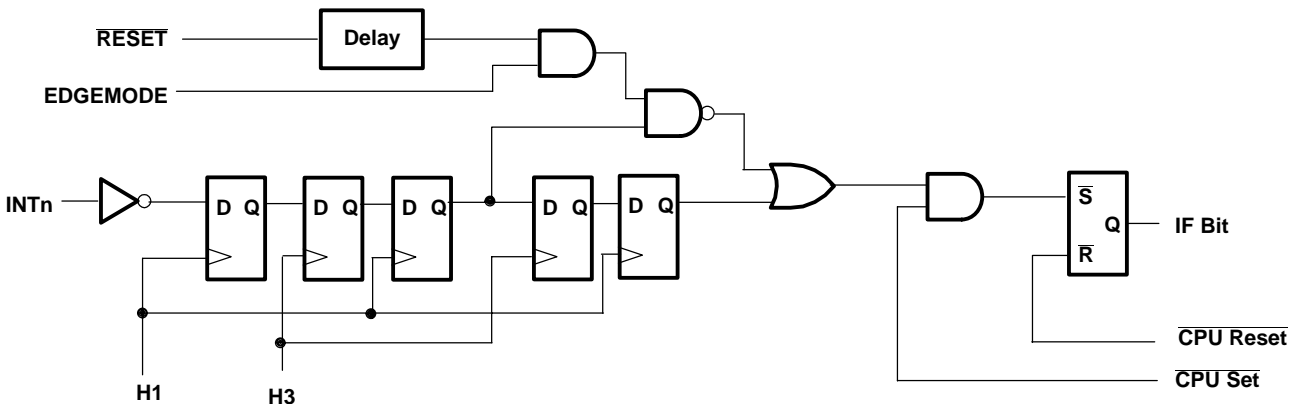


Figure 7. EDGEMODE and Interrupt Flag Circuit

reset operation

When RESET is applied, the CPU attempts to safely exit any pending read or write operations that may be in progress. This can take as much as 10 CPU cycles, after which, the address, data, and control pins will be in an inactive or high-impedance state.

When both RESET and SHZ are applied, the device will immediately enter the reset state with the pins held in high-impedance mode. SHZ should then be disabled at least 10 CPU cycles before RESET is set high. SHZ can be used during power-up sequencing to prevent undefined address, data, and control pins, avoiding system conflicts.

PAGE0 - PAGE3 select lines

To facilitate simpler and higher speed connection to external devices, the SM/SMJ320VC33 includes four predecoded select pins that have the same timings as STRB. These pins are decoded from A22, A23, and STRB and are active only during external accesses over the ranges shown in Table 4. All external bus accesses are controlled by a single bus control register.

Table 4. PAGE0 - PAGE3 Ranges

| | START | END |
|-------|----------|------------|
| PAGE0 | 0x000000 | 0x3FFFFFF |
| PAGE1 | 0x400000 | 0x7FFFFFF |
| PAGE2 | 0x800000 | 0xBFFFFFF |
| PAGE3 | 0xC00000 | 0xFFFFFFFF |

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using external logic with the $\overline{\text{READY}}$ pin

The key to designing external wait-state logic is the internal bus control register and associated internal logic that logically combines the external $\overline{\text{READY}}$ pin with the much faster on-chip bus control logic. This essentially allows slow external logic to interact with the bus while easily meeting the $\overline{\text{READY}}$ input timings. It is also relevant to mention that the combined ready signals are sampled on the rising edge of the internal H1 clock. Please refer to Figure 8 for the following examples.

example 1

A simple 0 or WTCNT wait-state decoder can be created by simply tying an address line back to the $\overline{\text{READY}}$ pin and selecting the AND option. When the tied back address is low, the bus will run with 0 wait states. When the tied back address is high, the bus will be controlled by the internal wait-state counter.

By enabling the bank compare logic, proper operation is further ensured by inserting a null cycle before a read on the next bank is performed (writes are not pre-extended). This extra time can also be used by external logic to affect the feedback path.

example 2

An N-WTCNT minimum wait-state decoder can also be created by tying back an address line to $\overline{\text{READY}}$ and logically ORing it with the internal bank compare and wait count signals. When the address pin is low, bus timing is determined by the internal WTCNT and BNKCMP settings. When the address line is high, the bus can run no faster than the WTCNT counter and will be extended as long as $\overline{\text{READY}}$ is held high.

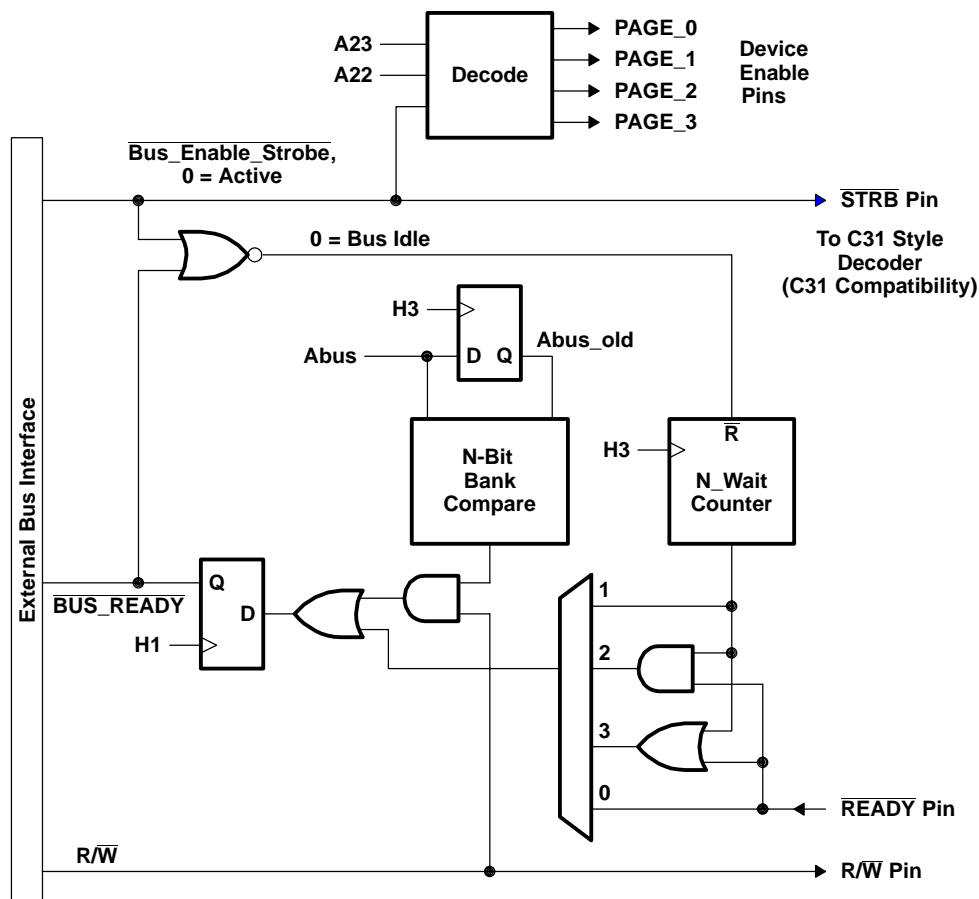


Figure 8. Internal Ready Logic, Simplified Diagram

example 2 (continued)

Table 5. MUX Select (Bus Control Register Bits 4 and 3)

| BIT 4 | BIT 3 | RESULTS |
|-------|-------|---|
| 0 | 0 | Ignore internal wait counter and use only external READY |
| 0 | 1 | Use only internal wait counter and ignore ready pin |
| 1 | 0 | Logically AND internal wait counter with ready pin |
| 1 | 1 | Logically OR internal wait counter with ready pin (reset default) |

posted writes

External writes are effectively "posted" to the bus, which then acts like an output latch until the write completes. Therefore, if the application code is executing internally, it can perform a very slow external write with no penalty since the bus acts like it has a one-level-deep write FIFO.

data bus I/O buffer

The circuit shown in Figure 9 is incorporated into each data pin to lightly "hold" the last driven value on the data bus pins when the DSP or an external device is not actively driving the bus. Each bus keeper is built from a three-state driver with nominal 15 k Ω output resistance which is fed back to the input in a positive feedback configuration. The resistance isolated driver then pulls the output in one direction or the other keeping the last driven value. This circuit is enabled in all functional modes and is only disabled when $\overline{\text{SHZ}}$ is pulled low.

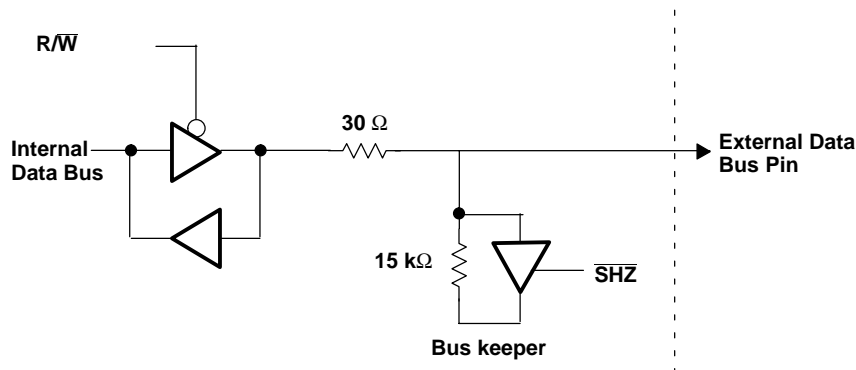


Figure 9. Bus Keeper Circuit

For an external device to change the state of these pins, it must be able to drive a small dc current until the driver threshold is crossed. At the crossover point, the driver changes state, agreeing with the external driver and assisting the change. The voltage threshold of the bus keeper is approximately at 50% of the DV_{DD} supply voltage. The typical output impedance of 30 Ω for all SM/SMJ320VC33 I/O pins is easily capable of meeting this requirement.

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bootloader operation

When $\text{MCBL}/\overline{\text{MP}} = 1$, an internal ROM is decoded into the address range of 0x000000-0x000FFF. Therefore, when reset occurs, execution begins within the internal ROM program and vector space. No external activity will be evident until one of the boot options is enabled. These options are enabled by pulling an external interrupt pin low, which the boot-load software then detects, causing a particular routine to be executed (see Table 6).

Table 6. INT0 - INT3 Sources

| ACTIVE INTERRUPT | ADDRESS/SOURCE WHERE BOOT DATA IS READ FROM | DATA FORMAT |
|------------------|---|---|
| INT0 | 0x001000 | 8, 16, or 32-bit width |
| INT1 | 0x400000 | 8, 16, or 32-bit width |
| INT2 | 0xFFFF00 | 8, 16, or 32-bit width |
| INT3 | Serial Port | 32-bit, external clock, and frame synch |

When $\text{MCBL}/\overline{\text{MP}} = 1$, the reset and interrupt vectors are hard-coded within the internal ROM. Since this is a read-only device, these vectors cannot be modified. To enable user-defined interrupt routines, the internal vectors contain fixed values that point to an internal section of SRAM beginning at 0x809FC1. Code execution begins at these locations so it is important to place branch instructions (to the interrupt routine) at these locations and not vectors.

The bootloader program requires a small stack space for calls and returns. Two SRAM locations at 0x809800 and 0x809801 are used for this stack. Data should not be boot loaded into these locations as this will corrupt the bootloader program run-time stack. After the boot-load operation is complete, a program can reclaim these locations. The simplest solution is to begin a program stack or uninitialized data section at 0x809800.

For additional detail on bootloader operation including the bootloader source code, see the *TMS320C3x User's Guide* (literature number SPRU031).

A bit I/O line or external logic can be used to safely disable the MCBL mode after bootloading is complete. However, to ensure proper operation, the CPU should not be currently executing code or using external data as the change takes place. In the following example, the XF0 pin is 3-state on reset, which allows the pullup resistor to place the DSP in MCBL mode. The following code, placed at the beginning of an application then causes the XF0 pin to become an active-logic-low output, changing the DSP mode to MP. The cache-enable and RPTS instructions are used since they cause the LDI instruction to be executed multiple times even though it has been fetched only once (before the mode change). In other words, the RPTS instruction acts as a one-level-deep program cache for externally executed code. If the application code is to be executed from internal RAM, no special provisions are needed.

```
LDI    8000h, ST    ; Enable the cache
RPTS   4            ; RPTS will fetch the following opcode 1 time
LDI    2h, IOF      ; Drive MCBL/MP=0 for several cycles allowing
                    ; the pipeline to clear
```

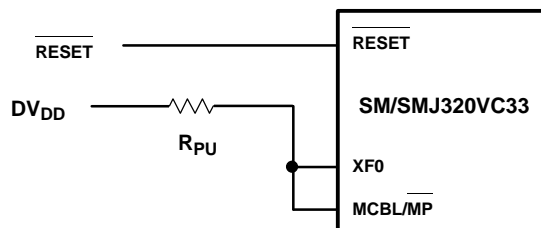


Figure 10. Changing Bootload Select Pin

JTAG emulation

Though the 320VC33 contains a JTAG debug port which allows multiple JTAG enabled chips to be daisy-chained, boundary scan of the pins is not supported. If the pin scan path is selected, it will be routed through a null register with a length of one. For additional information concerning the emulation interface, see *JTAG/MPSD Emulation Technical Reference* (literature number SPDU079).

designing a target system emulator connector (14-pin header)

JTAG target devices support emulation through a dedicated emulation port. This port is a superset of the test access port standard and is accessed by the emulator. To communicate with the emulator, **the target system must have a 14-pin header** (two rows of seven pins) with the connections that are shown in Figure 11. Table 7 describes the emulation signals.

| | | | |
|-----------------------|----|----|---------------------------|
| TMS | 1 | 2 | TRST |
| TDI | 3 | 4 | GND |
| PD (V _{CC}) | 5 | 6 | no pin (key) [†] |
| TDO | 7 | 8 | GND |
| TCK_RET | 9 | 10 | GND |
| TCK | 11 | 12 | GND |
| EMU0 | 13 | 14 | EMU1 |

Header Dimensions:
Pin-to-pin spacing, 0.100 in. (X,Y)
Pin width, 0.025-in. square post
Pin length, 0.235-in. nominal

[†] While the corresponding female position on the cable connector is plugged to prevent improper connection, the cable lead for pin 6 is present in the cable and is grounded, as shown in the schematics and wiring diagrams in this document.

Figure 11. 14-Pin Header Signals and Header Dimensions

Table 7. 14-Pin Header Signal Descriptions

| SIGNAL | DESCRIPTION | EMULATOR [†] STATE | TARGET [†] STATE |
|----------------------|--|--------------------------------|------------------------------|
| TMS [‡] | Test mode select | O | I |
| TDI | Test data input | O | I |
| TDO | Test data output | I | O |
| TCK | Test clock. TCK is a 10.368-MHz clock source from the emulation cable pod. This signal can be used to drive the system test clock | O | I |
| TRST [§] | Test reset | O | I |
| EMU0 [¶] | Emulation pin 0 | I | I/O |
| EMU1 [¶] | Emulation pin 1 | I | I/O |
| PD(V _{CC}) | Presence detect. Indicates that the emulation cable is connected and that the target is powered up. PD should be tied to V _{CC} in the target system. | I | O |
| TCK_RET | Test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK. | I | O |
| GND | Ground | | |

[†] I = input; O = output

[‡] Use 1-50K pullups for TMS, EMU0 and EMU1.

[§] Use 1-50K pulldown for TRST. Do not use pullup resistors on TRST: it has an internal pulldown device. In a low-noise environment, TRST can be left floating. In a high-noise environment, an additional pulldown resistor may be needed. (The size of this resistor should be based on electrical current considerations.)

[¶] EMU0 and EMU1 are I/O drivers configured as open-drain (open-collector) drivers. They are used as bidirectional signals for emulation global start and stop.

designing a target system emulator connector (14-pin header) (continued)

Although other headers can be used, recommended parts include:

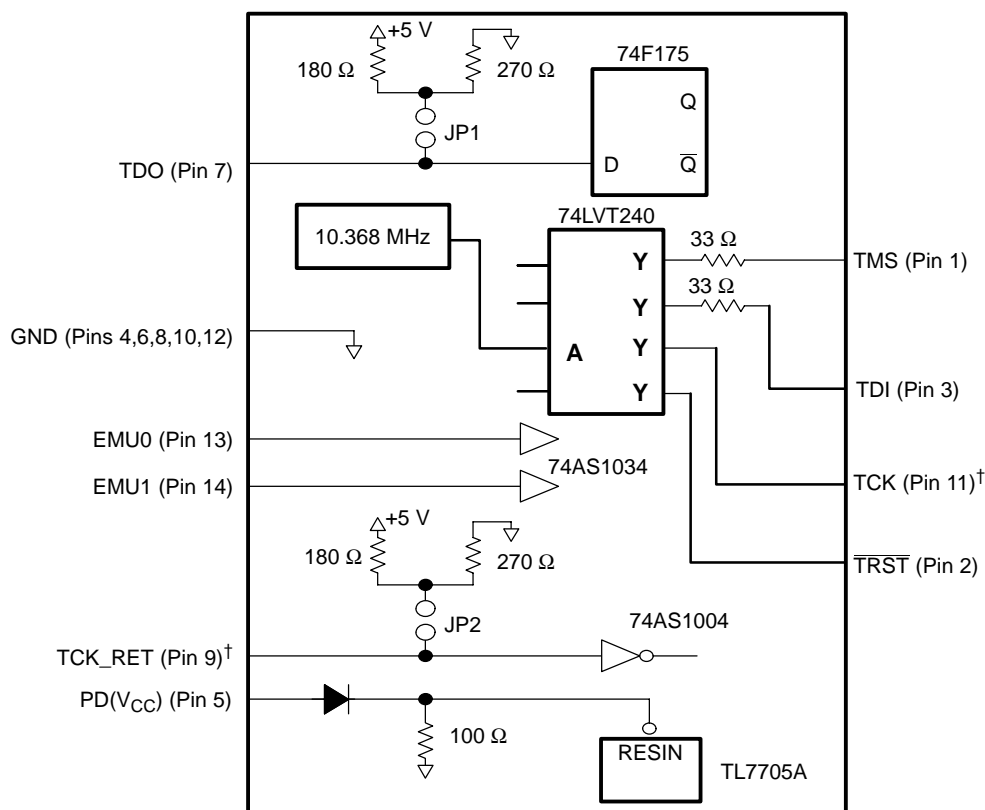
straight header, unshrouded

DuPont Connector Systems
part numbers: 65610-114
65611-1 14
67996-114
67997-114

JTAG emulator cable pod logic

Figure 12 shows a portion of the emulator cable pod. The functional features of the pod are as follows:

- Signals TDO and TCK_RET can be parallel-terminated inside the pod if required by the application. By default, these signals are not terminated.
- Signal TCK is driven with a 74LVT240 device. Because of the high-current drive ($32\text{ mA } I_{OL}/I_{OH}$), this signal can be parallel-terminated. If TCK is tied to TCK_RET, the parallel terminator in the pod can be used.
- Signals TMS and TDI can be generated from the falling edge of TCK_RET, according to the bus slave device timing rules.
- Signals TMS and TDI are series-terminated to reduce signal reflections.
- A 10.368-MHz test clock source is provided. Another test clock can be used for greater flexibility.



† The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK is provided as an optional target system test clock source.

Figure 12. JTAG Emulator Cable Pod Interface

device and development support tool nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ DSP family devices and support tools. Each TMS320™ DSP member has one of three prefixes: TMX, TMP, or TMS. Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX/TMDX) through fully qualified production devices/tools (TMS/TMDS). This development flow is defined below.

Device development evolutionary flow:

- SMX** Experimental device that is not necessarily representative of the final device's electrical specifications
- TMP** Final silicon die that conforms to the device's electrical specifications but has not completed quality and reliability verification
- SM/SMJ** Fully-qualified production device

Support tool development evolutionary flow:

- TMDX** Development support product that has not yet completed Texas Instruments internal qualification testing.
- TMDS** Fully qualified development support product

TMX and TMP devices and TMDX development support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

TMS devices and TMDS development support tools have been characterized fully, and the quality and reliability of the device has been demonstrated fully. TI's standard warranty applies.

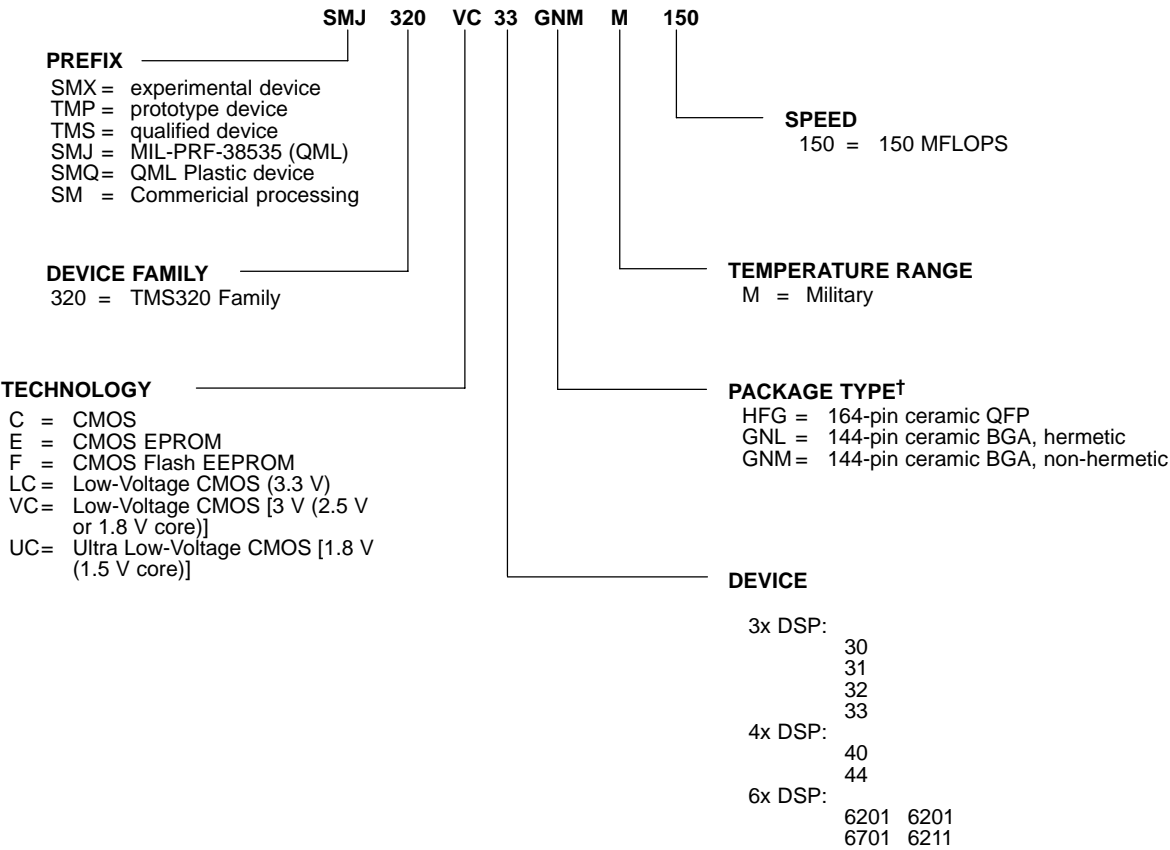
Predictions show that prototype devices (TMX or TMP) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, HFG, GNM, or GNL) and temperature range (for example, M). Figure 13 provides a legend for reading the complete device name for any TMS320™ DSP family member.

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device and development support tool nomenclature (continued)



† QFP = Quad Flat Package
LQFP = Low-Profile Quad Flat Package
BGA = Ball Grid Array

Figure 13. TMS320™ DSP Device Nomenclature

absolute maximum ratings over specified temperature range (unless otherwise noted)[†]

| | |
|--|-------------------|
| Supply voltage range, DV_{DD}^{\ddagger} | - 0.3 V to 4 V |
| Supply voltage range, CV_{DD}^{\ddagger} | - 0.3 V to 2.4 V |
| Input voltage range, V_I^{\S} | - 1 V to 4.6 V |
| Output voltage range, V_O | - 0.3 V to 4.6 V |
| Continuous power dissipation (worst case) [¶] | 500 mW |
| Operating case temperature range, T_C | -55 °C to 125 °C |
| Storage temperature range, T_{stg} | - 55 °C to 150 °C |

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

[‡] All voltage values are with respect to V_{SS} .

[§] Absolute dc input level should not exceed the DV_{DD} or V_{SS} supply rails by more than 0.3 V. An instantaneous low current pulse of < 2 ns, < 10 mA, and < 1 V amplitude is permissible.

[¶] Actual operating power is much lower. This value was obtained under specially produced worst-case test conditions for the SM/SMJ320VC33, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern to the external data and address buses at the maximum possible rate with a capacitive load of 30 pF. See normal (I_{CC}) current specification in the electrical characteristics table and also read *TMS320C3x General-Purpose Applications* (literature number SPRU194).

recommended operating conditions^{‡¶||}

| | MIN | NOM | MAX | UNIT |
|--|-------------------|-----|----------------------|------|
| CV_{DD} Supply voltage for the core CPU [☆] | 1.71 | 1.8 | 1.89 | V |
| DV_{DD} Supply voltage for the I/O pins [□] | 3.14 | 3.3 | 3.46 | V |
| V_{SS} Supply ground | | 0 | | V |
| V_{IH} High-level input voltage | 0.7 x DV_{DD} | | $DV_{DD} + 0.3^{\S}$ | V |
| V_{IL} Low-level input voltage | -0.3 [§] | | 0.3 x DV_{DD} | V |
| I_{OH} High-level output current | | | 4 | mA |
| I_{OL} Low-level output current | | | 4 | mA |
| T_C Operating case temperature | -55 | | 125 | °C |
| C_L Capacitive load per output pin | | | 30 | pF |

[‡] All voltage values are with respect to V_{SS} .

[§] Absolute dc input level should not exceed the DV_{DD} or V_{SS} supply rails by more than 0.3 V. An instantaneous low current pulse of < 2 ns, < 10 mA, and < 1 V amplitude is permissible.

[#] All inputs and I/O pins are configured as inputs.

^{||} All input and I/O pins use a Schmidt hysteresis inputs except \overline{SHZ} and D0-D31. Hysteresis is approximately 10% of DV_{DD} and is centered at 0.5 x DV_{DD} .

[☆] CV_{DD} should not exceed DV_{DD} by more than 0.7 V. (Use a Schottky clamp diode between these supplies.)

[□] DV_{DD} should not exceed CV_{DD} by more than 2.5 V.

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electrical characteristics over recommended ranges of supply voltage (unless otherwise noted)[†]

| PARAMETER | | TEST CONDITIONS [‡] | MIN | TYP [§] | MAX | UNIT |
|------------------|---|---|------|------------------|-----|------|
| V _{OH} | High-level output voltage | DV _{DD} = MIN, I _{OH} = MAX | 2.4 | | | V |
| V _{OL} | Low-level output voltage | DV _{DD} = MIN, I _{OL} = MAX | | | 0.4 | V |
| I _Z | High-impedance current | T _C = 25°C, DV _{DD} = MAX | -5 | | +5 | μA |
| I _I | Input current | T _C = 25°C, V _I = V _{SS} to DV _{DD} | -5 | | +5 | μA |
| I _{IPU} | Input current (with internal pullup) | Inputs with internal pullups [¶] | -600 | | 10 | μA |
| I _{IPD} | Input current (with internal pulldown) | Inputs with internal pulldowns [¶] | 600 | | -10 | μA |
| I _{BKU} | Input current (with bus keeper) pullup [#] | Bus keeper opposes until conditions match | -600 | | 10 | μA |
| I _{BKD} | Input current (with bus keeper) pulldown [#] | | 600 | | -10 | μA |
| I _{DDD} | Supply current, pins ★ | T _C = 25°C, f _x = 75 MHz DV _{DD} = MAX | | 25 | 260 | mA |
| I _{DDC} | Supply current, core CPU ★ | T _C = 25°C, f _x = 75 MHz CV _{DD} = MAX | | 60 | 215 | mA |
| I _{DD} | IDLE2, Supply current, I _{DDD} plus I _{DDC} | PLL enabled, oscillator enabled | | 2 | | mA |
| | | PLL disabled, oscillator enabled | | 500 | | μA |
| | | PLL disabled, oscillator disabled, FCLK = 0 | | 50 | | |
| C _i | Input capacitance | All inputs except XIN | | | 10* | pF |
| | | XIN | | | 10* | |
| C _o | Output capacitance | | | | 10* | pF |

* Not production tested

[†] All voltage values are with respect to V_{SS}.

[‡] For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

[§] For VC33, all typical values are at DV_{DD} = 3.3, CV_{DD} = 1.8 V, T_C (case temperature) = 25°C.

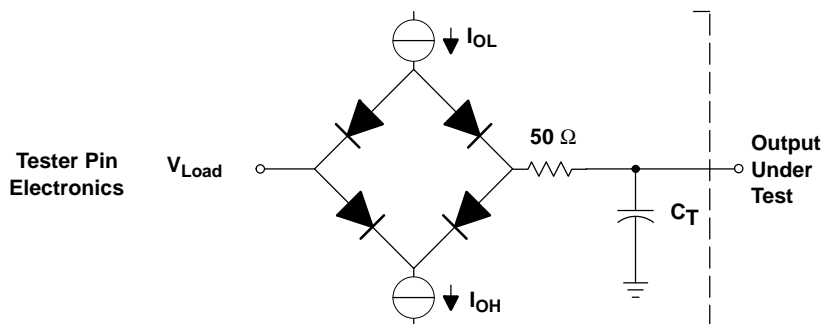
[¶] Pins with internal pullup devices: TDI, TCK, and TMS. Pin with internal pulldown device: TRST.

[#] Pins D0-D31 include internal bus keepers that maintain valid logic levels when the bus is not driven (see Figure 9).

^{||} Actual operating current is less than this maximum value. This value was obtained under specially produced worst-case test conditions, which are not sustained during normal device operation. These conditions consist of continuous parallel writes of a checkerboard pattern at the maximum rate possible. See *TMS320C3x General-Purpose Applications* (literature number SPRU194).

★f_x is the PLL output clock frequency.

PARAMETER MEASUREMENT INFORMATION



Where: I_{OL} = 4 mA (all outputs) for dc levels test.
I_O and I_{OH} are adjusted during ac timing analysis to achieve an ac termination of 50 Ω
V_{LOAD} = DV_{DD}/2
C_T = 40-pF typical load-circuit capacitance

Figure 14. Test Load Circuit

PARAMETER MEASUREMENT INFORMATION

timing parameter symbology

Timing parameter symbols used herein were created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows, unless otherwise noted:

Lowercase subscripts and their meanings

| | |
|-----|--|
| a | access time |
| c | cycle time (period) |
| d | delay time |
| dis | disable time |
| en | enable time |
| f | fall time |
| h | hold time |
| r | rise time |
| su | setup time |
| t | transition time |
| v | valid time |
| w | pulse duration (width) |
| x | unknown, changing, or don't care level |

Letters and symbols and their meanings

| | |
|---|----------------|
| H | High |
| L | Low |
| V | Valid |
| Z | High Impedance |

Additional symbols and their meaning

| | | | |
|---------|---|-------|----------------------------------|
| A | Address lines (A23- A0) | H | H1 and H3 |
| ASYNCH | Asynchronous reset signals (XF0, XF1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, TCLK0, and TCLK1) | HOLD | $\overline{\text{HOLD}}$ |
| CLKX | CLKX0 | HOLDA | $\overline{\text{HOLDA}}$ |
| CLKR | CLKR0 | IACK | $\overline{\text{IACK}}$ |
| CONTROL | Control signals | INT | $\overline{\text{INT3- INT0}}$ |
| D | Data lines (D31- D0) | PAGE | $\overline{\text{PAGE0- PAGE3}}$ |
| DR | DR | RDY | RDY |
| DX | DX | RW | R/ $\overline{\text{W}}$ |
| EXTCLK | EXTCLK | RW | R/ $\overline{\text{W}}$ |
| FS | FSX/R | RESET | RESET |
| FSX | FSX0 | S | $\overline{\text{STRB}}$ |
| FSR | FSR0 | SCK | CLKX/R |
| GPI | General-purpose input | SHZ | $\overline{\text{SHZ}}$ |
| GPIO | General-purpose input/output; peripheral pin (CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, TCLK0, and TCLK1) | TCLK | TCLK0, TCLK1, or TCLKx |
| GPO | General-purpose output | XF | XF0, XF1, or XFx |
| H1 | H1 | XF0 | XF0 |
| H3 | H3 | XF1 | XF1 |
| | | XIN | XIN |

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phase-locked loop (PLL) circuit timing

phase-locked loop characteristics using EXTCLK or on-chip crystal oscillator†

| PARAMETER | | MIN | MAX | UNIT |
|---------------------|---|-----|------|--------|
| F _{pllin} | Frequency range, PLL input | 5* | 15* | MHz |
| F _{pllout} | Frequency range, PLL output | 25* | 75* | MHz |
| I _{pll} | PLL current, CV _{DD} supply | | 2* | mA |
| P _{pll} | PLL power, CV _{DD} supply | | 5* | mW |
| PLL _{dc} | PLL output duty cycle at H1 | 45* | 55* | % |
| PLLJ | PLL output jitter, F _{pllout} = 25 MHz | | 400* | ps |
| PLL _{LOCK} | PLL lock time in input cycles | | 1000 | cycles |

* Not production tested

† Duty cycle is defined as $100 \cdot t_1 / (t_1 + t_2) \%$

To ensure clean internal clock references, the minimal low and high pulse durations must be maintained. At high frequencies, this may require a fast rise and fall time as well as a tightly controlled duty cycle. At lower frequencies, these requirements are less restrictive when in x1 and x0.5 modes. The PLL, however, must have an input duty cycle of between 40% and 60% for proper operation.

clock circuit timing

The following table defines the timing parameters for the clock circuit signals.

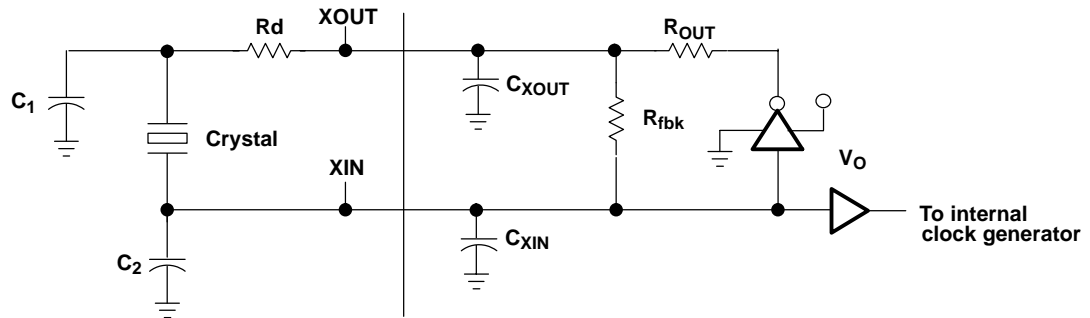
circuit parameters for on-chip crystal oscillator† (see Figure 15)

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|----------------------|-----------|--------------------|------------|
| V_O Oscillator internal supply voltage | | CV_{DD} | | V |
| F_O Fundamental mode frequency range | 1* | | 20* | MHz |
| V_{bias} DC bias point (input threshold) | 40* | 50 | 60* | % V_O |
| R_{fbk} Feedback resistance | 100* | 300 | 500* | k Ω |
| R_{out} Small signal ac output impedance | 250* | 500 | 1000* | Ω |
| V_{xoutac} The ac output voltage with test crystal‡ | | 85 | | % V_O |
| V_{xinac} The ac input voltage with test crystal‡ | | 85 | | % V_O |
| V_{xoutl} $V_{xin} = V_{xinh}$, $I_{xout} = 0$, $F_O=0$ (logic input) | $V_{SS} - 0.1^*$ | | $V_{SS} + 0.3^*$ | V |
| V_{xouth} $V_{xin} = V_{xinl}$, $I_{xout} = 0$, $F_O=0$ (logic input) | $CV_{DD} - 0.3^*$ | | $CV_{DD} + 0.1^*$ | V |
| V_{inl} When used for logic level input, oscillator enabled | -0.3* | | $0.2 \times V_O^*$ | V |
| V_{inh} When used for logic level input, oscillator enabled | $0.8 \times V_O^*$ | | $DV_{DD} + 0.3^*$ | V |
| V_{xinh} When used for logic level input, oscillator disabled | $0.7 \times DV_{DD}$ | | $DV_{DD} + 0.3$ | V |
| C_{xout} XOUT internal load capacitance | 2* | 3 | 5* | pF |
| C_{xin} XIN internal load capacitance | 2* | 3 | 5* | pF |
| $t_{d(XIN-H1)}$ Delay time, XIN to H1 x1 and x0.5 modes | 2 | 5.5 | 8 | ns |
| I_{inl} Input current, feedback enabled, $V_{il} = 0$ | | | 50* | μA |
| I_{inh} Input current, feedback enabled, $V_{il} = V_{ih}$ | | | -50* | μA |

* Not production tested

† This circuit is intended for series resonant fundamental mode operation.

‡ Signal amplitude is dependent on the crystal and load used.



NOTE A: See Table 3 for value of Rd.

Figure 15. On-Chip Oscillator Circuit

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clock circuit timing (continued)

The following tables define the timing requirements and switching characteristics for EXTCLK.

timing requirements for EXTCLK, all modes (see Figure 16 and Figure 17)

| | | | MIN | MAX | UNIT |
|------------------|--|-----------------------------------|-------|------|------|
| $t_{r(EXTCLK)}$ | Rise time, EXTCLK | $F = F_{max}$, x0.5 and x1 modes | | 1* | ns |
| | | $F < F_{max}$ | | 4* | |
| $t_{f(EXTCLK)}$ | Fall time, EXTCLK | $F = F_{max}$, x0.5 and x1 modes | | 1* | ns |
| | | $F < F_{max}$ | | 4* | |
| $t_{w(EXTCLKL)}$ | Pulse duration, EXTCLK low | x5 mode | 21* | | ns |
| | | x1 mode | 6* | | |
| | | x0.5 mode | 4* | | |
| $t_{w(EXTCLKH)}$ | Pulse duration, EXTCLK high | x5 mode | 21* | | ns |
| | | x1 mode | 5* | | |
| | | x0.5 mode | 4* | | |
| $t_{dc(EXTCLK)}$ | Duty cycle, EXTCLK [$t_{w(EXTCLKH)} / t_{c(H)}$] | x5 PLL mode | 40* | 60* | % |
| | | x1 and x0.5 modes, $F = \max$ | 45 | 55 | |
| | | x1 and x0.5 modes, $F = 0$ Hz | 0* | 100* | |
| $t_{c(EXTCLK)}$ | Cycle time, EXTCLK | x5 mode | 66.7* | 200* | ns |
| | | x1 mode | 13.3 | | |
| | | x0.5 mode | 10* | | |
| F_{ext} | Frequency range, $1/t_{c(EXTCLK)}$ | x5 mode | 5* | 15* | MHz |
| | | x1 mode | 0 | 75 | |
| | | x0.5 mode | 0* | 100* | |

* Not production tested

switching characteristics for EXTCLK over recommended operating conditions, all modes (see Figure 16 and Figure 17)

| PARAMETER | | | MIN | TYP | MAX | UNIT |
|-------------------|--|-------------|-------|------------------------|-----|------|
| V_{mid} | Mid-level, used to measure duty cycle | | | $0.5 \times DV_{DD}$ | | V |
| $t_{d(EXTCLK-H)}$ | Delay time, EXTCLK to H1 and H3 | x1 mode | 2* | 4.5 | 7* | ns |
| | | x0.5 mode | 2* | 4.5 | 7* | |
| $t_{r(H)}$ | Rise time, H1 and H3 | | | | 3* | ns |
| $t_{f(H)}$ | Fall time, H1 and H3 | | | | 3* | ns |
| $t_{d(HL-HH)}$ | Delay time, from H1 low to H3 high or from H3 low to H1 high | | -1.5* | | 2* | ns |
| $t_{c(H)}$ | Cycle time, H1 and H3 | x5 PLL mode | | $1/(5 \times f_{ext})$ | | ns |
| | | x1 mode | | $1/f_{ext}$ | | |
| | | x0.5 mode | | $2/f_{ext}$ | | |

* Not production tested



clock circuit timing (continued)

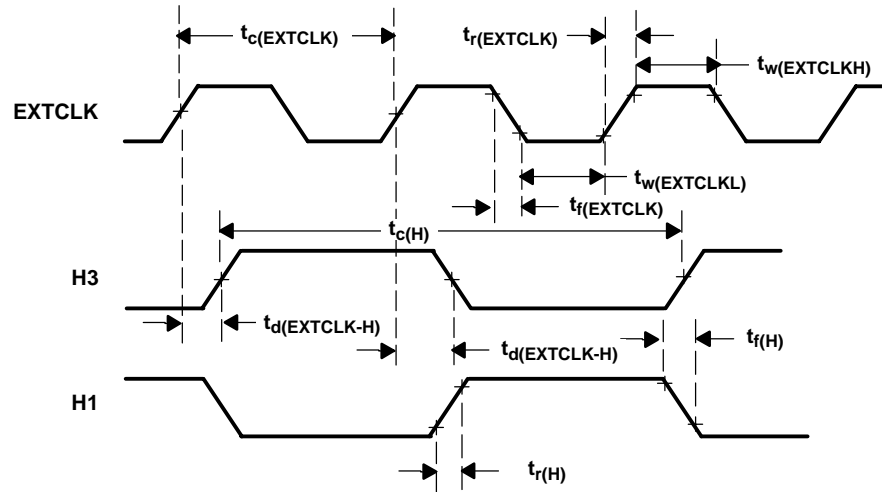
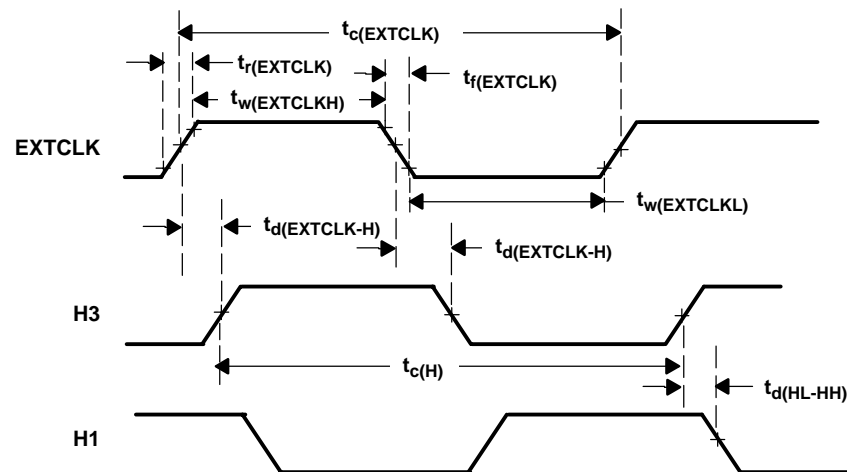


Figure 16. Divide-By-Two Mode



NOTE A: EXTCLK is held low.

Figure 17. Divide-By-One Mode

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memory read/write timing

The following tables define memory read/write timing parameters for $\overline{\text{STRB}}$.

timing requirements for memory read/write† (see Figure 18, Figure 19, and Figure 20)

| | | MIN | MAX | UNIT |
|---------------------------------------|--|--|--------------------------------|------|
| $t_{\text{su}}(\text{D-H1L})\text{R}$ | Setup time, Data before H1 low (read) | 5* | | ns |
| $t_{\text{h}}(\text{H1L-D})\text{R}$ | Hold time, Data after H1 low (read) | -1* | | ns |
| $t_{\text{su}}(\text{RDY-H1H})$ | Setup time, $\overline{\text{RDY}}$ before H1 high | 5 | | ns |
| $t_{\text{h}}(\text{H1H-RDY})$ | Hold time, $\overline{\text{RDY}}$ after H1 high | -1* | | ns |
| $t_{\text{d}}(\text{A-RDY})$ | Delay time, Address valid to $\overline{\text{RDY}}$ | | P - 6*‡ | ns |
| $t_{\text{v}}(\text{A-D})$ | Valid time, Data valid after address PAGE _x , or $\overline{\text{STRB}}$ valid | 0 wait state, $C_{\text{L}} = 30 \text{ pF}$ | 6* | ns |
| | | 1 wait state | $t_{\text{c}}(\text{H}) + 6^*$ | ns |

* Not production tested

† These timings assume a similar loading of 30 pF on all pins.

‡ P = $t_{\text{c}}(\text{H})/2$ (when duty cycle equals 50%).

switching characteristics over recommended operating conditions for memory read/write† (see Figure 18, Figure 19, and Figure 20)

| PARAMETER | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{\text{d}}(\text{H1L-SL})$ | -1* | 3 | ns |
| $t_{\text{d}}(\text{H1L-SH})$ | -1* | 3 | ns |
| $t_{\text{d}}(\text{H1H-RWL})\text{W}$ | -1* | 3 | ns |
| $t_{\text{d}}(\text{H1L-A})$ | -1* | 3 | ns |
| $t_{\text{d}}(\text{H1H-RWH})\text{W}$ | -1* | 3 | ns |
| $t_{\text{d}}(\text{H1H-A})\text{W}$ | -1* | 3* | ns |
| $t_{\text{v}}(\text{H1L-D})\text{W}$ | | 5 | ns |
| $t_{\text{h}}(\text{H1H-D})\text{W}$ | 0* | 5 | ns |

* Not production tested

† These timings assume a similar loading of 30 pF on all pins.

Output load characteristics for high-speed and low-speed (low-noise) output buffers are shown in Figure 18. High-speed buffers are used on A0 - A23, PAGE₀ - PAGE₃, H1, H3, $\overline{\text{STRB}}$, and R/W. All other outputs use the low-speed, (low-noise) output buffer.

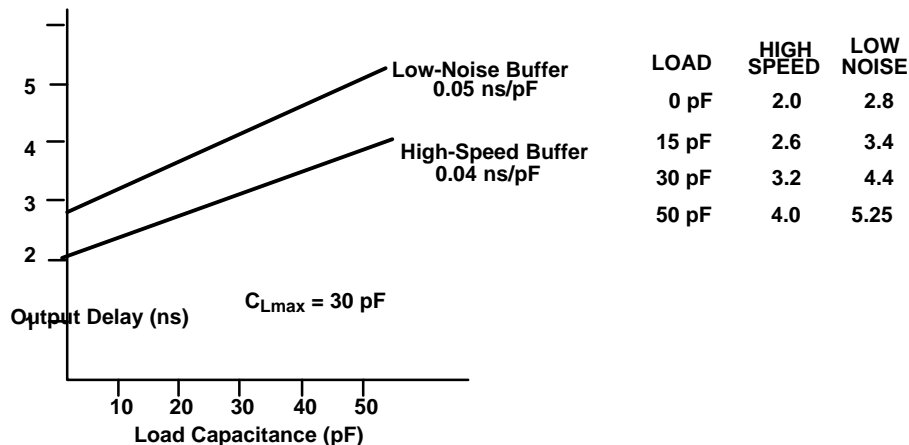
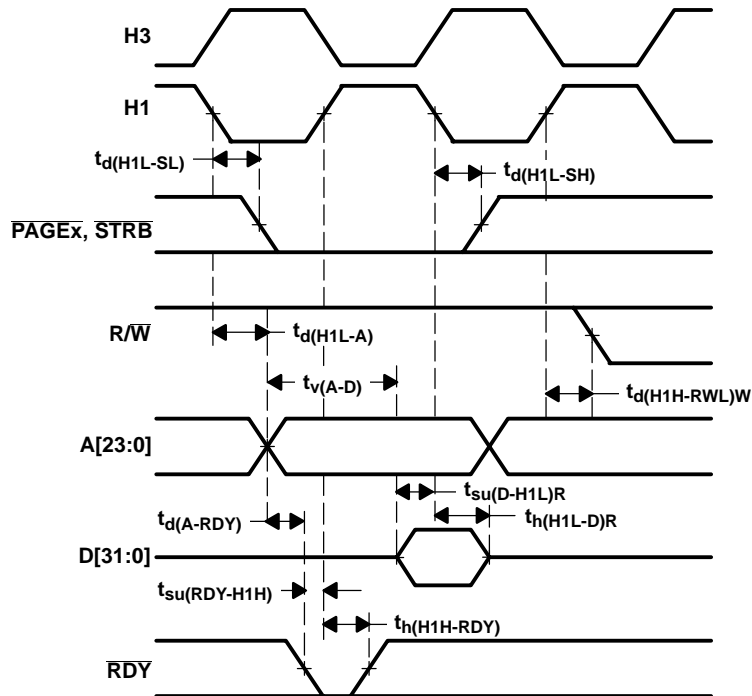


Figure 18. Output Load Characteristics, Buffer Only

memory read/write timing (continued)



NOTE A: STRB remains low during back-to-back read operations.

Figure 19. Timing for Memory ($\text{STRB} = 0$ and $\text{PAGE} = 0$) Read

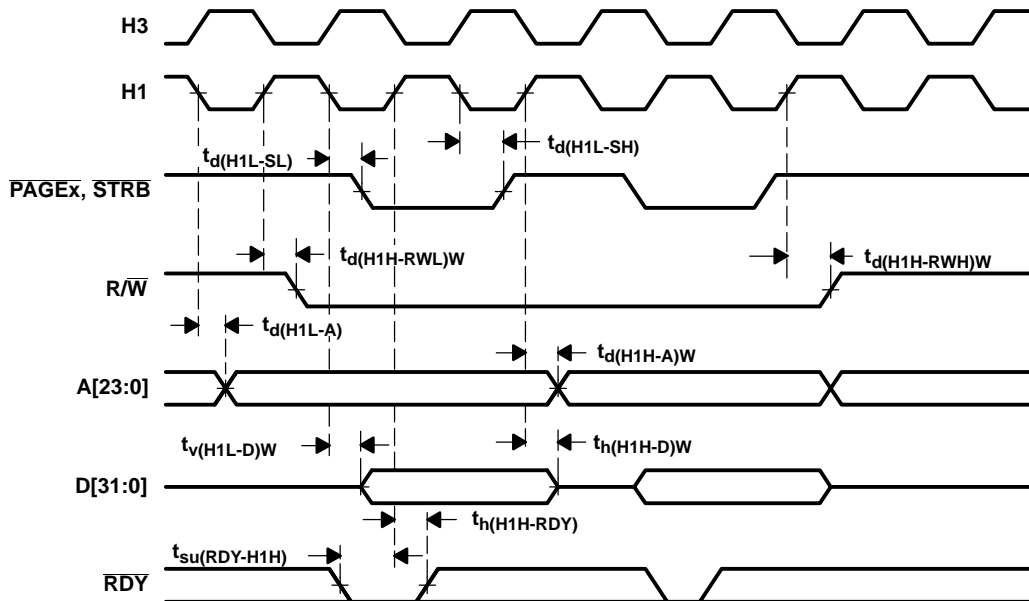


Figure 20. Timing for Memory ($\text{STRB} = 0$ and $\text{PAGE} = 0$) Write

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XF0 and XF1 timing when executing LDFI or LDII

The following tables define the timing parameters for XF0 and XF1 during execution of LDFI or LDII.

timing requirements for XF0 and XF1 when executing LDFI or LDII (see Figure 21)

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_{su}(XF1-H1L)$ Setup time, XF1 before H1 low | 4* | | ns |
| $t_h(H1L-XF1)$ Hold time, XF1 after H1 low | 0* | | ns |

* Not production tested

switching characteristics over recommended operating conditions for XF0 and XF1 when executing LDFI or LDII (see Figure 21)

| PARAMETER | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_d(H3H-XF0L)$ Delay time, H3 high to XF0 low | | 3 | ns |

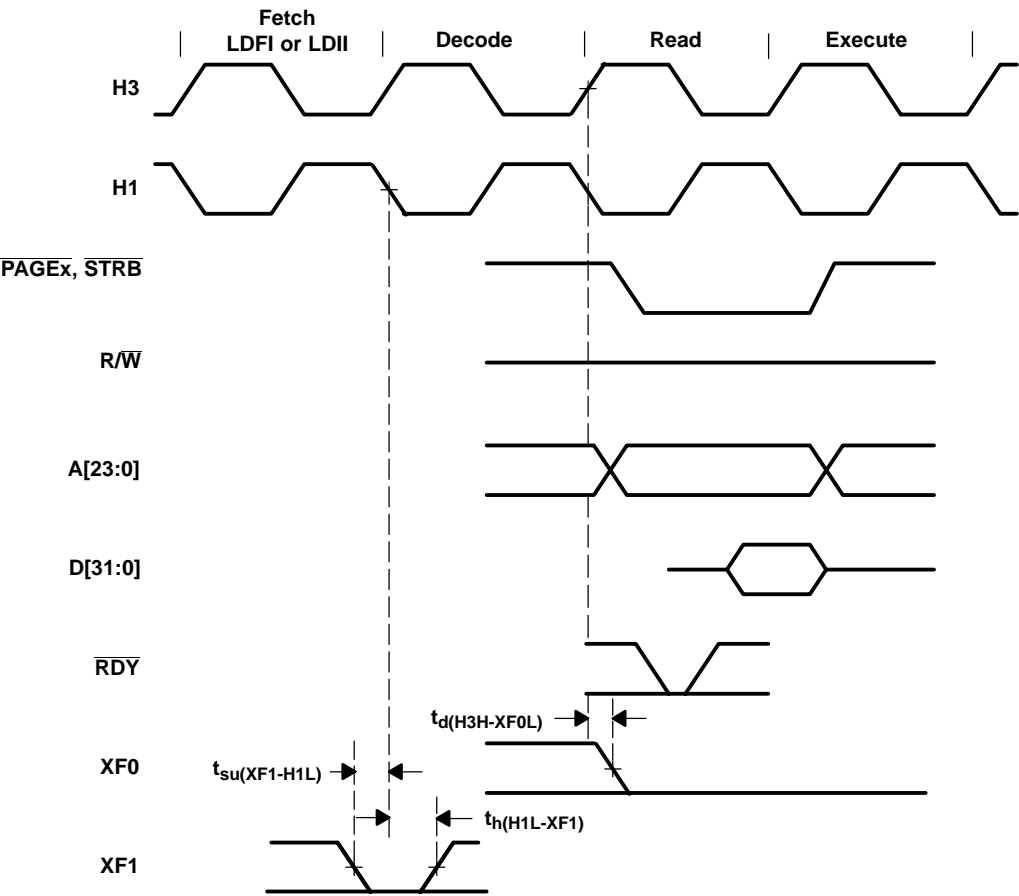


Figure 21. Timing for XF0 and XF1 When Executing LDFI or LDII

XF0 timing when executing STFI and STII†

The following table defines the timing parameters for the XF0 pin during execution of STFI or STII.

switching characteristics over recommended operating conditions for XF0 when executing STFI or STII (see Figure 22)

| PARAMETER | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{d(H3H-XF0H)}$ Delay time, H3 high to XF0 high† | | 3 | ns |

† XF0 is always set high at the beginning of the execute phase of the interlock-store instruction. When no pipeline conflicts occur, the address of the store is also driven at the beginning of the execute phase of the interlock-store instruction. However, if a pipeline conflict prevents the store from executing, the address of the store will not be driven until the store can execute.

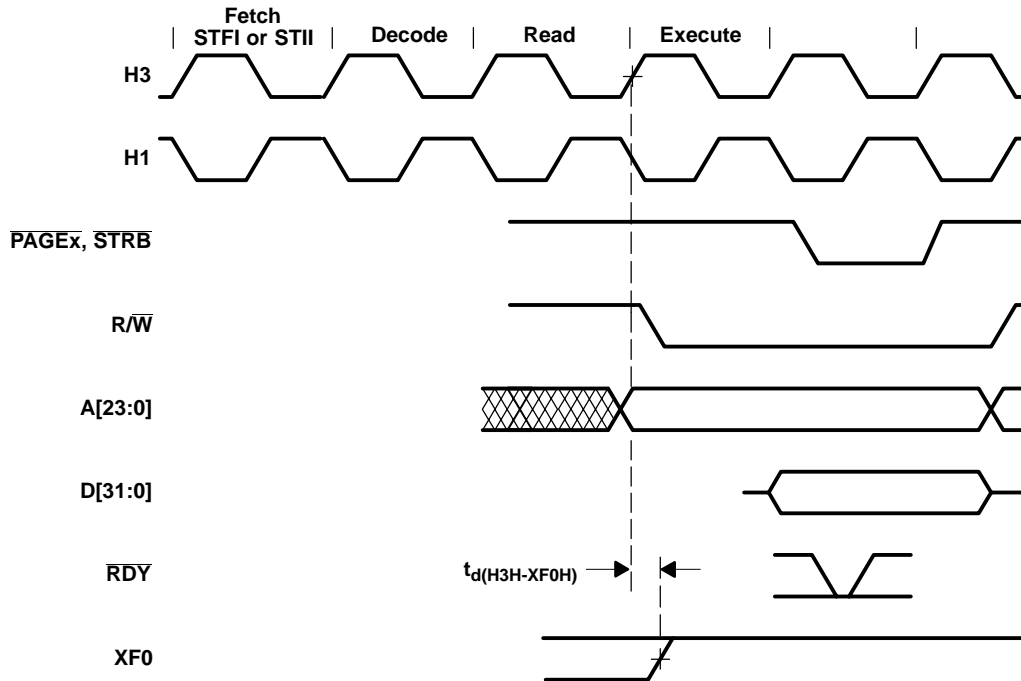


Figure 22. Timing for XF0 When Executing an STFI or STII

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XF0 and XF1 timing when executing SIGI

The following tables define the timing parameters for the XF0 and XF1 pins during execution of SIGI.

timing requirements for XF0 and XF1 when executing SIGI (see Figure 23)

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_{su}(XF1-H1L)$ Setup time, XF1 before H1 low | 4* | | ns |
| $t_h(H1L-XF1)$ Hold time, XF1 after H1 low | 0* | | ns |

* Not production tested

switching characteristics over recommended operating conditions for XF0 and XF1 when executing SIGI (see Figure 23)

| PARAMETER | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_d(H3H-XF0L)$ Delay time, H3 high to XF0 low | | 3 | ns |
| $t_d(H3H-XF0H)$ Delay time, H3 high to XF0 high | | 3 | ns |

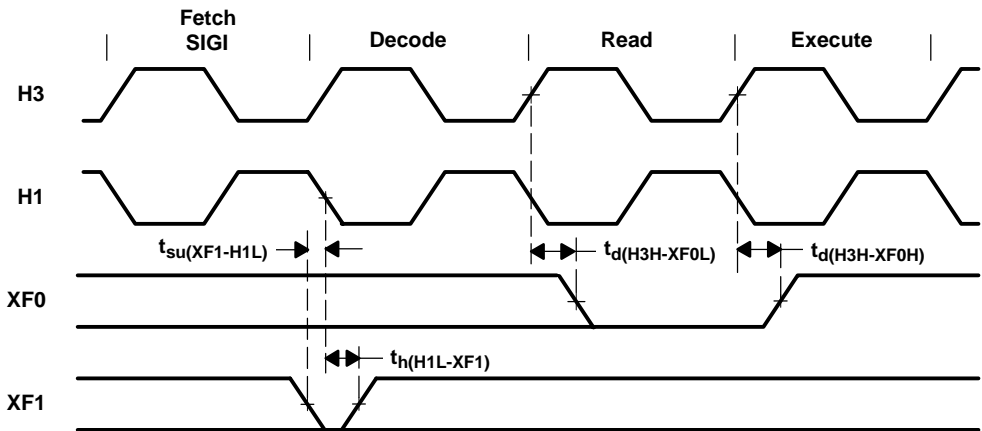


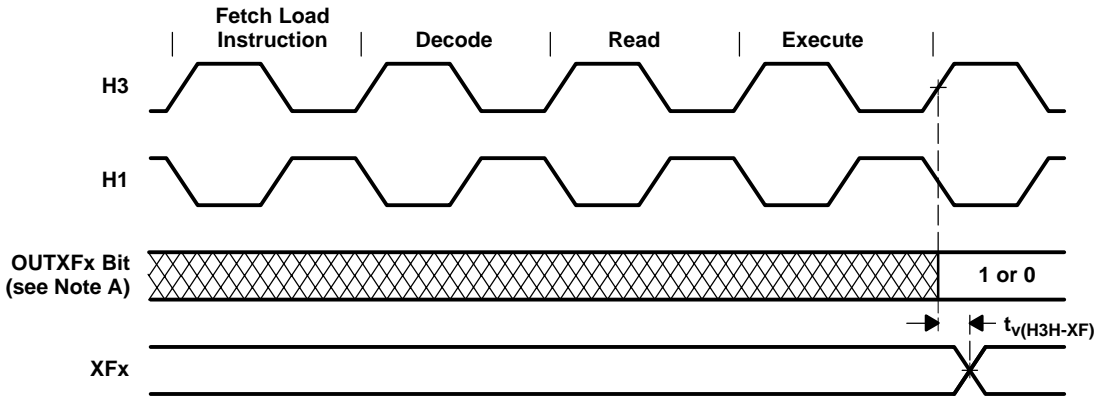
Figure 23. Timing for XF0 and XF1 When Executing SIGI

loading when XF is configured as an output

The following table defines the timing parameter for loading the XF register when the XF_x pin is configured as an output.

switching characteristics over recommended operating conditions for loading the XF register when configured as an output pin (see Figure 24)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------|---|-----|-----|------|
| $t_{v(H3H-XF)}$ | Valid time, XF _x after H3 high | 3 | | ns |



NOTE A: OUTXF_x represents either bit 2 or 6 of the IOF register.

Figure 24. Timing for Loading XF Register When Configured as an Output Pin

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changing XFx from an output to an input

The following table defines the timing parameters for changing the XFx pin from an output pin to an input pin.

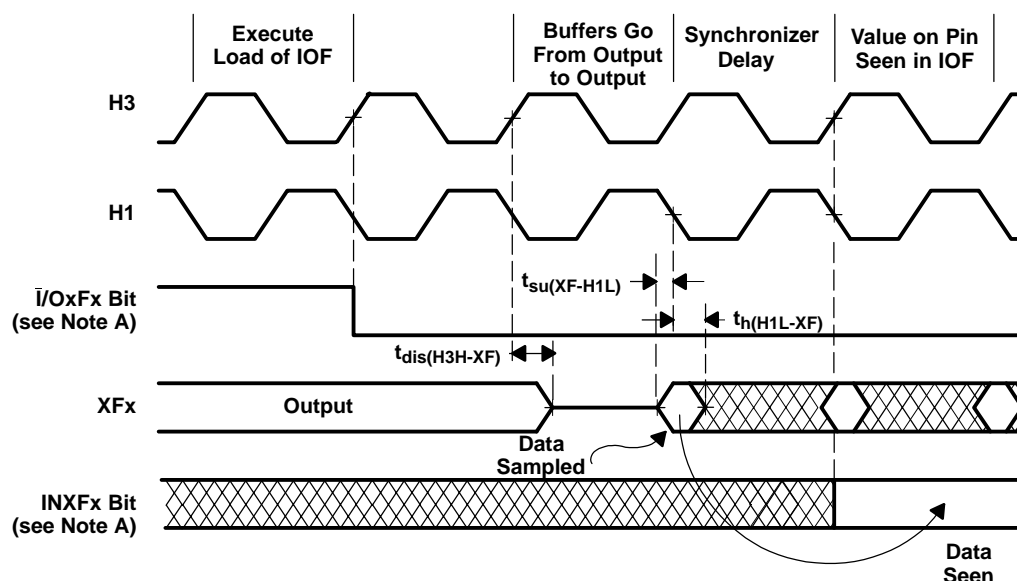
timing requirements for changing XFx from output to input mode (see Figure 25)

| | | MIN | MAX | UNIT |
|------------------|-------------------------------|-----|-----|------|
| $t_{su}(XF-H1L)$ | Setup time, XFx before H1 low | 4 | | ns |
| $t_h(H1L-XF)$ | Hold time, XFx after H1 low | 0 | | ns |

switching characteristics over recommended operating conditions for changing XFx from output to input mode (see Figure 25)

| PARAMETER | MIN | MAX | UNIT |
|-------------------|-----|-----|------|
| $t_{dis}(H3H-XF)$ | | 5* | ns |

* Not production tested



NOTE A: $\bar{I}/OxFx$ represents either bit 1 or bit 5 of the IOF register, and $INXFx$ represents either bit 3 or bit 7 of the IOF register.

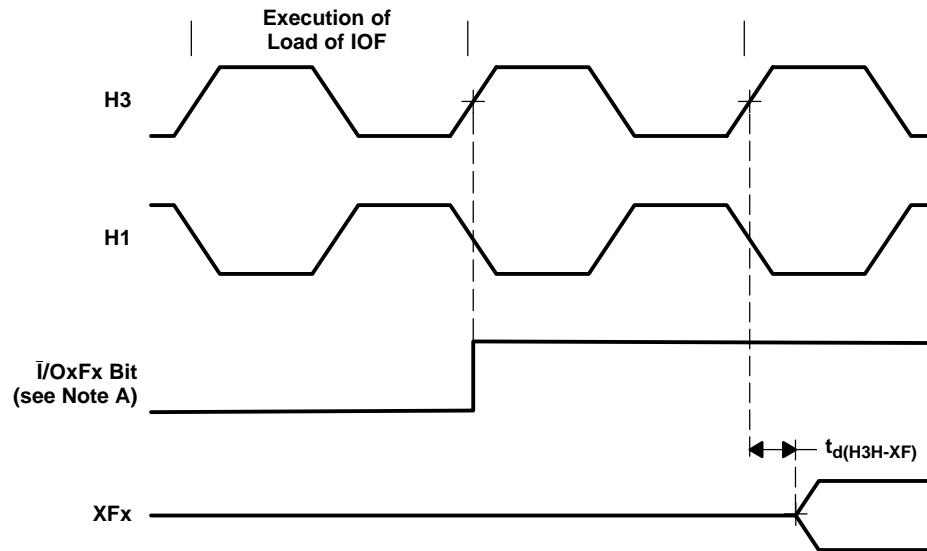
Figure 25. Timing for Changing XFx From Output to Input Mode

changing XFx from an input to an output

The following table defines the timing parameter for changing the XFx pin from an input pin to an output pin.

switching characteristics over recommended operating conditions for changing XFx from input to output mode (see Figure 26)

| PARAMETER | | MIN | MAX | UNIT |
|-----------------|---|-----|-----|------|
| $t_{d(H3H-XF)}$ | Delay time, H3 high to XFx switching from input to output | | 3 | ns |



NOTE A: $\bar{I}/OxFx$ represents either bit 1 or bit 5 of the IOF register.

Figure 26. Timing for Changing XFx From Input to Output Mode

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reset timing

$\overline{\text{RESET}}$ is an asynchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 27 occurs; otherwise, an additional delay of one clock cycle is possible.

The asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.

Resetting the device initializes the bus control register to seven software wait states and therefore results in slow external accesses until these registers are initialized.

$\overline{\text{HOLD}}$ is a synchronous input that can be asserted during reset. It can take nine CPU cycles before $\overline{\text{HOLDA}}$ is granted.

The following table defines the timing parameters for the $\overline{\text{RESET}}$ signal. The numbers shown in Figure 27 correspond with those in the NO. column of the following table.

timing requirements for $\overline{\text{RESET}}$ (see Figure 27)

| | | MIN | MAX | UNIT |
|---|--|-----|---------|------|
| $t_{\text{su}}(\overline{\text{RESET}}\text{-EXTCLKL})$ | Setup time, $\overline{\text{RESET}}$ before EXTCLK low | 5* | P - 7*† | ns |
| $t_{\text{su}}(\overline{\text{RESET}}\text{-H1L})$ | Setup time, $\overline{\text{RESET}}$ high before H1 low and after ten H1 clock cycles | 5 | | ns |

* Not production tested

† P = $t_{\text{c}}(\text{EXTCLK})$

switching characteristics over recommended operating conditions for $\overline{\text{RESET}}$ (see Figure 27)

| PARAMETER | | MIN* | MAX* | UNIT |
|--|--|------|------|------|
| $t_{\text{d}}(\text{EXTCLKH-H1H})$ | Delay time, EXTCLK high to H1 high | 2 | 7 | ns |
| $t_{\text{d}}(\text{EXTCLKH-H1L})$ | Delay time, EXTCLK high to H1 low | 2 | 7 | ns |
| $t_{\text{d}}(\text{EXTCLKH-H3L})$ | Delay time, EXTCLK high to H3 low | 2 | 7 | ns |
| $t_{\text{d}}(\text{EXTCLKH-H3H})$ | Delay time, EXTCLK high to H3 high | 2 | 7 | ns |
| $t_{\text{dis}}(\text{H1H-DZ})$ | Disable time, Data (high impedance) from H1 high† | | 6 | ns |
| $t_{\text{dis}}(\text{H3H-AZ})$ | Disable time, Address (high impedance) from H3 high | | 6 | ns |
| $t_{\text{d}}(\text{H3H-CONTROLH})$ | Delay time, H3 high to control signals high | | 3 | ns |
| $t_{\text{d}}(\text{H1H-RWH})$ | Delay time, H1 high to R/W high | | 3 | ns |
| $t_{\text{d}}(\text{H1H-IACKH})$ | Delay time, H1 high to $\overline{\text{TACK}}$ high | | 3 | ns |
| $t_{\text{dis}}(\overline{\text{RESETL}}\text{-ASYNCH})$ | Disable time, Asynchronous reset signals disabled (high impedance) from $\overline{\text{RESET}}$ low§ | | 6 | ns |

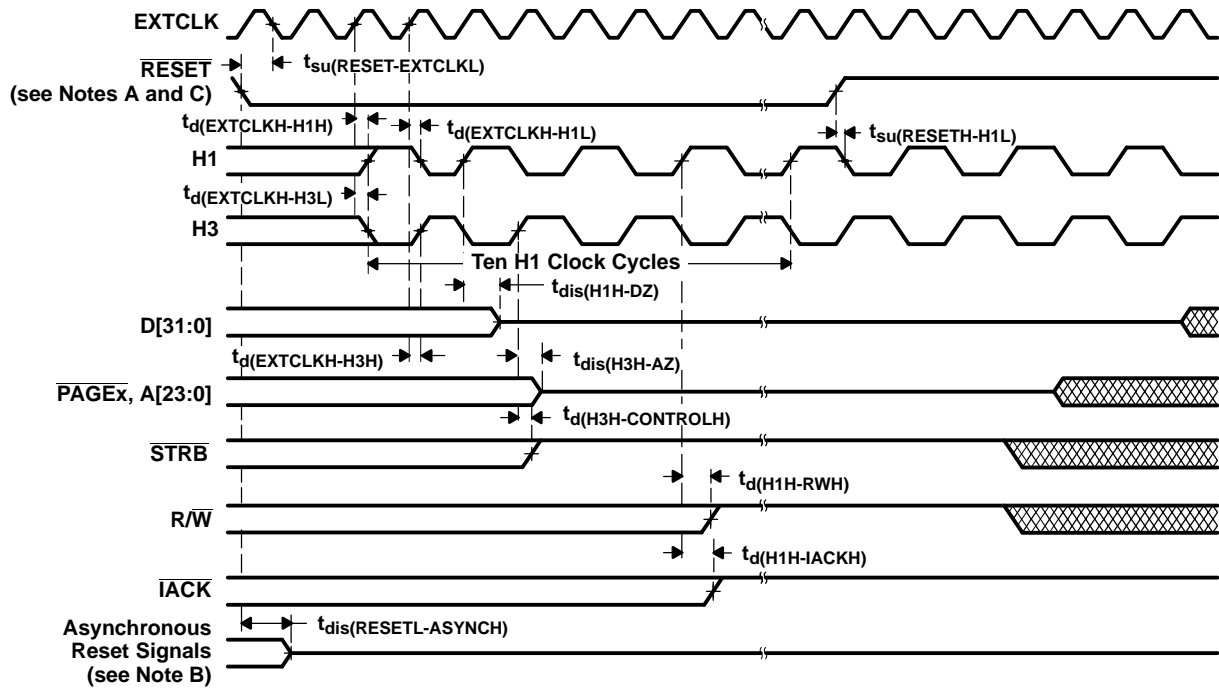
* Not production tested

† High impedance for Dbus is limited to nominal bus keeper $Z_{\text{OUT}} = 15 \text{ k}\Omega$.

§ Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.



reset timing (continued)



- NOTES:
- A. Clock circuit is configured in C31-compatible divide-by-2 mode. If configured for x1 mode, EXTCLK directly drives H3.
 - B. Asynchronous reset signals include XF0/1, CLKX0, DX0, FSX0, CLKR0, DR0, FSR0, and TCLK0/1.
 - C. \overline{RESET} is a synchronous input that can be asserted at any point during a clock cycle. If the specified timings are met, the exact sequence shown occurs; otherwise, an additional delay of one clock cycle is possible.
 - D. In microprocessor mode, the reset vector is fetched twice, with seven software wait states each time. In microcomputer mode, the reset vector is fetched twice, with no software wait states.
 - E. The address and $PAGE3-PAGE0$ outputs are placed in a high-impedance state during reset requiring a nominal 10-22 k Ω pullup. If not, undesirable spurious reads can occur when these outputs are not driven.

Figure 27. RESET Timing

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interrupt response timing

The following table defines the timing parameters for the $\overline{\text{INTx}}$ signals.

timing requirements for $\overline{\text{INT3-INT0}}$ response (see Figure 28)

| | | MIN | NOM | MAX | UNIT |
|--|---|--------------------|------|---------------------|------|
| $t_{\text{su}}(\overline{\text{INT-H1L}})$ | Setup time, $\overline{\text{INT3-INT0}}$ before H1 low | 4* | | | ns |
| $t_{\text{h}}(\text{H1L-INT})$ | Hold time, $\overline{\text{INT3-INT0}}$ after H1 low | | | 0 | ns |
| $t_{\text{w}}(\overline{\text{INT}})$ | Pulse duration, interrupt to ensure only one interrupt | $P + 5^{*\dagger}$ | 1.5P | $2P - 5^{*\dagger}$ | ns |

* Not production tested

$\dagger P = t_{\text{c}}(\text{H})$

The interrupt ($\overline{\text{INTx}}$) pins are synchronized inputs that can be asserted at any time during a clock cycle. The TMS320C3x interrupts are selectable as level- or edge-sensitive. Interrupts are detected on the falling edge of H1. Therefore, interrupts must be set up and held to the falling edge of the internal H1 for proper detection. The CPU and DMA respond to detected interrupts on instruction-fetch boundaries only.

For the processor to recognize only one interrupt when level mode is selected, an interrupt pulse must be set up and held such that a logic-low condition occurs for:

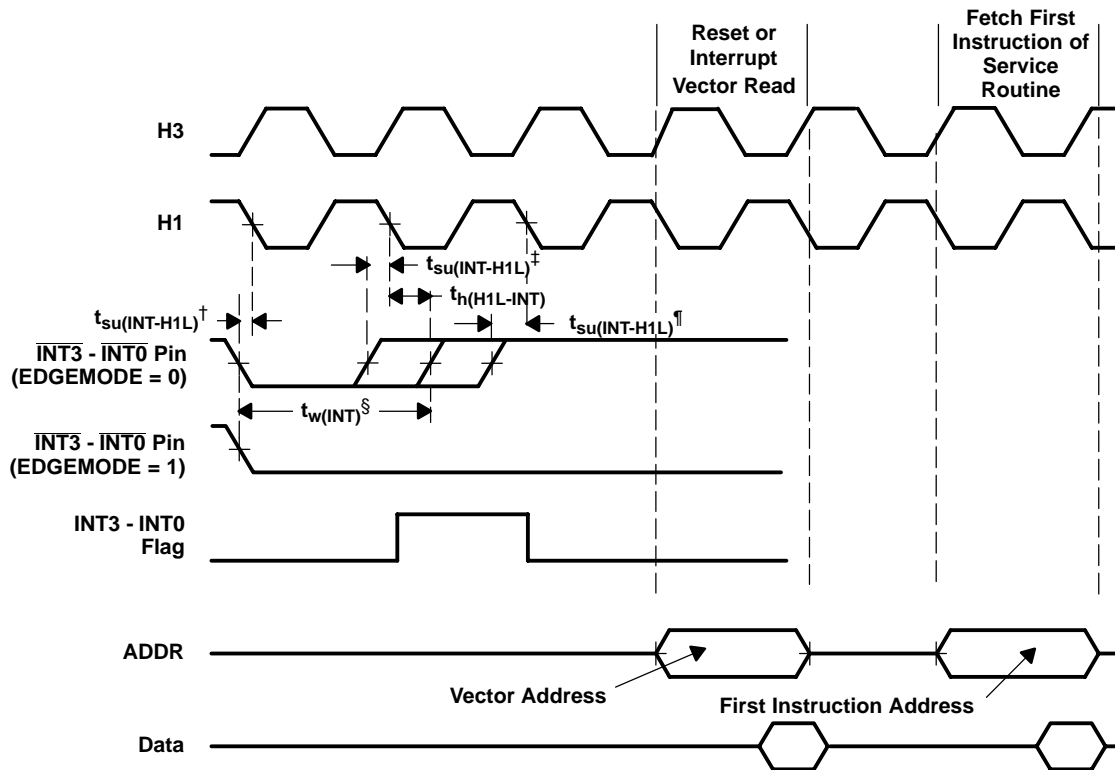
- A minimum of one H1 falling edge
- No more than two H1 falling edges
- Interrupt sources whose edges cannot be specified to meet the H1 falling edge setup and hold times must be further restricted in pulse width as defined by $t_{\text{w}}(\overline{\text{INT}})$ (parameter 51) in the table above.

When $\text{EDGEMODE}=1$, the falling edge of the $\overline{\text{INT0-INT3}}$ pins are detected using synchronous logic (see Figure 7). The pulse low and high time should be two CPU clocks or greater.

The TMS320C3x can set the interrupt flag from the same source as quickly as two H1 clock cycles after it has been cleared.

If the specified timings are met, the exact sequence shown in Figure 28 occurs; otherwise, an additional delay of one clock cycle is possible.

interrupt response timing (continued)



[†] Falling edge of H1 just detects \overline{INTx} falling edge.

[‡] Falling edge of H1 detects second \overline{INTx} low, however flag clear takes precedence.

[§] Nominal width.

[¶] Falling edge of H1 misses previous \overline{INTx} low as \overline{INTx} rises.

Figure 28. $\overline{INT3}$ - $\overline{INT0}$ Response Timing

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interrupt-acknowledge timing

The $\overline{\text{IACK}}$ output goes active on the first half-cycle (H1 rising) of the decode phase of the IACK instruction and goes inactive at the first half-cycle (H1 rising) of the read phase of the IACK instruction.

The following table defines the timing parameters for the $\overline{\text{IACK}}$ signal. The numbers shown in Figure 29 correspond with those in the NO. column of the table below.

NOTE: The IACK instruction can be executed at anytime to signal an event. It is most often used within an interrupt routine to signal which interrupt has occurred.

switching characteristics over recommended operating conditions for $\overline{\text{IACK}}$ (see Figure 29)

| PARAMETER | | MIN | MAX | UNIT |
|--------------------|--|-----|-----|------|
| $t_{d(H1H-IACKL)}$ | Delay time, H1 high to $\overline{\text{IACK}}$ low | -1* | 3 | ns |
| $t_{d(H1H-IACKH)}$ | Delay time, H1 high to $\overline{\text{IACK}}$ high | -1* | 3 | ns |

* Not production tested

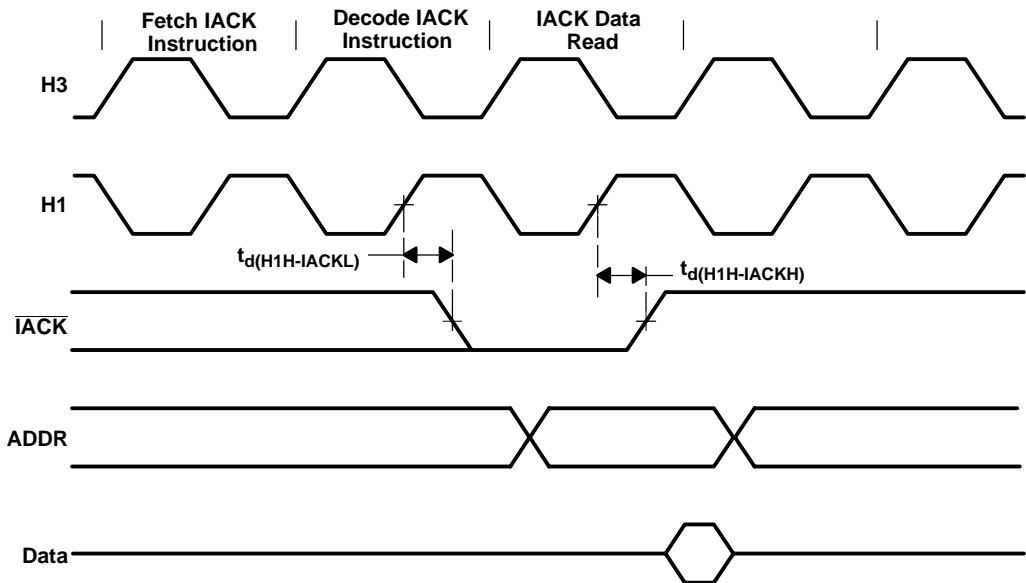


Figure 29. Interrupt Acknowledge ($\overline{\text{IACK}}$) Timing

serial-port timing parameters

The following tables define the timing parameters for the serial port.

timing requirements (see Figure 30 and Figure 31)

| | | MIN | MAX | UNIT |
|---------------------|---|------------|---|------|
| $t_{c(SCK)}$ | Cycle time, CLKX/R | CLKX/R ext | $t_{c(H)} \times 2.6^*$ | ns |
| | | CLKX/R int | $t_{c(H)} \times 4^{*\dagger}$ $t_{c(H)} \times 2^{16^*}$ | |
| $t_{w(SCK)}$ | Pulse duration, CLKX/R high/low | CLKX/R ext | $t_{c(H)} + 5$ | ns |
| | | CLKX/R int | $[t_{c(SCK)}/2] - 4^*$ $[t_{c(SCK)}/2] + 4^*$ | |
| $t_r(SCK)$ | Rise time, CLKX/R | | 3^* | ns |
| $t_f(SCK)$ | Fall time, CLKX/R | | 3^* | ns |
| $t_{su(DR-CLKRL)}$ | Setup time, DR before CLKR low | CLKR ext | 4^* | ns |
| | | CLKR int | 5^* | |
| $t_h(CLKRL-DR)$ | Hold time, DR after CLKR low | CLKR ext | 3^* | ns |
| | | CLKR int | 0^* | |
| $t_{su(FSR-CLKRL)}$ | Setup time, FSR before CLKR low | CLKR ext | 4^* | ns |
| | | CLKR int | 5^* | |
| $t_h(SCKL-FS)$ | Hold time, FSX/R input after CLKX/R low | CLKX/R ext | 3^* | ns |
| | | CLKX/R int | 0^* | |
| $t_{su(FSX-CLKX)}$ | Setup time, external FSX before CLKX | CLKX ext | $-[t_{c(H)} - 6]$ $[t_{c(SCK)}/2] - 6^*$ | ns |
| | | CLKX int | $-[t_{c(H)} - 10]^*$ $t_{c(SCK)}/2^*$ | |

* Not production tested

† A cycle time of $t_{c(H)} \times 2$ is possible when the device is operated at lower CPU frequencies. See the *TMS320VC33 Silicon Update* (literature number SPRZ176) for further details.

switching characteristics over recommended operating conditions (see Figure 30 and Figure 31)

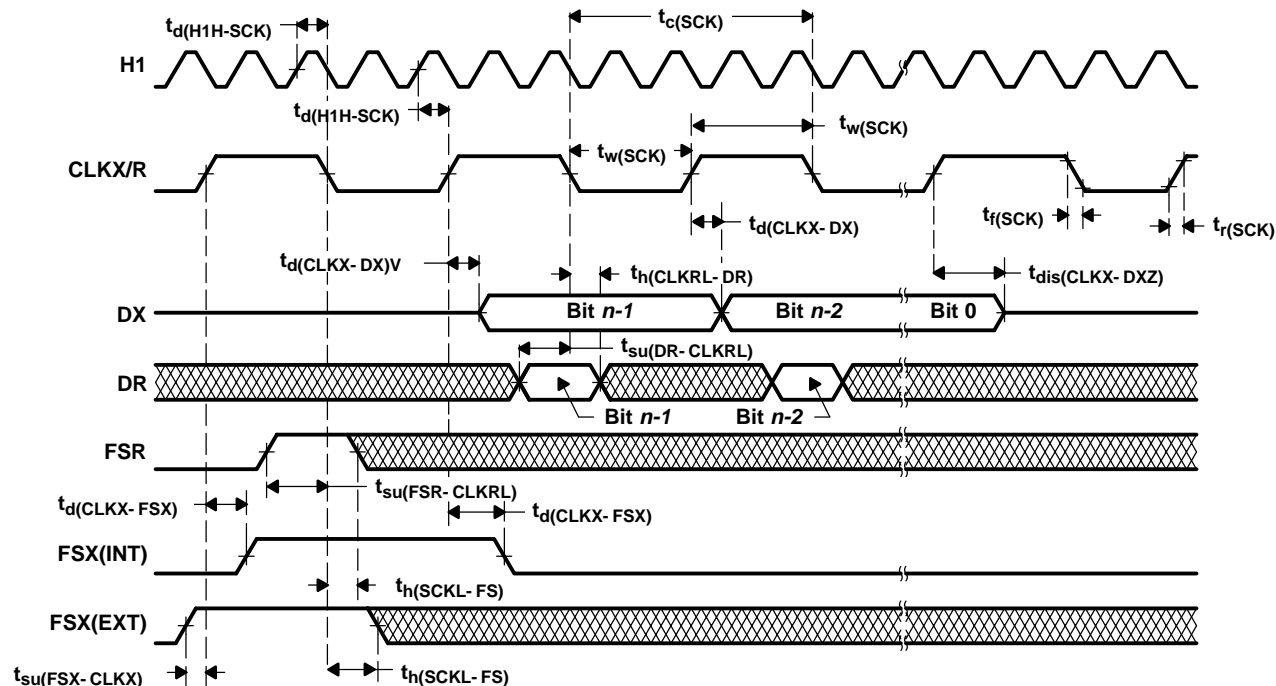
| PARAMETER | | MIN | MAX | UNIT |
|---------------------|--|----------|-------|------|
| $t_{d(H1H-SCK)}$ | Delay time, H1 high to internal CLKX/R | | 4^* | ns |
| $t_{d(CLKX-DX)}$ | Delay time, CLKX to DX valid | CLKX ext | 6 | ns |
| | | CLKX int | 5^* | |
| $t_{d(CLKX-FSX)}$ | Delay time, CLKX to internal FSX high/low | CLKX ext | 5 | ns |
| | | CLKX int | 4^* | |
| $t_{d(CLKX-DX)V}$ | Delay time, CLKX to first DX bit, FSX precedes CLKX high | CLKX ext | 4 | ns |
| | | CLKX int | 5^* | |
| $t_{d(FSX-DX)V}$ | Delay time, FSX to first DX bit, CLKX precedes FSX | | 6 | ns |
| $t_{dis(CLKX-DXZ)}$ | Disable time, DX high impedance following last data bit from CLKX high | | 6 | ns |

* Not production tested

data-rate timing modes

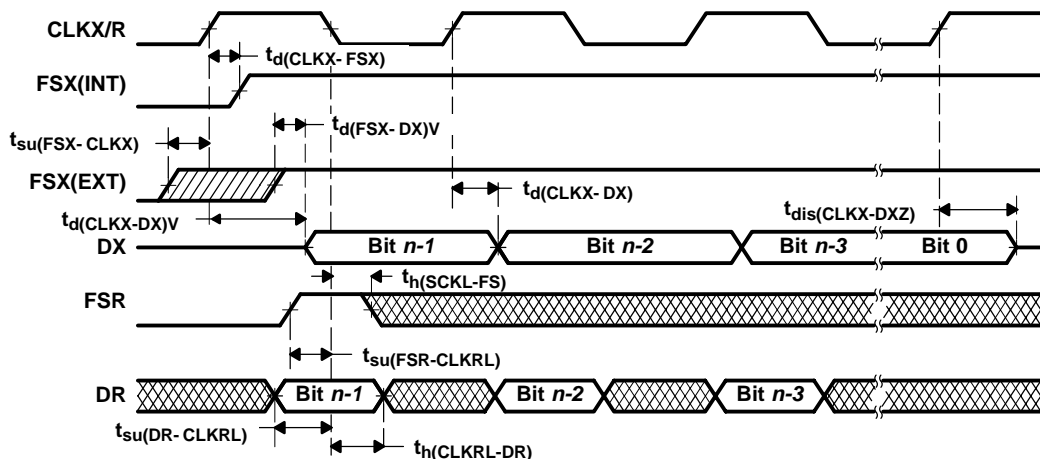
Unless otherwise indicated, the data-rate timings shown in Figure 30 and Figure 31 are valid for all serial-port modes, including handshake. For a functional description of serial-port operation, see the *TMS320C3x User's Guide* (literature number SPRU031).

The serial-port timing parameters are defined in the preceding "serial-port timing parameters" tables. The numbers shown in Figure 30 and Figure 31 correspond with those in the NO. column of each table.



- NOTES: A. Timing diagrams show operations with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.

Figure 30. Fixed Data-Rate Mode Timing



- NOTES: A. Timing diagrams show operation with CLKXP = CLKRP = FSXP = FSRP = 0.
B. Timing diagrams depend on the length of the serial-port word, where n = 8, 16, 24, or 32 bits, respectively.
C. The timings that are not specified expressly for the variable data-rate mode are the same as those that are specified for the fixed data-rate mode.

Figure 31. Variable Data-Rate Mode Timing

HOLD timing

$\overline{\text{HOLD}}$ is a synchronous input that can be asserted at any time during a clock cycle. If the specified timings are met, the exact sequence shown in Figure 32 and Figure 33 occurs; otherwise, an additional delay of one clock cycle is possible.

The table, "timing parameters for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ ", defines the timing parameters for the $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ signals. The numbers shown in Figure 32 and Figure 33 correspond with those in the NO. column of the table.

The NOHOLD bit of the primary-bus control register overrides the $\overline{\text{HOLD}}$ signal. When this bit is set, the device comes out of hold and prevents future hold cycles.

Asserting $\overline{\text{HOLD}}$ prevents the processor from accessing the primary bus. Program execution continues until a read from or a write to the primary bus is requested. In certain circumstances, the first write is pending, thus allowing the processor to continue (internally) until a second external write is encountered.

Figure 32, Figure 33, and the accompanying timings are for a zero wait-state bus configuration. Since $\overline{\text{HOLD}}$ is internally captured by the CPU on the H1 falling edge one cycle before the present cycle is terminated, the minimum $\overline{\text{HOLD}}$ width for any bus configuration is, therefore, WTCNT+3. Also, $\overline{\text{HOLD}}$ should not be deasserted before $\overline{\text{HOLDA}}$ has been active for at least one cycle.

timing requirements for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (see Figure 32 and Figure 33)

| | | MIN | MAX | UNIT |
|--|--|-----------------------------|-----|------|
| $t_{\text{su}}(\overline{\text{HOLD}}-\text{H1L})$ | Setup time, $\overline{\text{HOLD}}$ before H1 low | 3 | | ns |
| $t_{\text{w}}(\overline{\text{HOLD}})$ | Pulse duration, $\overline{\text{HOLD}}$ low | $3t_{\text{c}}(\text{H})^*$ | | ns |

*Not production tested.

switching characteristics over recommended operating conditions for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (see Figure 32 and Figure 33)

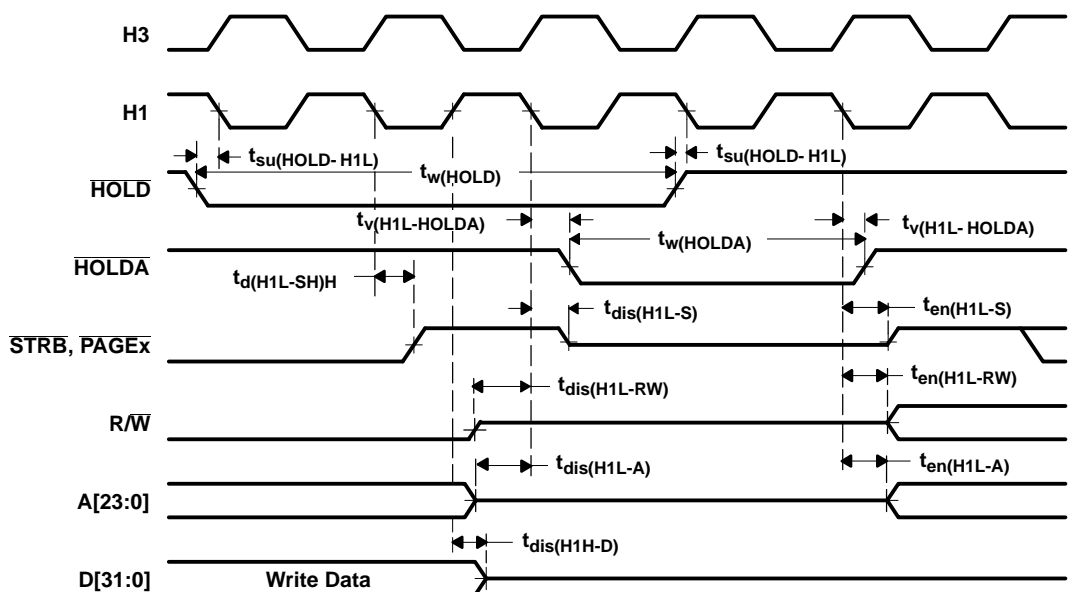
| PARAMETER | | MIN | MAX | UNIT |
|--|--|---------------------------------|-----|------|
| $t_{\text{v}}(\text{H1L}-\overline{\text{HOLDA}})$ | Valid time, $\overline{\text{HOLDA}}$ after H1 low | -1* | 3* | ns |
| $t_{\text{w}}(\overline{\text{HOLDA}})$ | Pulse duration, $\overline{\text{HOLDA}}$ low | $2t_{\text{c}}(\text{H}) - 4^*$ | | ns |
| $t_{\text{d}}(\text{H1L}-\text{SH})\text{H}$ | Delay time, H1 low to $\overline{\text{STRB}}$ high for a $\overline{\text{HOLD}}$ | -1 | 3 | ns |
| $t_{\text{dis}}(\text{H1L}-\text{S})$ | Disable time, $\overline{\text{STRB}}$ to the high-impedance state from H1 low | | 4 | ns |
| $t_{\text{en}}(\text{H1L}-\text{S})$ | Enable time, $\overline{\text{STRB}}$ enabled (active) from H1 low | | 4 | ns |
| $t_{\text{dis}}(\text{H1L}-\text{RW})$ | Disable time, $\text{R}/\overline{\text{W}}$ to the high-impedance state from H1 low | | 5* | ns |
| $t_{\text{en}}(\text{H1L}-\text{RW})$ | Enable time, $\text{R}/\overline{\text{W}}$ enabled (active) from H1 low | | 4 | ns |
| $t_{\text{dis}}(\text{H1L}-\text{A})$ | Disable time, Address to the high-impedance state from H1 low | | 4* | ns |
| $t_{\text{en}}(\text{H1L}-\text{A})$ | Enable time, Address enabled (valid) from H1 low | | 5 | ns |
| $t_{\text{dis}}(\text{H1H}-\text{D})$ | Disable time, Data to the high-impedance state from H1 high | | 4* | ns |

* Not production tested

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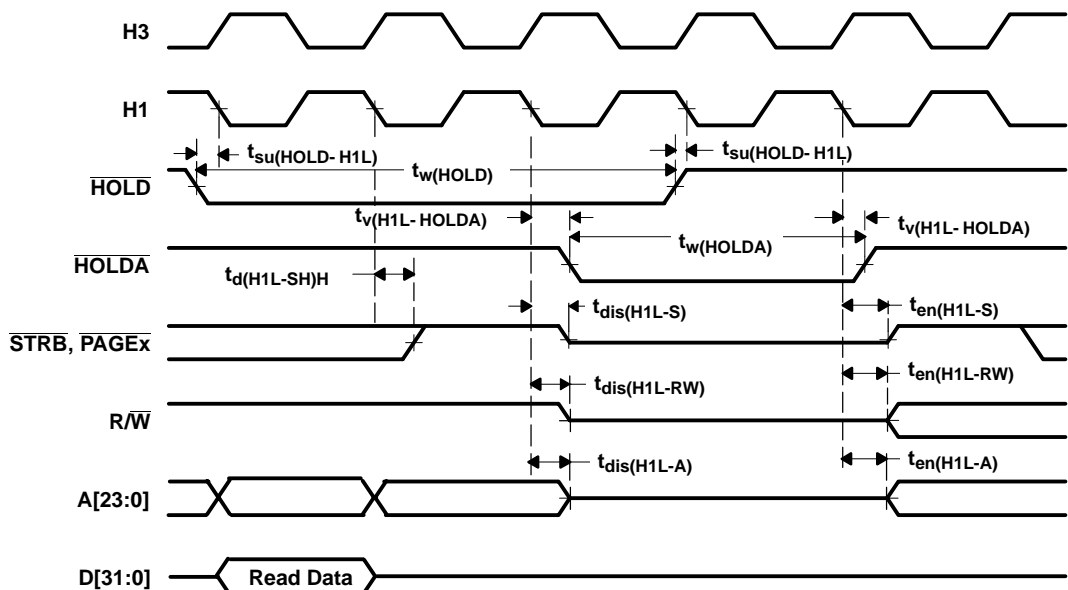
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HOLD timing (continued)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 32. Timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (After Write)



NOTE A: $\overline{\text{HOLDA}}$ goes low in response to $\overline{\text{HOLD}}$ going low and continues to remain low until one H1 cycle after $\overline{\text{HOLD}}$ goes back high.

Figure 33. Timing for $\overline{\text{HOLD}}/\overline{\text{HOLDA}}$ (After Read)

general-purpose I/O timing

Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The contents of the internal control registers associated with each peripheral define the modes for these pins.

peripheral pin I/O timing

The following table shows the timing parameters for changing the peripheral pin from a general-purpose output pin to a general-purpose input pin and vice versa.

timing requirements for peripheral pin general-purpose I/O (see Note 1, Figure 34, and Figure 35)

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{su}(GPIO-H1L)$ Setup time, general-purpose input before H1 low | 3* | | ns |
| $t_h(H1L-GPIO)$ Hold time, general-purpose input after H1 low | 0* | | ns |

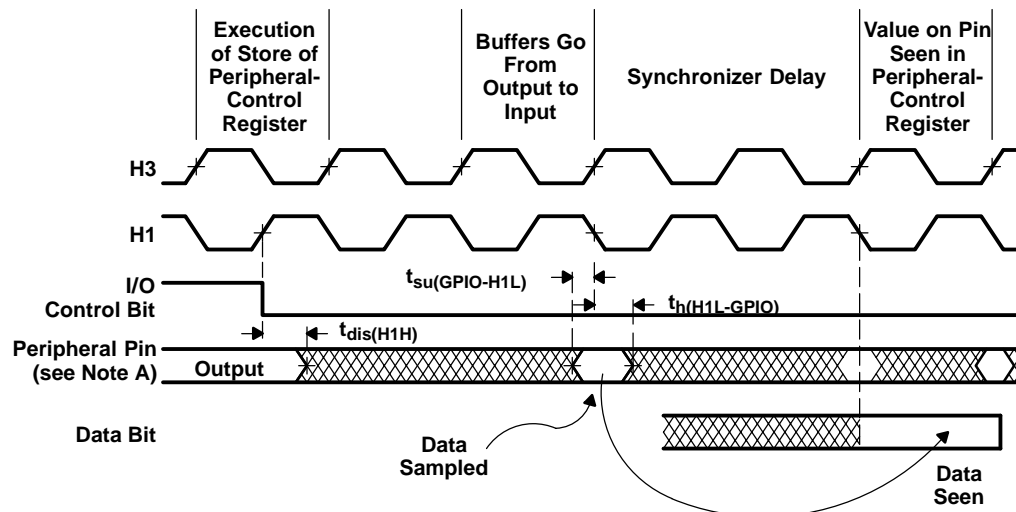
* Not production tested

NOTE 1: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.

switching characteristics over recommended operating conditions for peripheral pin general-purpose I/O (see Note 1, Figure 34, and Figure 35)

| PARAMETER | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_d(H1H-GPIO)$ Delay time, H1 high to general-purpose output | | 4 | ns |
| $t_{dis}(H1H)$ Disable time, general-purpose output from H1 high | | 5 | ns |

NOTE 1: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1. The modes of these pins are defined by the contents of internal-control registers associated with each peripheral.



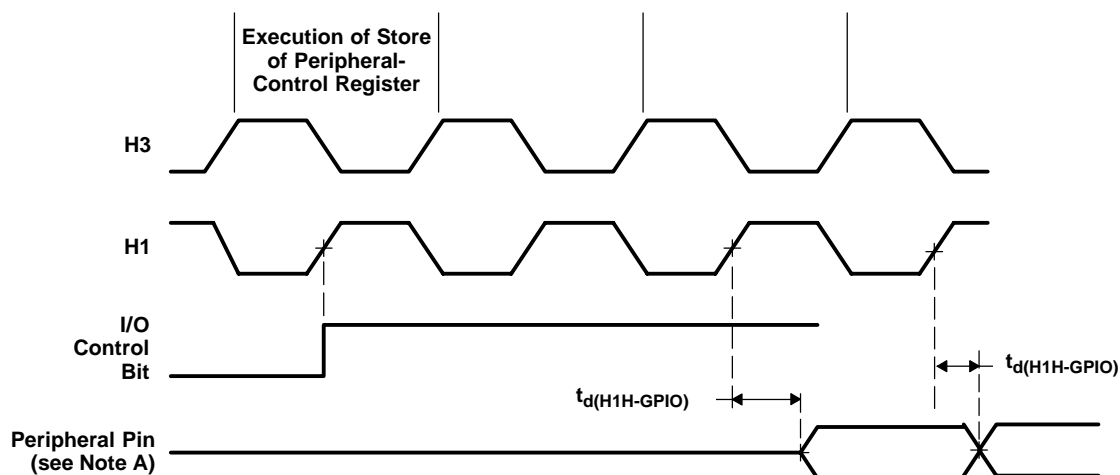
NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 34. Change of Peripheral Pin From General-Purpose Output to Input Mode Timing

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peripheral pin I/O timing (continued)



NOTE A: Peripheral pins include CLKX0, CLKR0, DX0, DR0, FSX0, FSR0, and TCLK0/1.

Figure 35. Change of Peripheral Pin From General-Purpose Input to Output Mode Timing

timer pin timing

Valid logic-level periods and polarity are specified by the contents of the internal control registers. The following tables define the timing parameters for the timer pin.

timing requirements for timer pin (see Figure 36 and Figure 37)

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| $t_{su}(TCLK-H1L)^{\dagger}$ Setup time, TCLK external before H1 low | 3* | | ns |
| $t_{h}(H1L-TCLK)^{\dagger}$ Hold time, TCLK external after H1 low | 0 | | ns |

* Not production tested

\dagger These requirements are applicable for a synchronous input clock.

switching characteristics over recommended operating conditions for timer pin (see Figure 36 and Figure 37)

| PARAMETER | MIN | MAX | UNIT |
|--|----------|--|------|
| $t_{d}(H1H-TCLK)$ Delay time, H1 high to TCLK internal valid | | 3 | ns |
| $t_{c}(TCLK)^{\ddagger}$ Cycle time, TCLK | TCLK ext | $t_{c(H)} \times 2.6^*$ | ns |
| | TCLK int | $t_{c(H)} \times 2^*$ $t_{c(H)} \times 2^{32^*}$ | |
| $t_{w}(TCLK)^{\ddagger}$ Pulse duration, TCLK | TCLK ext | $t_{c(H)} + 5^*$ | ns |
| | TCLK int | $[t_{c}(TCLK)/2] - 4^*$ $[t_{c}(TCLK)/2] + 4^*$ | |

* Not production tested

\ddagger These parameters are applicable for an asynchronous input clock.

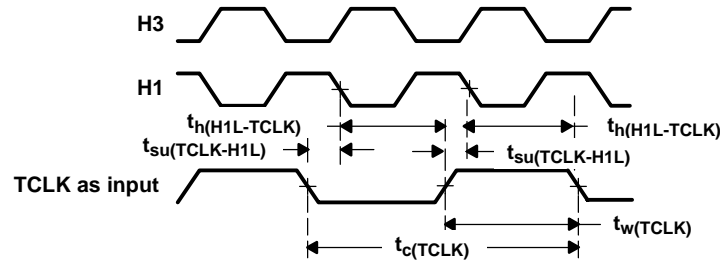


Figure 36. Timer Pin Timing, Input

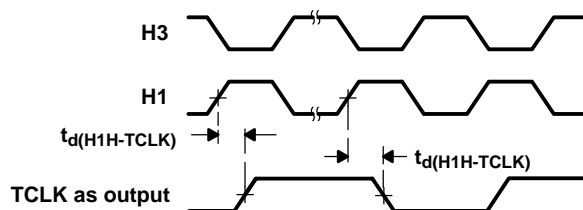


Figure 37. Timer Pin Timing, Output

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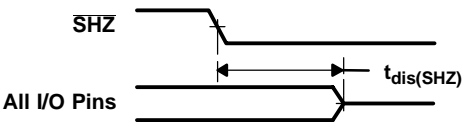
SHZ pin timing

The following table defines the timing parameter for the SHZ pin.

switching characteristics over recommended operating conditions for SHZ (see Figure 38)

| PARAMETER | MIN | MAX | UNIT |
|---|-----|-----|------|
| t _{dis} (SHZ) Disable time, SHZ low to all outputs, I/O pins disabled (high impedance) | 0* | 8* | ns |

* Not production tested



NOTE A: Enabling SHZ destroys SM/SMJ320VC33 register and memory contents. Assert SHZ = 1 and reset the SM/SMJ320VC33 to restore it to a known condition.

Figure 38. Timing for SHZ

test access port timing

The following table defines the timing parameter for the test access port.

timing for test access port (see Figure 39)

| | MIN | MAX | UNIT |
|---|-----|-----|------|
| t _{su} (TMS-TCKH) Setup time, TMS/TDI to TCK high | 5* | | ns |
| t _h (TCKH-TMS) Hold time, TMS/TDI from TCK high | 5* | | ns |
| t _d (TCKL-TDOV) Delay time, TCK low to TDO valid | 0* | 10* | ns |
| t _r (TCK) Rise time, TCK | | 3* | ns |
| t _f (TCK) Fall time, TCK | | 3* | ns |

* Not production tested

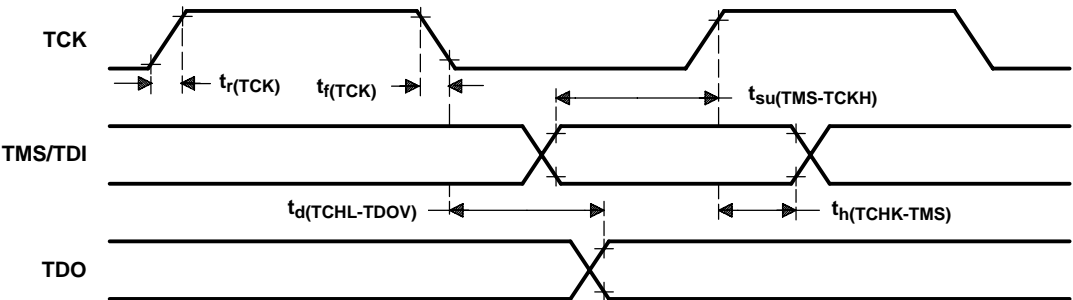
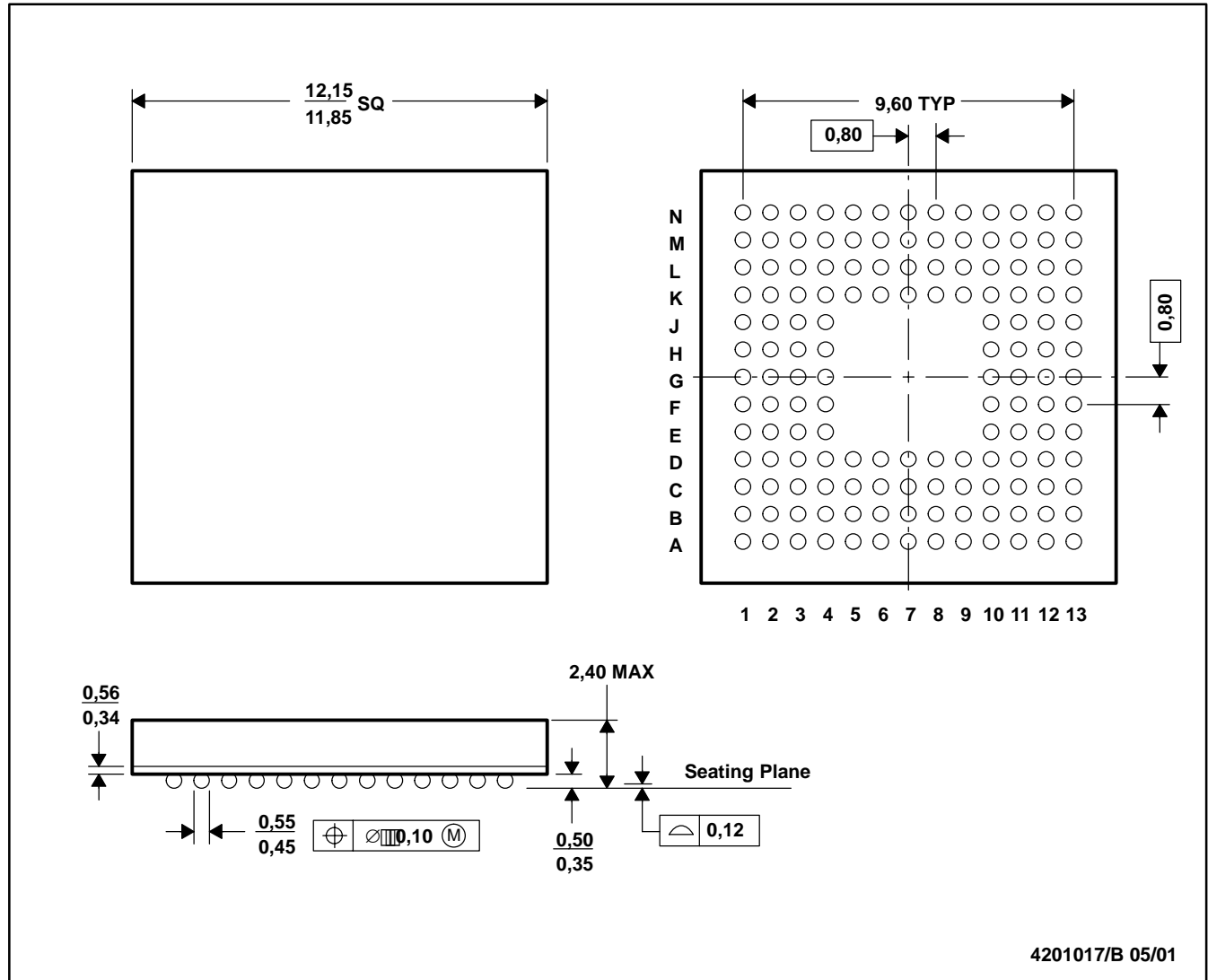


Figure 39. IEEE-1149.1 Test Access Port Timings

MECHANICAL DATA

GNM (S-CBGA-N144)

CERAMIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.

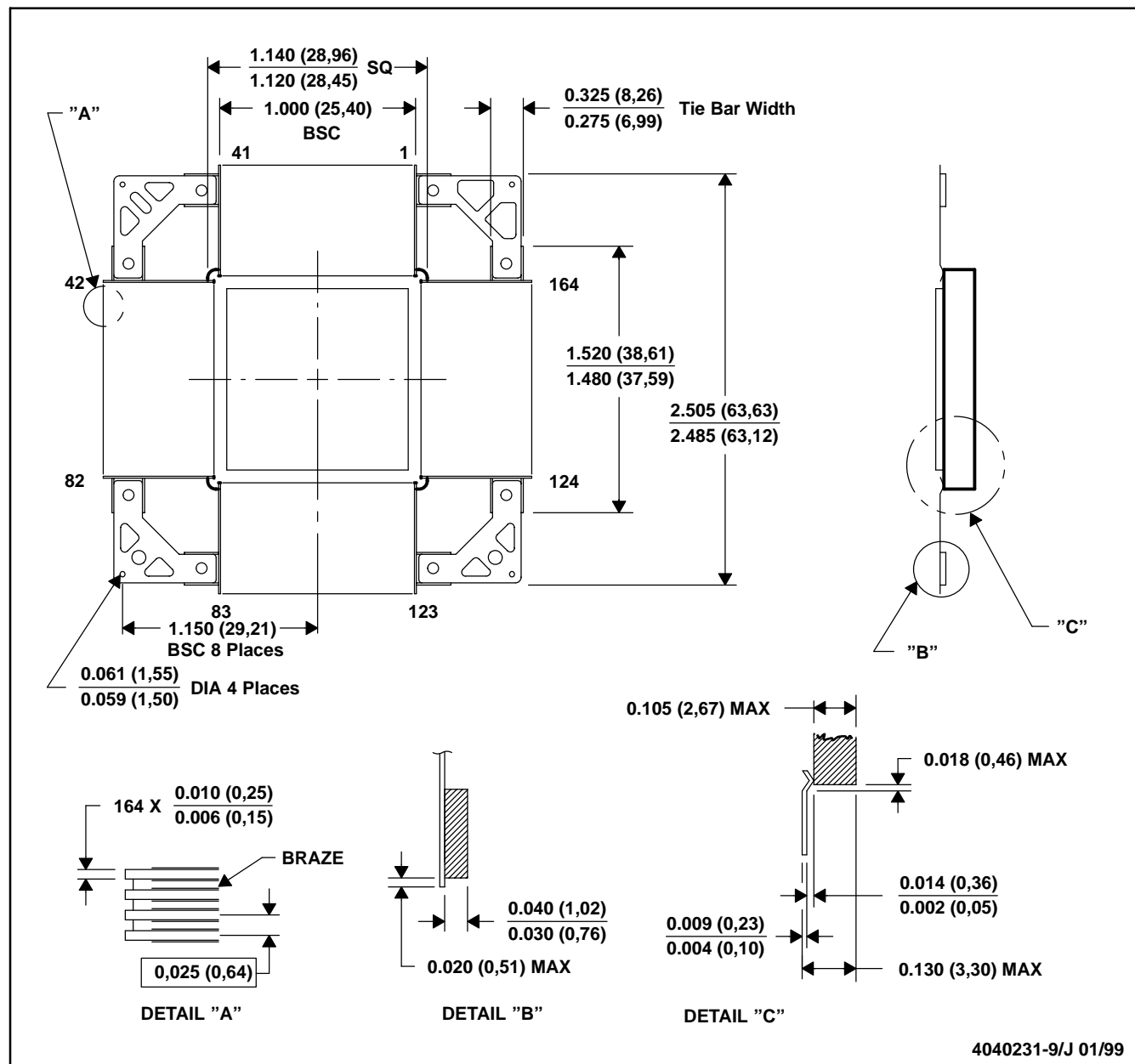
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MECHANICAL DATA

HFG (S-CQFP-F164)

CERAMIC QUAD FLATPACK WITH NCTB



- NOTES:
- C. All linear dimensions are in inches (millimeters).
 - D. This drawing is subject to change without notice.
 - E. Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier
 - F. This package is hermetically sealed with a metal lid.
 - G. The leads are gold-plated and can be solder-dipped.
 - H. Leads not shown for clarity purposes
 - I. Falls within JEDEC MO-113AA (REV D)

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|-------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-0053901QYA | ACTIVE | CFP | HFG | 164 | 1 | None | Call TI | Level-NC-NC-NC |
| 5962-0053901QYC | ACTIVE | CFP | HFG | 164 | 1 | None | Call TI | Level-NC-NC-NC |
| 5962-0053902QYA | ACTIVE | CFP | HFG | 164 | 1 | None | Call TI | Level-NC-NC-NC |
| 5962-0053902QYC | ACTIVE | CFP | HFG | 164 | 4 | None | Call TI | Level-NC-NC-NC |
| SM320VC33GNMM150 | ACTIVE | CBGA | GNM | 144 | 1 | None | Call TI | Level-1-235C-UNLIM |
| SMJ320VC33HFGM150 | ACTIVE | CFP | HFG | 164 | 1 | None | Call TI | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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