8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89980 Series

MB89983/P985/PV980

■ DESCRIPTION

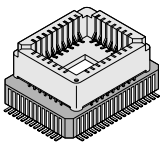
The MB89980 series is a line of the general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as an LCD controller/driver, an A/D converter, timers, remote control transmission output, buzzer output, PWM timers, and external interrupts.

■ FEATURES

- F²MC-8L family CPU core
- Dual-clock control system
- Maximum memory size: 8-Kbyte ROM, 256-byte RAM (max.)
- Minimum execution time: 0.95 μs/4.2 MHz
- I/O ports: max. 47 channels (max. 13 high-current type)
- 21-bit time-base counter
- 8/16-bit timer/counter: 8bit x 2 channels or 16-bit x 1 channels
- External interrupts (wake-up function): Four channels with edge selection plus eight level-interrupt channels
- 8-bit A/D converter: 4 channels
- 8-bit PWM timers: 2 channels
- Watch prescaler (15 bits)
- LCD controller/driver: 14 segments × 4 commons (max. 56 pixels)
- LCD driving reference voltage generator
- Remote control transmission output
- Buzzer output
- Power-on reset function (option)
- Low-power consumption modes (stop, sleep, and watch mode)
- CMOS technology

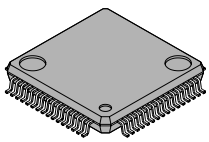
■ PACKAGE

64-pin Ceramic MQFP



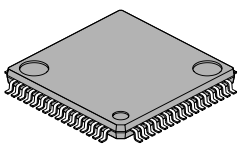
(MQP-64C-P01)

64-pin Plastic LQFP



(FPT-64P-M03)

64-pin Plastic QFP



(FPT-64P-M09)

■ PRODUCT LINEUP

Part number / Parameter	MB89983	MB89P985	MB89PV980
Classification	Mass production products (mask ROM products)	One-time PROM product (OTP)	Piggyback/evaluation product (for development)
ROM size	8 K x 8 bits (internal mask ROM)	16K x 8 bits (Internal PROM)	32K x 8 bits (External ROM)
RAM size	256 × 8 bits	512 x 8 bits	
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8,16 bits Minimum execution time: 0.95 µs/4.2 MHz Interrupt processing time: 9 µs/4.2 MHz		
Ports	General-purpose I/O ports (N-ch open-drain): 8 (4 ports also serve as peripherals, 3 ports are heavy-current drive type.) Output-only ports (N-ch open-drain): 20 (4 ports also serve as A/D, 14 ports serve as segment pins and 2 ports serve as common pins, 10 ports are heavy-current drive type .) General-purpose I/O ports (CMOS): 16 (12 ports also serve as an external interrupt,) Input-only ports (CMOS) 2 (serve with sub-clock pins) Output-only ports (CMOS) 1 (serves as peripherials Total: 47 (max.)		
Timer/counter	8-bit timer operation (toggled output capable, operating clock cycle 1.9 µs to 486 µs) 16-bit timer operation (toggled output capable, operating clock cycle 1.9 µs to 486 µs)		
LCD controller/driver	Common output: 4 (max.) Segment output: 14 (max.) *2 Bias power supply pins: 4 LCD display RAM size: 14 × 4 bits Dividing resistor for LCD driving: Built-in (an external resistor selectability)		
A/D converter	8-bit resolution × 4 channels A/D conversion mode (conversion time 43 µs/4.2 MHz (44 instruction cycles)) Sense mode (conversion time 11.9 µs/4.2 MHz) Continuous activation by an internal timer capable Reference voltage input		
PWM timer 1, PWM timer 2	8 bits × 2 channels 8-bit reload timer operation (toggled output capable, operating clock cycle: 0.95 µs to 124 ms) 8-bit resolution PWM operation (conversion cycle: 243 µs to 32 s)		

(Continued)

(Continued)

Part number / Parameter	MB89983	MB89P985	MB89PV980
External interrupt 1 (wake-up function)	4 independent channels (edge selectability) Rising edge/falling edge selectability Used also for wake-up from stop/sleep mode. (Edge detection is also permitted in stop mode.)		
External interrupt 2	"L" level interrupts × 8 channels		
Buzzer output	1 (7 frequencies are selectable by the software.)		
Remote control transmission output	1 (Pulse width and cycle are software selectable.)		
Standby modes	Subclock mode, sleep mode, stop mode, and watch mode		
Process	CMOS		
Operating voltage*1	2.2 V to 6.0 V	2.7 V to 6.0 V	

*1: Varies with conditions such as the operating frequency. (The operating voltage of the A/D converter is assured separately. See section "■ Electrical Characteristics.")

*2: See section "■ Mask Options."

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89983	MB89P985	MB89PV980
FPT-64P-M09	○	○	×
FPT-64P-M03	○	○	×
MQP-64C-P01	×	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV980, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in the sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

Take particular care on the following points:

- A pull-up resistor is not selectable for P40 to P47 and P60 to P65 if they are used as LCD pins.
- A pull-up resistor is not selectable for P50 to P53 if they are used as analog input.

4. Pull-up resistor

Pull-up resisitors of MB89P985 and MB89PV980 are selected by pull-up control registor (Port 0, 1, 5), but there are no pull-up resistor for Port 2, 4 and 6 in MB89P985 and MB89PV980.

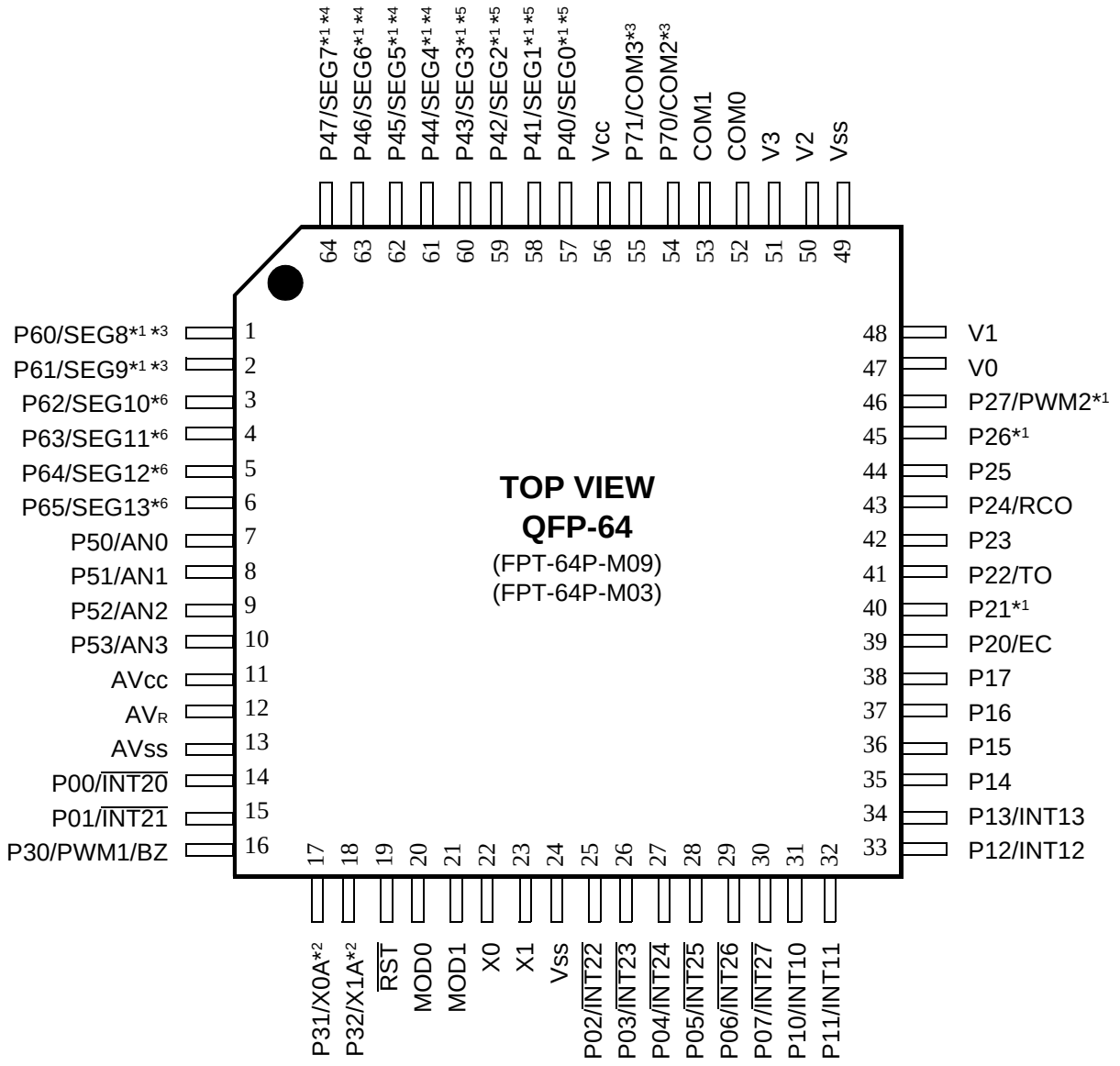
ALL pull-up resistor of MB89983 are selected by mask option (Port 0, 1, 2, 4, 5, 6)

5. Segment/Common port

The Segment/Port , Common/Port output in MB89P985 and MB89PV980 are selected by control register, LCR2.

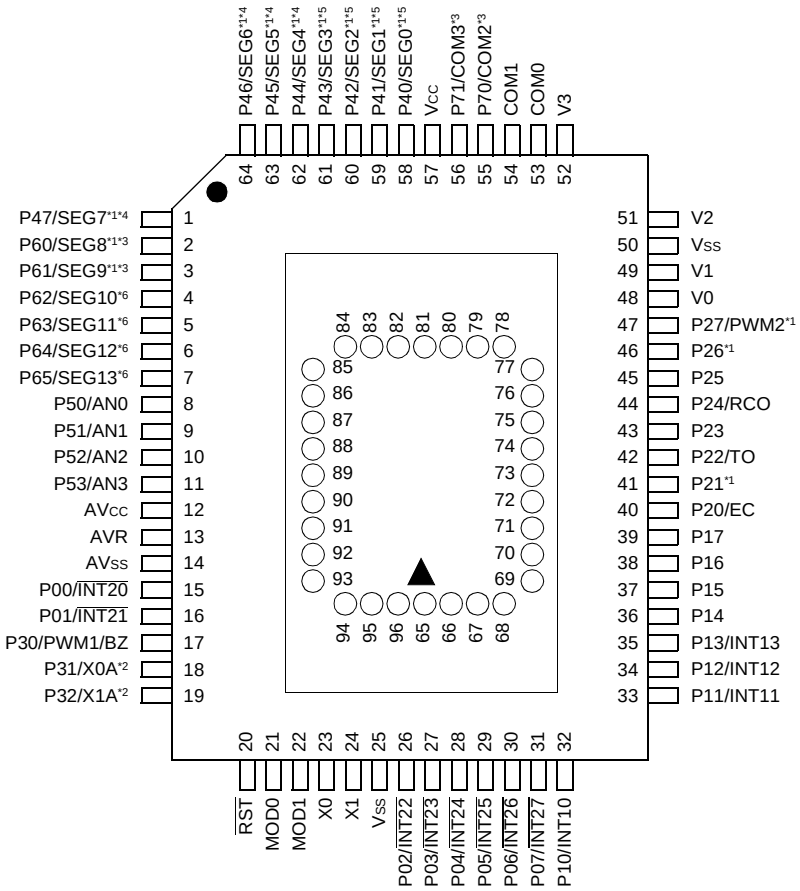
The Segment/Port , Common/Port output in MB89983 are selected by mask option.

■ PIN ASSIGNMENT



*1: Heavy-current drive type
*2: When the dual clock system is selected
*3, *4, *5, *6: Selected using mask option in MB89983, but selected by software in MB89P985 and MB89PV980.

(Top view)



(MQP-64C-P01)

*1: Heavy-current drive type
*2: When the dual clock system is selected
*3, *4,*5, *6: Selected using mask option in MB89983, but selected by software in MB89P985 and MB89PV980.

- Pin assignment on package top (MB89PV980 only)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	VPP	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	VSS	88	A10	96	VCC

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	I/O circuit type		Function
LQFP*1 QFP*2	MQFP*3		MB89983	MB89P985 MB89PV980	
22	23	X0	A		Crystal or other resonator connector pins for the main clock The external clock can be connected to X0. When this is done, be sure to leave X1 open. CR oscillation selectability in model with a mask ROM only.
23	24	X1			
20	21	MOD0	C		A hysteresis input type Memory access mode setting pins Connect directly to VSS.
21	22	MOD1			
19	20	$\overline{RST}$	D		Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset request (optional). The internal circuit is initialized by the input of “L”.
14 to 15	15 to 16	P00/$\overline{INT20}$ to P01/$\overline{INT21}$	E	F	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input is hysteresis input.
25 to 30	26 to 31	P02/$\overline{INT22}$ to P07/$\overline{INT27}$	E	F	General-purpose I/O ports Also serve as an external interrupt 2 input (wake-up function). External interrupt 2 input is hysteresis input.
31 to 34	32 to 35	P10/INT10 to P13/INT13	E	F	General-purpose I/O ports Also serve as input for external interrupt 1 input (wake-up function). External interrupt 1 input is hysteresis input.
35 to 38	36 to 39	P14 to P17	G	H	General-purpose I/O ports
39	40	P20/EC	J	K	N-ch open-drain general-purpose I/O port Also serve as the external clock input for the 8/16-bit timer/counter. The peripheral is a hysteresis input.
40	41	P21	L	M	N-ch open-drain general-purpose I/O port
41	42	P22/TO	L	M	N-ch open-drain general-purpose I/O port Also serves as an 8/16-bit timer/counter output.
42	43	P23	L	M	N-ch open-drain general-purpose I/O port
43	44	P24/RCO	L	M	N-ch open-drain general-purpose I/O port Also serves as Remote control output.
44 to 45	45 to 46	P25 to P26	L	M	N-ch open-drain general-purpose I/O port
46	47	P27/PWM2	L	M	N-ch open-drain general-purpose I/O port Also serves as the square wave or PWM wave output for the 8-bit PWM timer 2.

(Continued)

*1: FPT-64P-M03

*2: FPT-64P-M09

*3: MQP-64C-P01

(Continued)

Pin no.		Pin name	I/O circuit type		Function
LQFP*1 QFP*2	MQFP*3		MB89983	MB89P985 MB89PV980	
16	17	P30/PWM1/ BZ	I		General-purpose CMOS Output port Also serves as the square wave or PWM wave output for the 8-bit PWM timer 1, or buzzer output..
17	18	P31	S		General-purpose CMOS Input port (Hysteresis input type)
		X0A	B		Crystal or other resonator connector pins for the subclock (Subclock: 32.768 kHz) The external clock can be connected to X0A. When this is done, Be sure to leave X1A open.
18	19	P32	S		General-purpose CMOS Input port (Hysteresis input type)
		X1A	B		Crystal or other resonator connector pins for the subclock (Subclock: 32.768 kHz) The external clock can be connected to X0A. When this is done, Be sure to leave X1A open.
7 to 10	8 to 11	P50/AN0 to P53/AN3	P	Q	N-ch open-drain general-purpose output ports Also serve as the analog input for the A/D converter.
57 to 64	58 to 64 and 1	P40/SEG0 to P47/SEG7	N/O	T/O	N-ch open-drain general-purpose output ports (High current type) Also serve as an LCD controller/driver segment output.
1 to 2	2 to 3	P60/SEG8 to P61/SEG9	N/O	T/O	N-ch open-drain general-purpose output ports (High-current type) Also serve as an LCD controller/driver segment output.
3 to 6	4 to 7	P62/SEG10 to P65/SEG13	N/O	T/O	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver segment output.
54, 55	55, 56	P70/COM2, P71/COM3	N/O	T/O	N-ch open-drain general-purpose output ports Also serve as an LCD controller/driver common output.
52, 53	53, 54	COM0, COM1	O		LCD controller/driver common output

(Continued)

*1: FPT-64P-M03

*2: FPT-64P-M09

*3: MQP-64C-P01

(Continued)

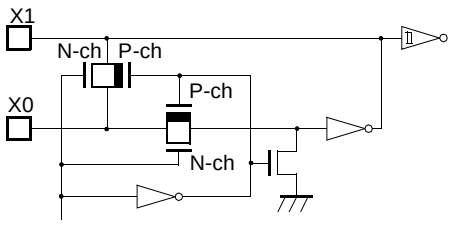
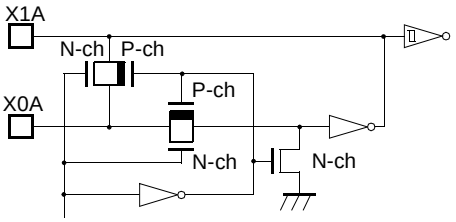
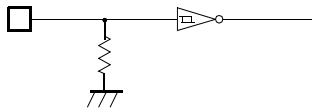
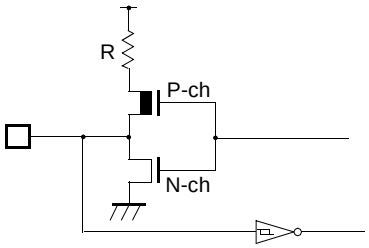
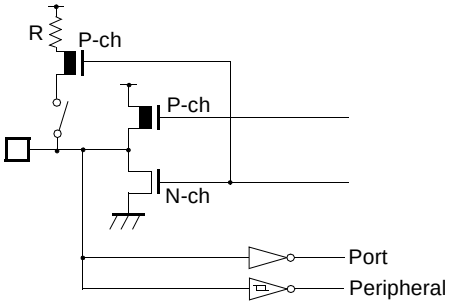
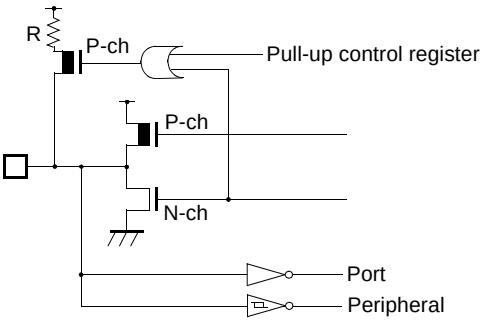
Pin no.		Pin name	I/O circuit type		Function
LQFP*1 QFP2*2	MQFP*3		MB89983	MB89P985 MB89PV980	
47, 48, 50, 51	48, 49 51, 52	V0 to V3	—	—	LCD driving power supply pins.
56	57	Vcc	—	—	Power supply pin
24, 49	25, 50	Vss	—	—	Power supply (GND) pin
11	12	AVcc	—	—	A/D converter power supply pin
12	13	AVR	—	—	A/D converter reference voltage input pin
13	14	AVss	—	—	A/D converter power supply pin Use this pin at the same voltage as VSS.

*1: FPT-64P-M03

*2: FPT-64P-M09

*3: MQP-64C-P01

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		Main clock (main clock crystal oscillator) • At an oscillation feedback resistor of approximately 1 MΩ/5.0 V • CR oscillation is selectable for MB89983 only
B		Subclock (subclock crystal oscillator) • At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V
C		• Hysteresis input • At a pull-down resistor (P-ch) of approximately 50 kΩ/5.0 V
D		• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
E		• CMOS output • CMOS input • The peripheral is a hysteresis input type. • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resistor is selected by mask option.
F		• CMOS output • CMOS input • The peripheral is a hysteresis input type. • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resisitor is selected by pull-up control register

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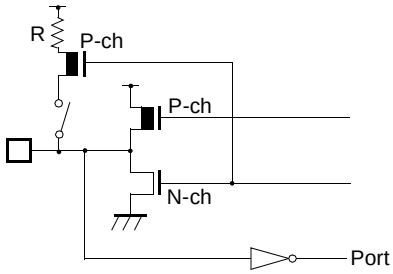
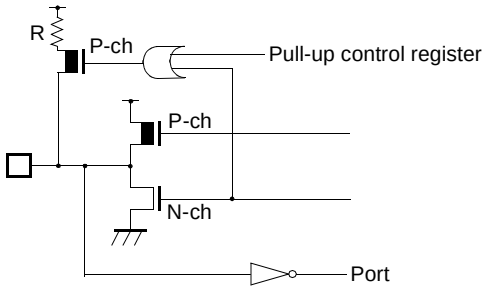
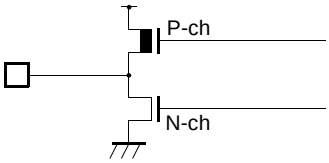
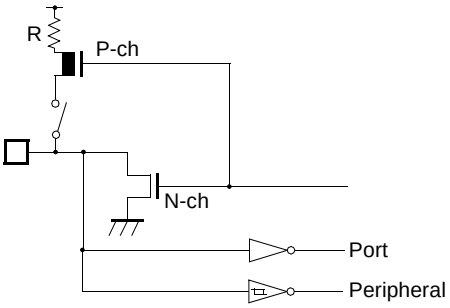
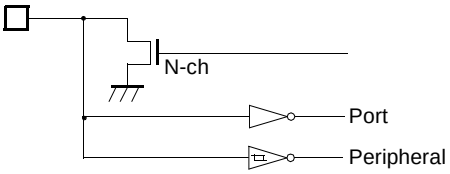
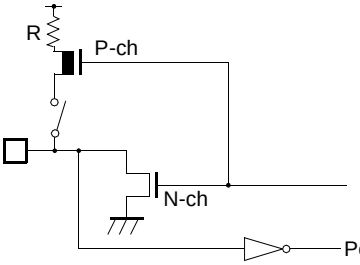
Type	Circuit	Remarks
G		• CMOS output • CMOS input • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resistor is selected by mask option.
H		• CMOS output • CMOS input • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resisitor is selected by pull-up control register
I		• CMOS output
J		• N-ch open-drain output • CMOS input • The peripheral is a hysteresis input type. • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resistor is selected by mask option.
K		• N-ch open-drain output • CMOS input • The peripheral is a hysteresis input type.
L		• N-ch open-drain output • CMOS input • P21, P26, and P27 are a heavy-current drive type. • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resistor is selected by mask option.

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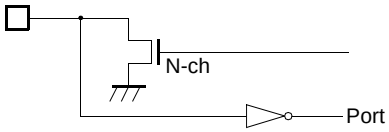
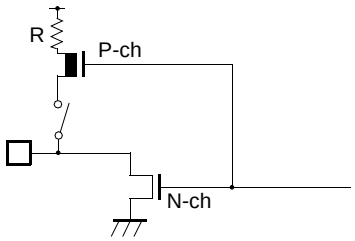
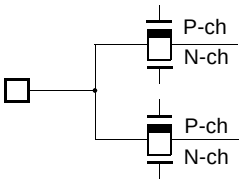
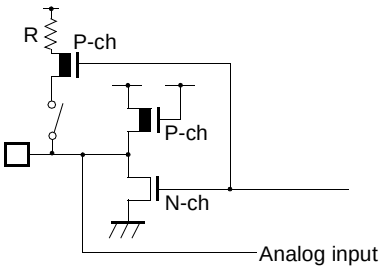
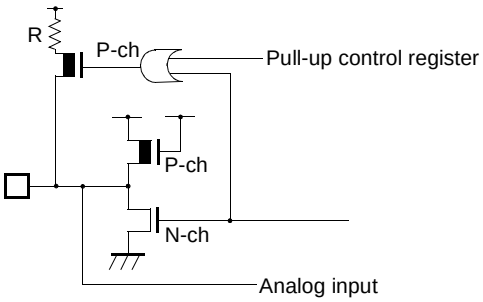
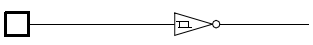
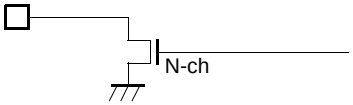
(Continued)

Type	Circuit	Remarks
M		• N-ch open-drain output • CMOS input • P21, P26, and P27 are a heavy-current drive type.
N		• N-ch open-drain output • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resistor is selected by mask option.
O		• LCD controller/driver common/segment output
P		• N-ch open-drain output • Analog input (A/D converter) • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resistor is selected by mask option.
Q		• N-ch open-drain output • Analog input (A/D converter) • Pull-up resistor is approximately 50 kΩ/5.0 V • Pull-up resisitor is selected by pull-up control register
S		• Hysteresis input
T		• N-ch open-drain output

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on " 1. Absolute Maximum Ratings" in section "■ Electrical Characteristics" is applied between V_{CC} to V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D Converters

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D converters are not in use.

4. Treatment of N.C. Pin

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

7. Treatment of two Vss pins

Two Vss pins should be connected together externally.

8. Treatment of input port pins in standby mode

To avoid current leakage, it is recommended to remain a known logic level of input port pins during the standby mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P985

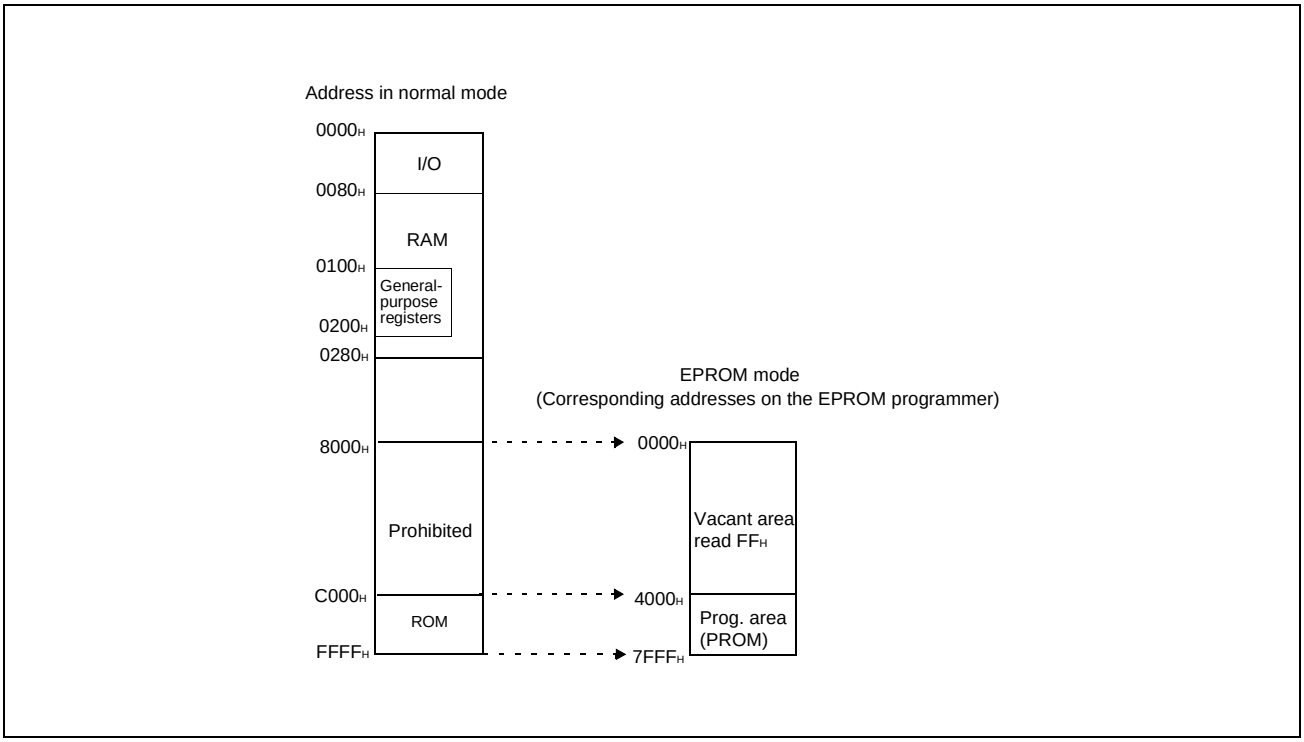
The MB89P985 is an OTPROM version of the MB89980 series.

1. Features

- 16-Kbyte PROM on chip
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P985 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

(1) Set the EPROM programmer to the MBM27C256A.

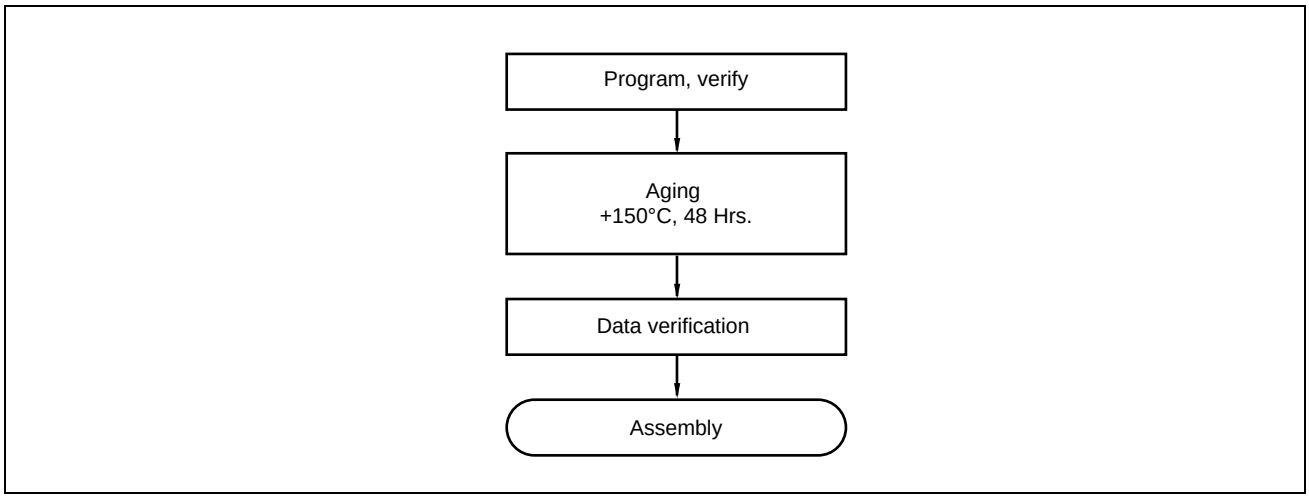
(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$
(note that addresses $C000_H$ to $FFFF_H$ while operating as a single chip assign to 4000_H to $7FFF_H$ in EPROM mode).

(3) Program with the EPROM programmer.

■ HANDLING THE MB89P985

1. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure.



2. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

3. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-64P-M03	TBD
FPT-64P-M09	TBD

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

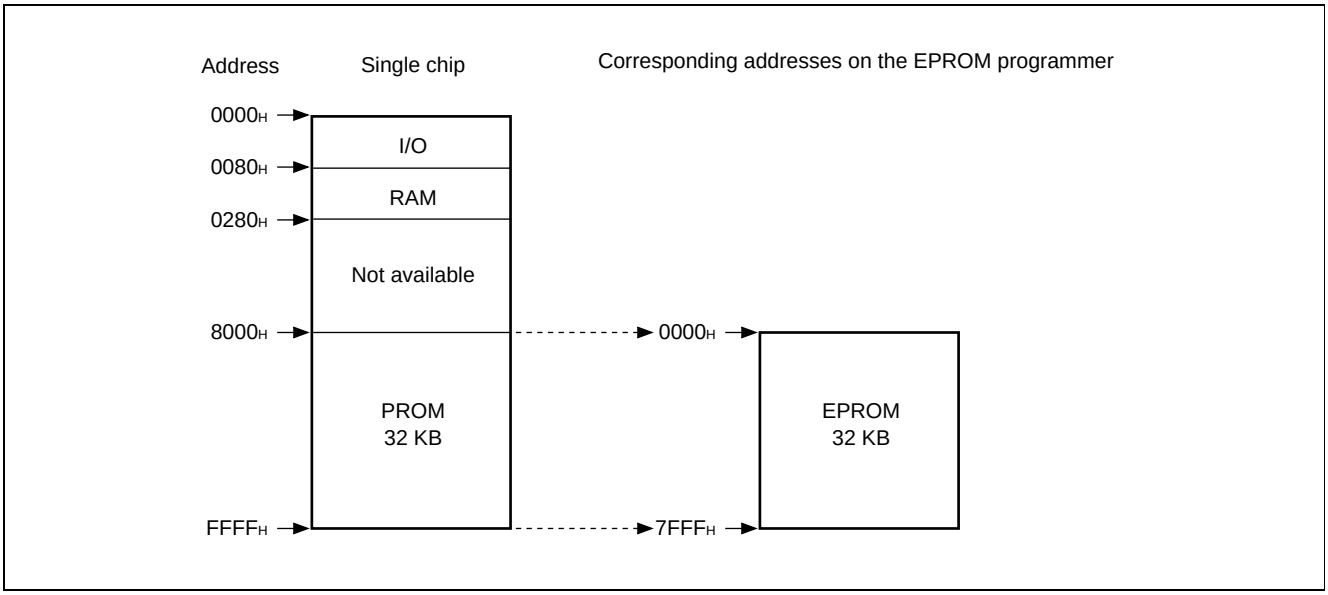
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32 (Rectangle)	ROM-32LC-28DP-YG

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode, such as 32-Kbyte PROM, option area is diagrammed below.



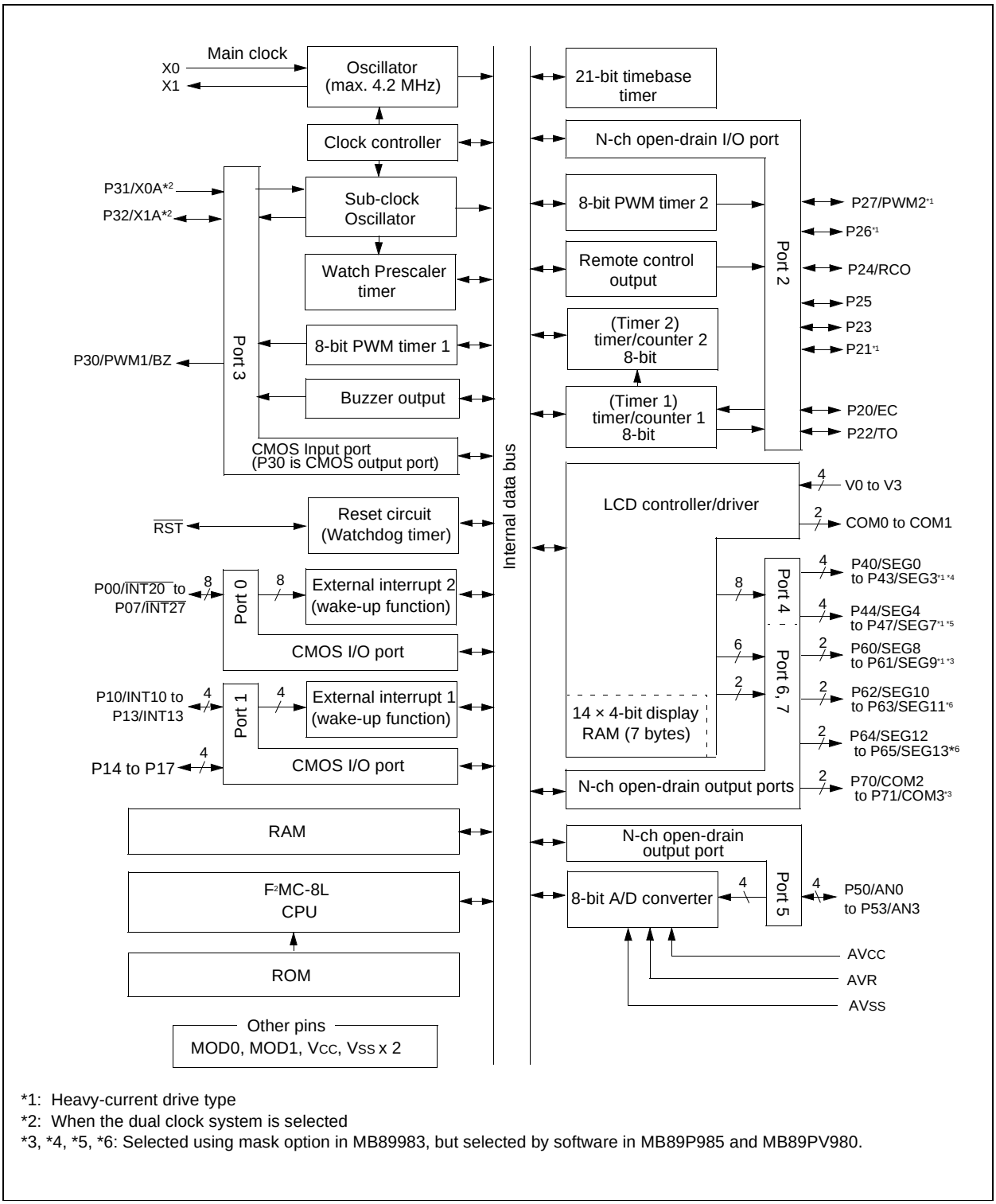
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

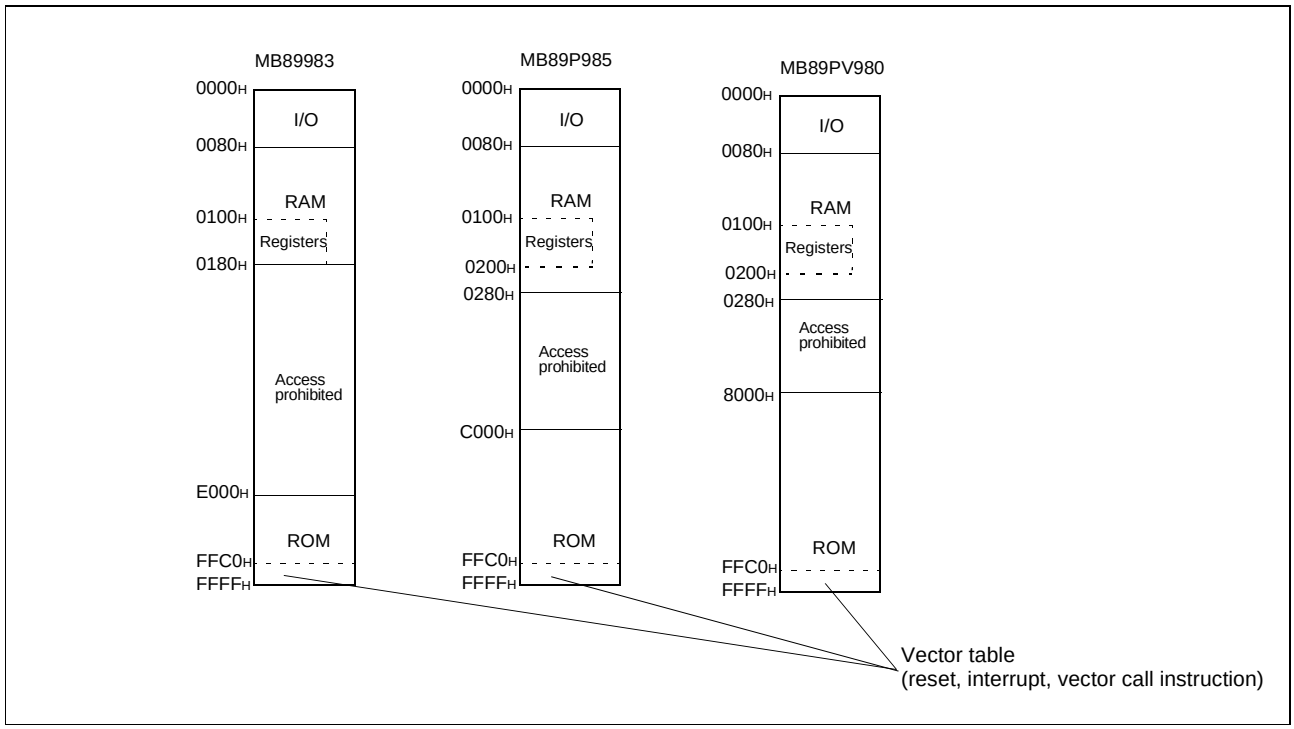


*1: Heavy-current drive type
*2: When the dual clock system is selected
*3, *4, *5, *6: Selected using mask option in MB89983, but selected by software in MB89P985 and MB89PV980.

■ CPU CORE

1. Memory Space

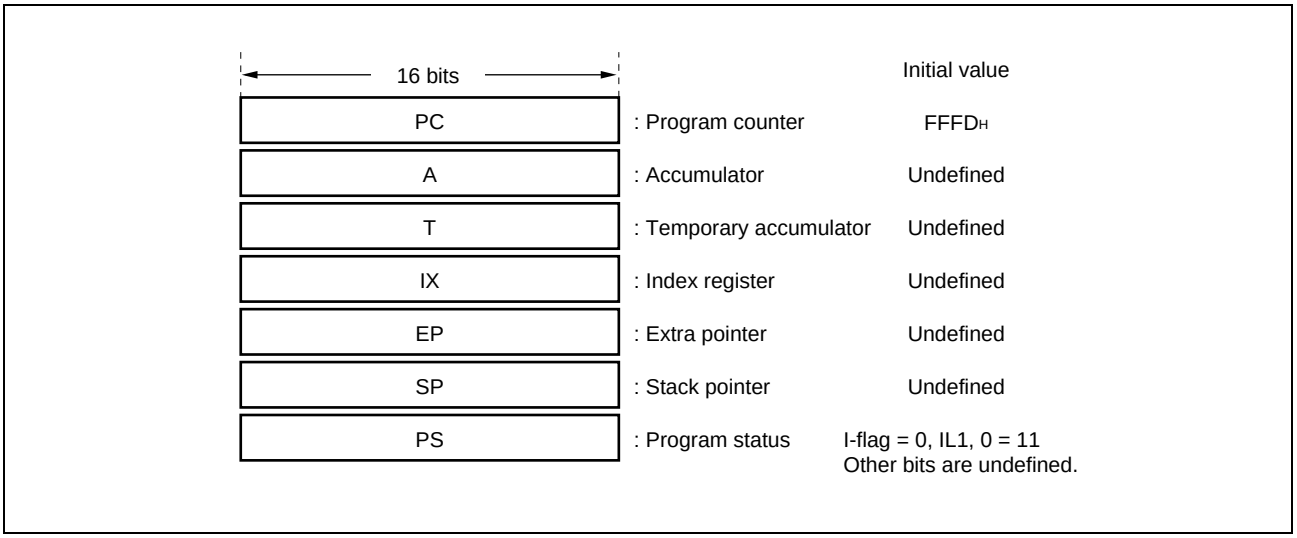
The microcontrollers of the MB89980 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89980 series is structured as illustrated below.



2. Registers

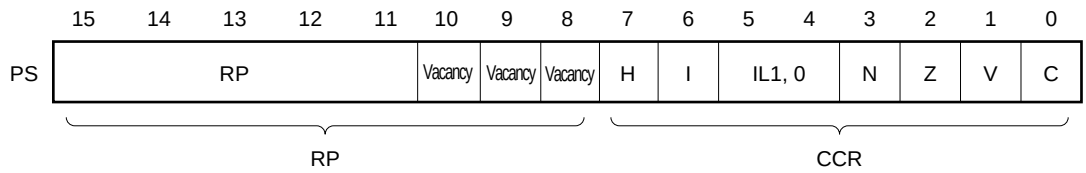
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 18-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



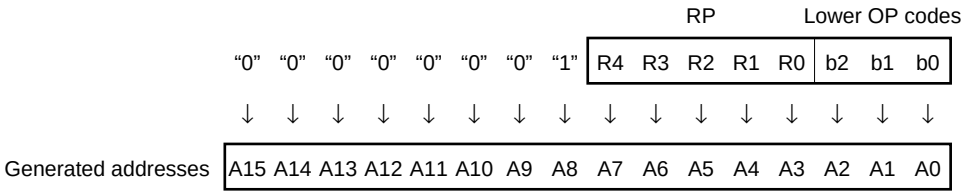
The PS can further be divide into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set the shift-out value in the case of a shift instruction.

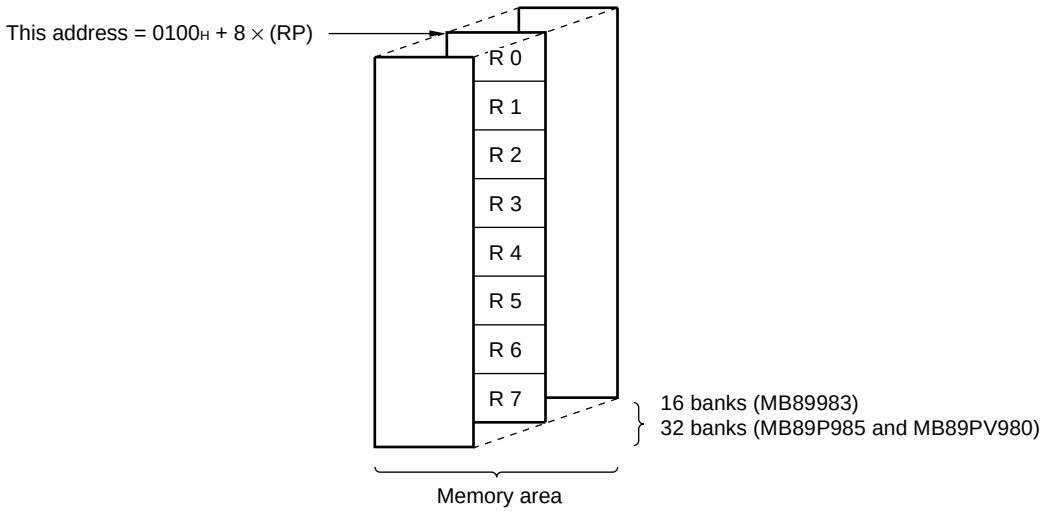
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 16 banks can be used on the MB89983 (RAM 256 × 8 bits). Up to a total of 32 banks can be used on the MB89P985 and MB89PV980 (RAM 512 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuraiton



■ I/O MAP

Address	Read/write	Register name	Register description
00H	R/W	PDR0	Port 0 data register
01H	W	DDR0	Port 0 data direction register
02H	R/W	PDR1	Port 1 data register
03H	W	DDR1	Port 1 data direction register
04H	R/W	PDR2	Port 2 data register
05H	W	DDR2	Port 2 data direction register
06H	(Vacancy)		
07H	R/W	SYCC	System clock control register
08H	R/W	STBC	Standby control register
09H	R/W	WDTC	Watchdog timer control register
0AH	R/W	TBTC	Timebase timer control register
0BH	R/W	WPCR	Watch prescaler control register
0CH	R/W	PDR3	Port 3 data register
0DH	(Vacancy)		
0EH	R/W	PDR4	Port 4 data register
0FH	R/W	PDR5	Port 5 data register
10H	R/W	BZCR	Buzzer register
11H	(Vacancy)		
12H	R/W	PDR6	Port 6 data register
13H	R/W	PDR7	Port 7 data register
14H	R/W	RCR1	Remote control transmission register 1
15H	R/W	RCR2	Remote control transmission register 2
16H to 17H	(Vacancy)		
18H	R/W	T2CR	Timer 2 control register
19H	R/W	T1CR	Timer 1 control register
1AH	R/W	T2DR	Timer 2 data register
1BH	R/W	T1DR	Timer 1 data register
1CH - 1DH	(Vacancy)		
1EH	R/W	CNTR1	PWM 1 control register
1FH	W	COMR1	PWM 1 compare register
20H	R/W	CNTR2	PWM 2 control register
21H	W	COMR2	PWM 2 compare register
22H to 2CH		(Vacancy)	
2DH	R/W	ADC1	A/D control register 1
2EH	R/W	ADC2	A/D control register 2
2FH	R/W	ADCD	A/D data register
30H	R/W	EIE1	External interrupt 1 control register
31H	R/W	EIF1	External interrupt 1 flag register

(Continued)

(Continued)

Address	Read/write	Register name	Register description
32H	R/W	EIE2	External interrupt 2 control register
33H	R/W	EIF2	External interrupt 2 flag register
34H to 3FH	(Vacancy)		
40H	R/W	PURR0	Pull-up control register 0 (For MB89P985/PV980 only)
41H	R/W	PURR1	Pull-up control register 1 (For MB89P985/PV980 only)
42H	R/W	PURR5	Pull-up control register 5 (For MB89P985/PV980 only)
43H to 5FH	(Vacancy)		
60H to 66H	R/W	VRAM	Display RAM
67H to 71H	(Vacancy)		
72H	R/W	LCR1	LCD control register 1
73H	R/W	LCR2	LCD control register 2 (For MB89P985/PV980 only)
74H to 7BH	(Vacancy)		
7CH	W	ILR1	Interrupt level setting register 1
7DH	W	ILR2	Interrupt level setting register 2
7EH	W	ILR3	Interrupt level setting register 3
7FH	Access prohibited	ITR	Interrupt test register

Notes: Do not use vacancies.

Notes: Read/write access symbols :

R/W : Readable and writable
R : Read-only
W : Write-only

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	AV_{CC} must not exceed V_{CC} + 0.3 V.
	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed AV_{CC} + 0.3 V.
LCD power supply voltage	V0 to V3	V_{SS} – 0.3	V_{SS} + 7.0	V	V0 to V3 must not exceed V_{CC}.
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	V_{I1} must not exceed V_{SS} + 7.0 V. All pins except P20 to P27 without a pull-up resistor
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P20 to P27 without a pull-up resistor
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	V_{O1} must not exceed V_{SS} + 7.0 V. All pins except P20 to P27, P40 to P47, P60 to P65, P70 and P71 without a pull-up resistor
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P20 to P27, P40 to P47, P60 to P65, P70 and P71 without a pull-up resistor
“L” level maximum output current	I_{OL1}	—	10	mA	All pins except P21, P26, P27, P40 to P47, P60 and P61
	I_{OL2}	—	20	mA	P21, P26, P27, P40 to P47, P60 and P61
“L” level average output current	I_{OLAV1}	—	4	mA	All pins except P21, P26, P27, P40 to P47, P60, P61 and power supply pins Average value (operating current × operating rate)
	I_{OLAV2}	—	8	mA	P21, P26, P27, P40 to P47, P60 and P61 Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	Peak value
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH1}	—	–5	mA	All pins except P30 and power supply pins
	I_{OH2}	—	–10	mA	P30

(Continued)

(Continued)

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
"H" level average output current	I_{OHAV1}	—	–2	mA	All pins except P30 and power supply pins Average value (operating current × operating rate)
	I_{OHAV2}	—	–4	mA	P30 Average value (operating current × operating rate)
"H" level total maximum output current	$\sum I_{OH}$	—	–50	mA	Peak value
"H" level total average output current	$\sum I_{OHAV}$	—	–10	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

Precautions: Parmanent device damage may occur if the above "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AV_{CC}	2.2*1	6.0*1	V	Normal operation assurance range*1
		2.2*1	4.0	V	Dual-clock mask ROM products
		1.5	6.0	V	Retains the RAM state in stop mode
	AVR	2.0	AV_{CC}	V	Normal operation assurance range
LCD power supply voltage	V0 to V3	V_{SS}	V_{CC}	V	V0 to V3 pins LCD power supply range (The optimum value dependent on the LCD element in use.)
Operating temperature	T_A	–40	+85	°C	

*1: The minimum operating power supply voltage varies with the execution time (instruction cycle time) setting for the operating frequency.
A/D converter assurance accuracy varies with the operating power supply voltage.

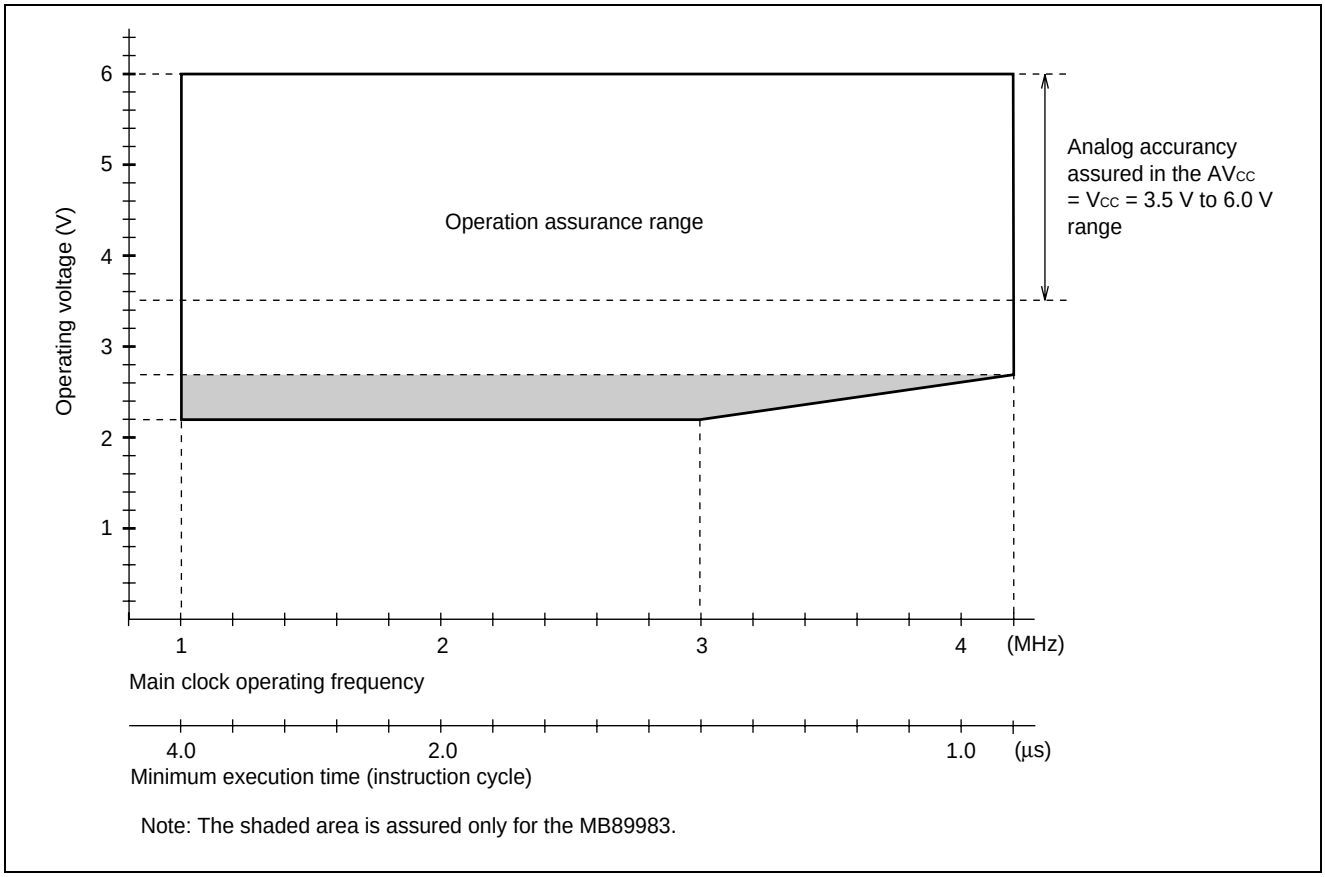


Figure 1 Operating Voltage vs. Main Clock Operating Frequency

Figures 1 indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

Warning: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely reliability and could result in device failure.

No warranty is made with respect to uses, operating condition, or combination not represented on the datasheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

2. DC Characteristics

(1) Pin DC characteristics (V_{CC} = +5.0 V)

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0, MOD1, EC, INT10 to INT13, INT20 to INT27		0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27		V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0, MOD1, EC, INT10 to INT13, INT20 to INT27		V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_{D1}	P20 to P27 P40 to P47, P60 to P65		V_{SS} – 0.3	—	V_{SS} + 6.0	V	P20 to P27 , P40 to P47, and P60 to P65 without pull-up resistor only
	V_{D2}	P50 to P53		V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17	I_{OH} = –2.0 mA	2.4	—	—	V	
	V_{OH2}	P30	I_{OH} = –6.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P30	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	P20, P22 to P25, P50 to P53, P62 to P65, P70 to P71	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL3}	P21, P26, P27, P40 to P47, P60, P61	I_{OL} = 8.0 mA	—	—	0.4	V	
	V_{OL4}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI}	P00 to P07, P10 to P17, MOD0, MOD1, P30	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor

(Continued)

(Continued)

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Open-drain output leakage current	I_{LO1}	P20 to P27, P40 to P47, P60 to P65, P70, P71	0.45 V < V_I < 6.0 V	—	—	±5	µA	Without pull-up resistor
	I_{LO2}	P50 to P53	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P53, P60 to P65, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	With pull-up resistor
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = +5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to SEG13		—	—	15	kΩ	
LCD divided resistance	R_{LCD}	—	Between V_{CC} and V0	300	500	750	kΩ	
LCD controller/driver leakage current	I_{LCDL}	V0 to V3, COM0 to COM3, SEG0 to SEG13	—	—	—	±1	µA	
Input capacitance	C_{IN}	Other than V_{CC}, V_{SS}	f = 1 MHz	—	10	—	pF	

Note: For pins which serve as the segment (SEG0 to SEG13) and ports (P40 to P47, P50 to P53, and P60 to P65), see the port parameter when these pins are used as ports and the segment parameter when they are used as segments.

(2) Pin DC Characteristics (V_{CC} = +3.0 V)

(V_{CC} = 3.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17	I_{OH} = –1.0 mA	2.4	—	—	V	
	V_{OH2}	P30	I_{OH} = –3.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P20 to P27, P30, P50 to P53, P62 to P65, P70 to P71	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL3}	P21, P26, P27 P40 to P47, P60, P61	I_{OL} = 3.6 mA	—	—	0.4	V	
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P53, P60 to P65, P70 to P71 $\overline{RST}$	V_I = 0.0 V	50	100	150	kΩ	With pull-up resistor

(3) Power Supply Current Characteristics (MB89983)

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CC1}	V_{CC}	F_{CH} = 4.2 MHz, V_{CC} = 5.0 V t_{inst}*2 = 4/F_{CH} Main clock operation mode	—	5.0	10.0	mA	MB89983
	I_{CC2}		F_{CH} = 4.2 MHz, V_{CC} = 3.0 V t_{inst}*2 = 64/F_{CH} Main clock operation mode	—	1.5	2.0	mA	
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V t_{inst}*2 = 2/F_{CL} Subclock operation mode	—	0.05	0.1	mA	
	I_{CCS1}		F_{CH} = 4.2 MHz, V_{CC} = 5.0 V t_{inst}*2 = 4/F_{CH} Main clock sleep mode	—	2.5	5.0	mA	
	I_{CCS2}		F_{CH} = 4.2 MHz, V_{CC} = 3.0 V t_{inst}*2 = 64/F_{CH} Main clock sleep mode	—	1.0	1.5	mA	
	I_{CCSL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V t_{inst}*2 = 2/F_{CL} Subclock sleep mode	—	25	50	μA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V Watch mode	—	10	15	μA	
	I_{CCH}		T_A = +25×C, V_{CC} = 5.0 V Stop mode	—	0.1	1.0	μA	
	I_A	AV_{CC}	F_{CH} = 4.2 MHz, V_{CC} = 5.0 V	—	1.0	3.0	mA	When A/D conversion is activated

*1: The power supply current is measured at the external clock, open output pins, and the external LCD dividing resistor (or external input for the reference voltage).

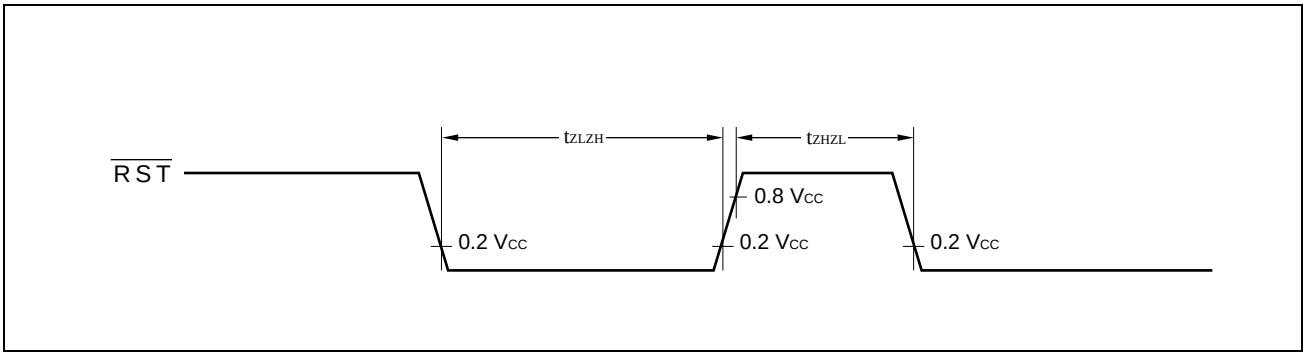
*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

4. AC Characteristics

(1) Reset Timing

(V_{CC} = +5.0 V ±10 %, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}	—	ns	
$\overline{RST}$ "H" pulse width	t_{ZHZL}		24 t_{XCYL}	—	ns	

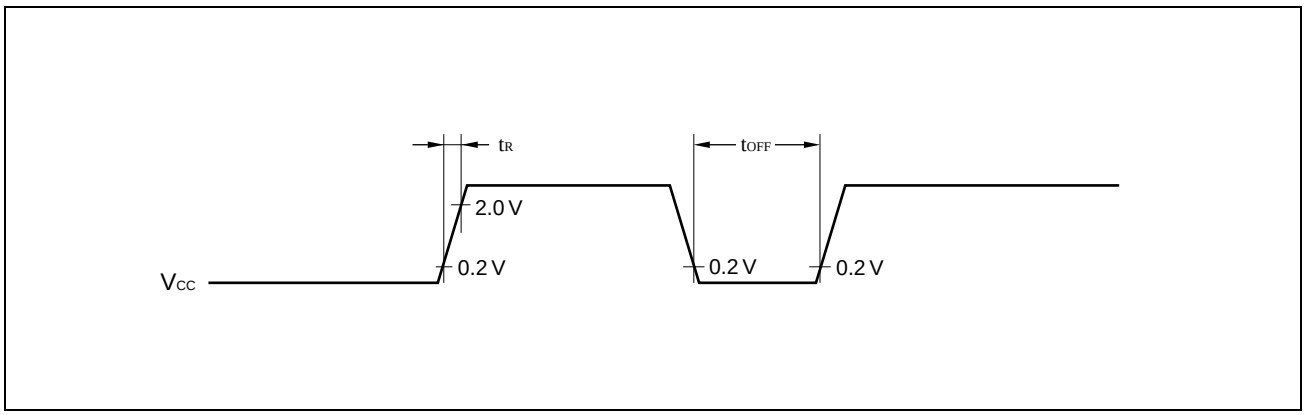


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}	—	1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

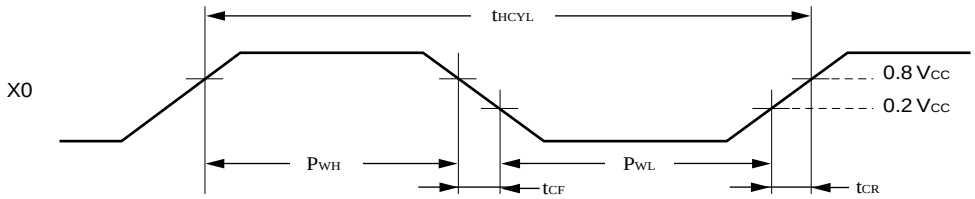


(3) Clock Timing

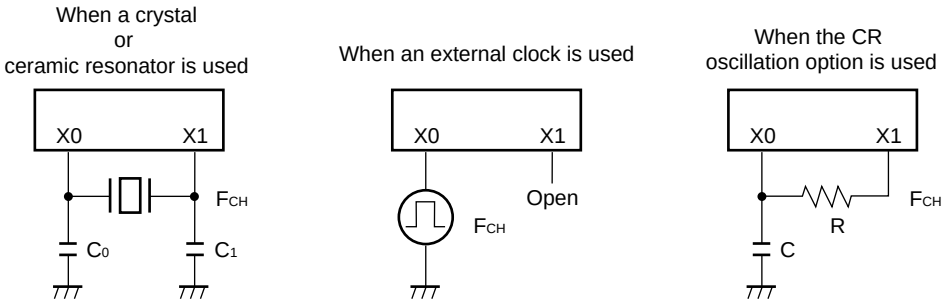
(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	4.2	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	238	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0	—	—	24	ns	

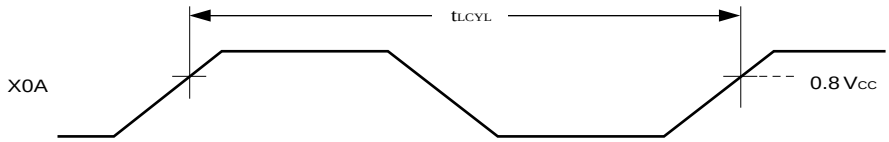
Main Clock Timing and Conditions



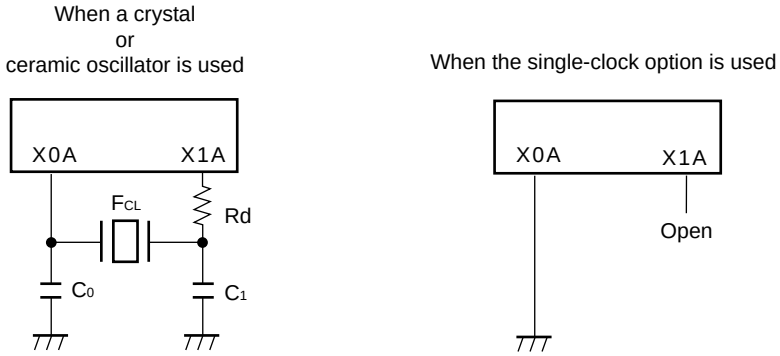
Main Clock Conditions



Subclock Timing and Conditions



Subclock Conditions



(4) Instruction Cycle

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

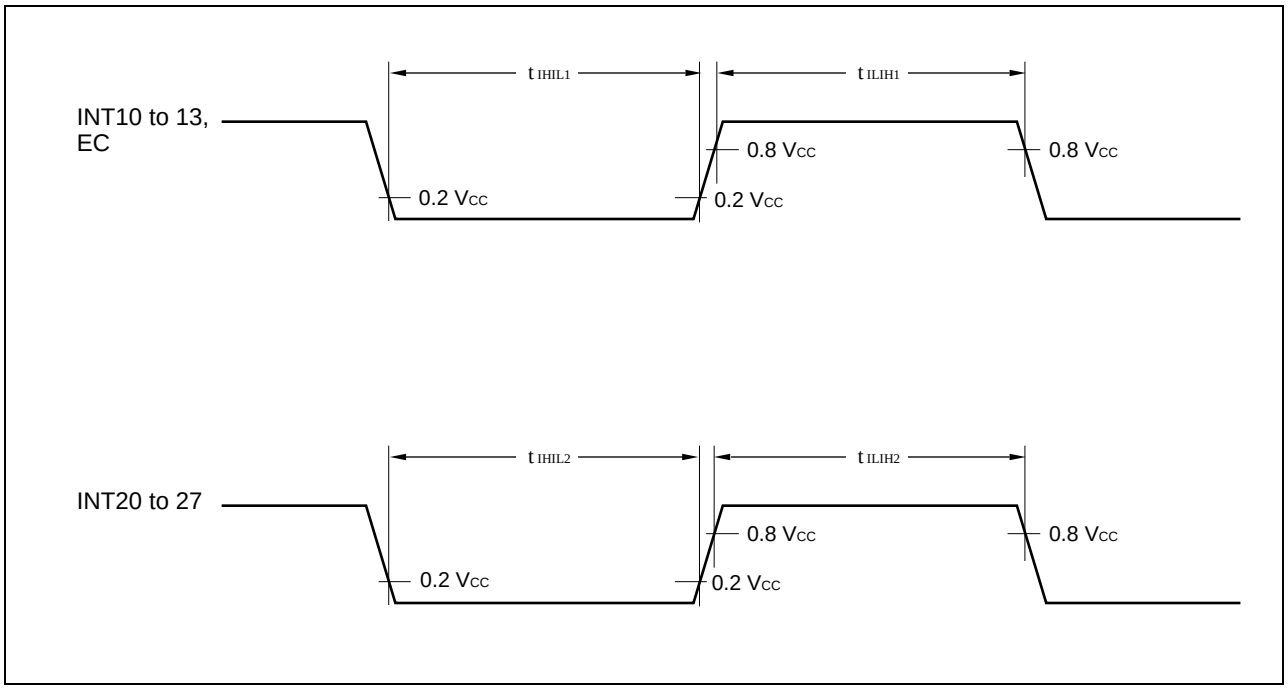
Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	4/F_{CH}, 8/F_{CH}, 16/F_{CH}, 64/F_{CH}	µs	(4/F_{CH}) t_{inst} = 1.0 µs at F_{CH} = 4 MHz
		2/F_{CL}	µs	t_{inst} = 62 µs at F_{CL} = 32.768 kHz

(5) Peripheral Input Timing

(V_{CC} = +5.0 V ±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT10 to INT13, EC	1 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}		1 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	INT20 to INT27	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



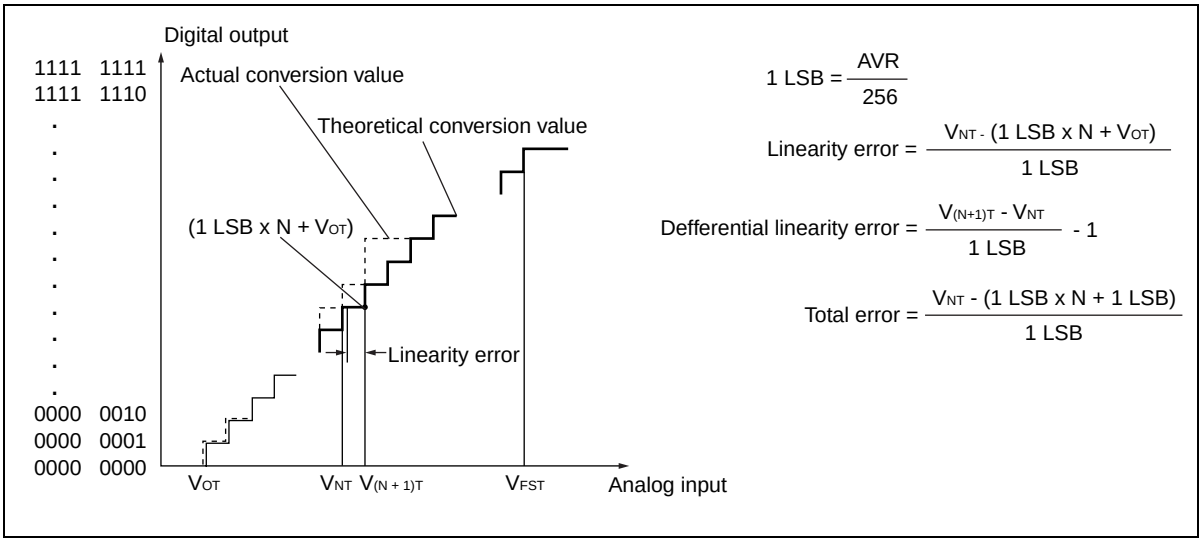
5. A/D Converter Electrical Characteristics

(3 MHz, $AV_{CC} = V_{CC}$ = +3.5 V to +6.0 V, $AV_{SS} = V_{SS}$ = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error			AVR = AV_{CC}	—	—	±1.5	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}			AV_{SS} – 1.0 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.0 LSB	mV	
Full-scale transition voltage	V_{FST}			AVR – 3.0 LSB	AVR – 1.5 LSB	AVR	mV	
Interchannel disparity	—			—	—	0.5	LSB	
A/D mode conversion time			—	—	44 t_{inst}	—	ms	
Sense mode conversion time				—	12 t_{inst}	—	ms	
Analog port input current	I_{AI}	AN0 to AN3		—	—	10	µA	
Analog input voltage	—			0.0	—	AVR	V	
Reference voltage	—	AVR		2.0	—	AV_{CC}	V	
Reference voltage supply current	I_R		AVR = 5.0 V, when A/D conversion is activated	—	100	—	µA	
	I_{RH}		AVR = 5.0 V, when A/D conversion is stopped	—	—	1	µA	

(1) A/D Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 8, analog voltage can be divided into 2^8=256.
- Linearity error (unit: LSB)
  The deviation of the straight line connecting the zero transition point (“0000 0000” ↔ “0000 0001”) with the full-scale transition point (“1111 1111” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



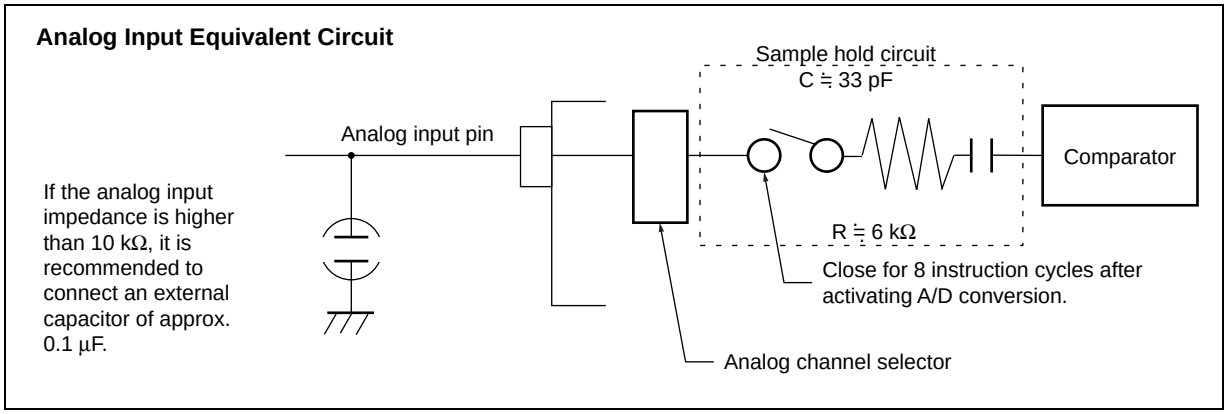
(2) Precautions

- **Input impedance of analog input pins**

The A/D converter contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 10 kΩ).

Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 µF for the analog input pin.

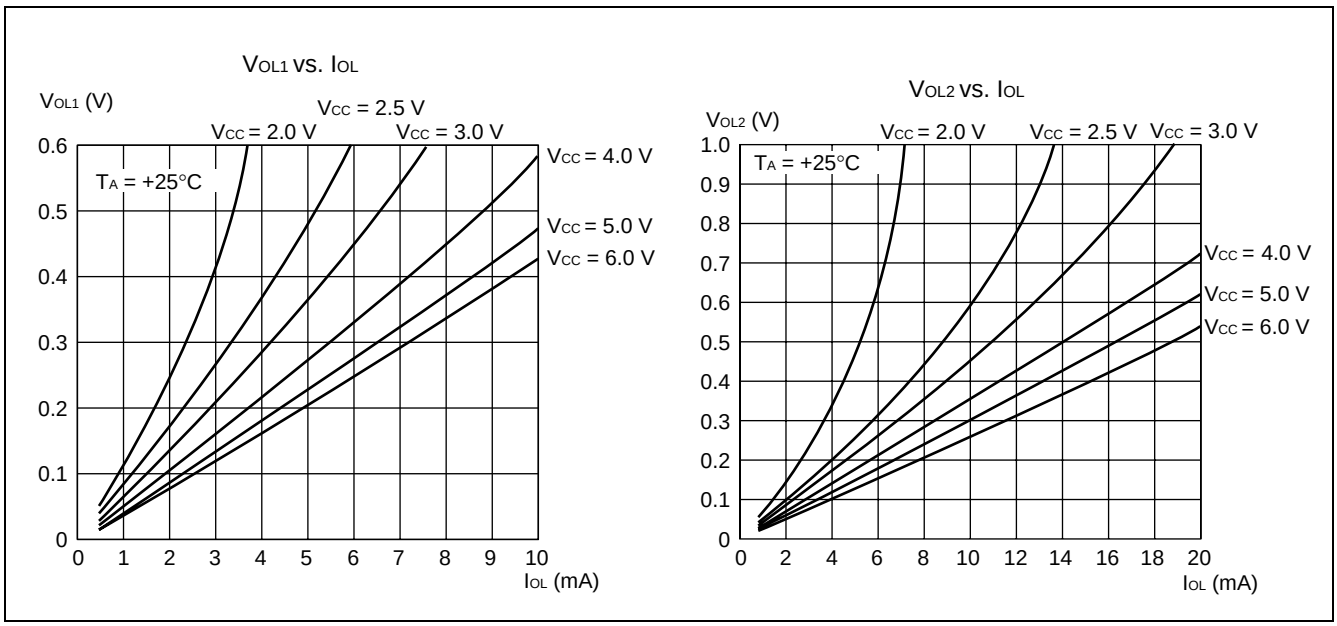


- **Error**

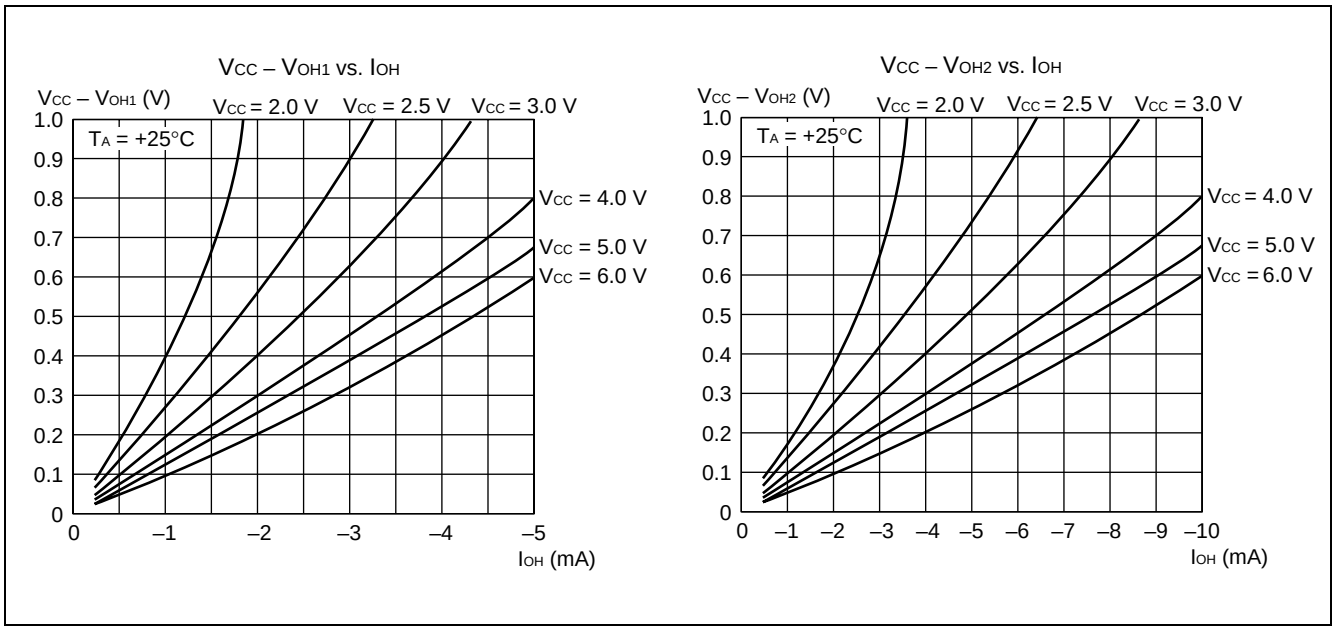
The smaller the |AVR – AVSS|, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

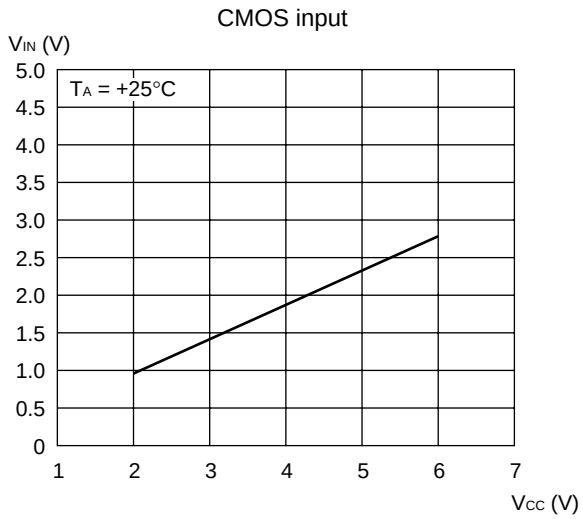
1. “L” Level Output Voltage

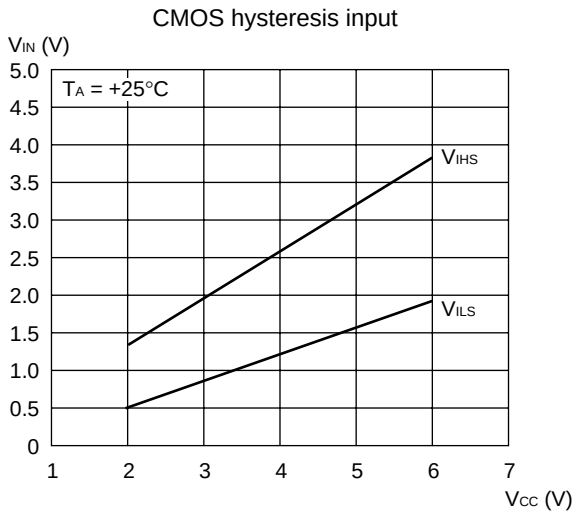


2. “H” Level Output Voltage



3. “H” Level Input Voltage/“L” level Input Voltage

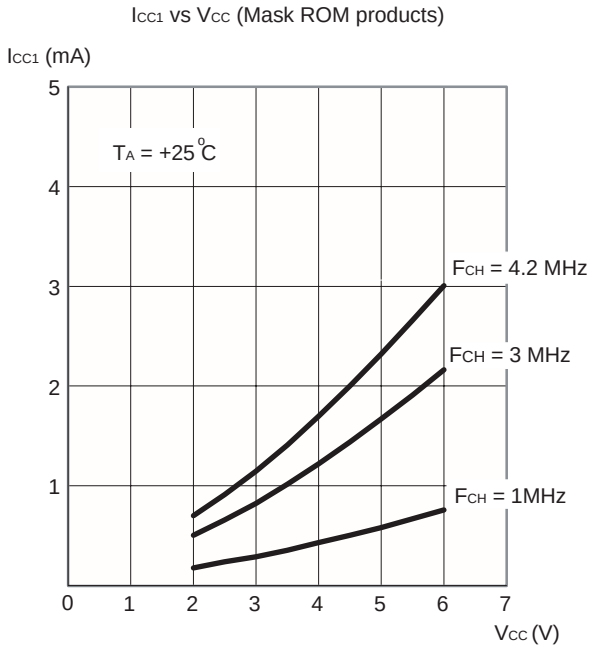


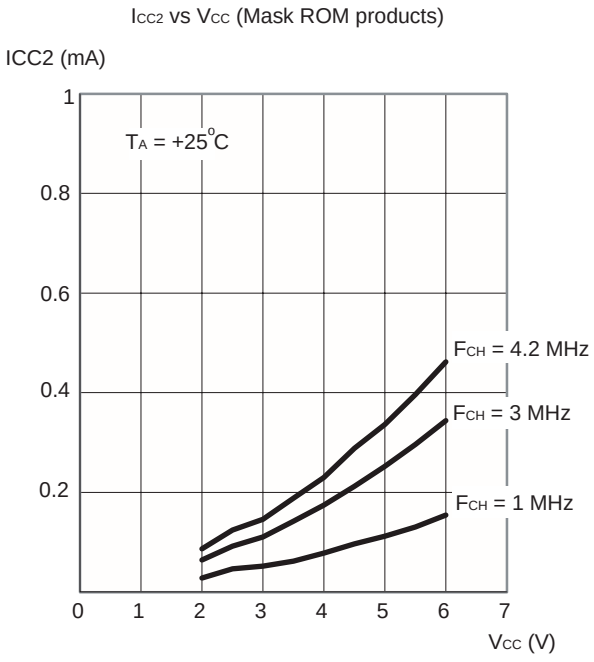


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

4. Power Supply Current (External Clock)





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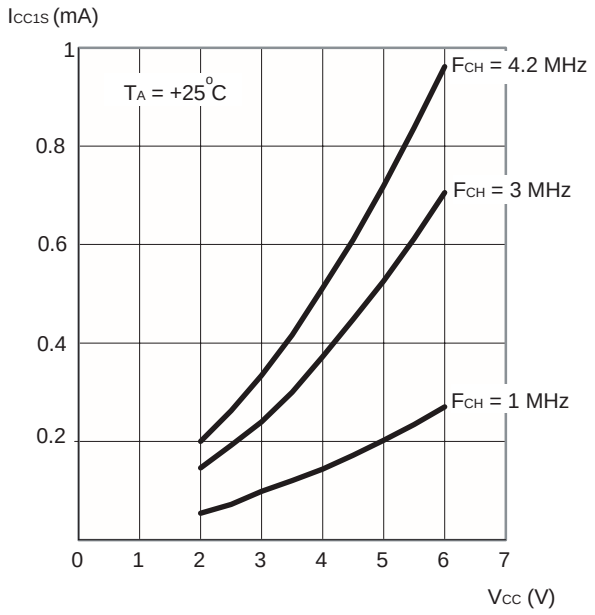
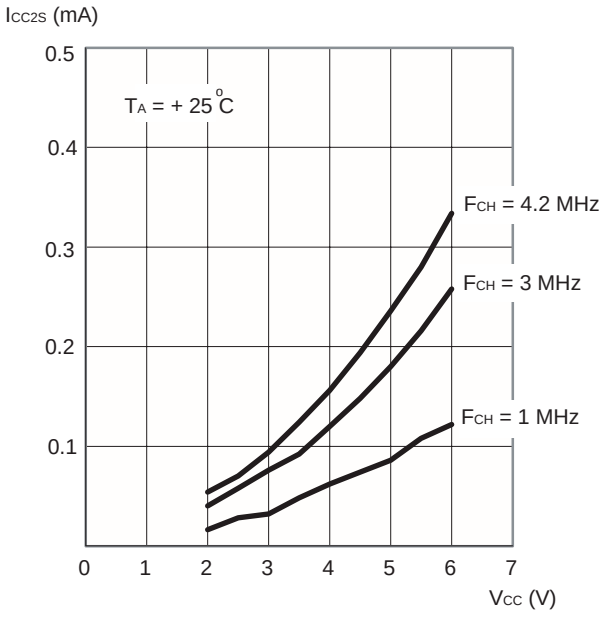
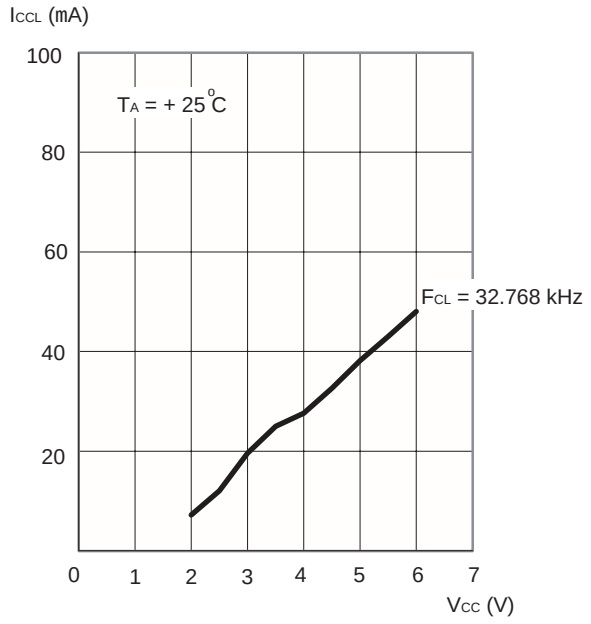
I_{CC1S} vs V_{CC} (Mask ROM products)



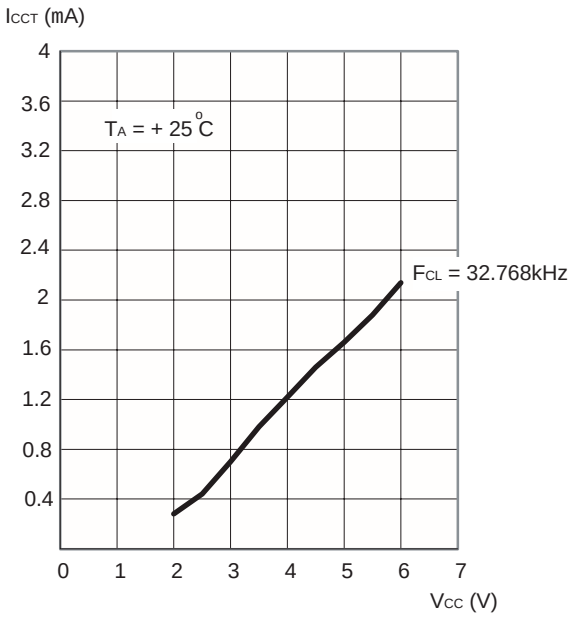
I_{CC2S} vs V_{CC} (Mask ROM products)



I_{CCL} vs V_{CC} (Mask ROM products)



I_{CCT} vs V_{CC}



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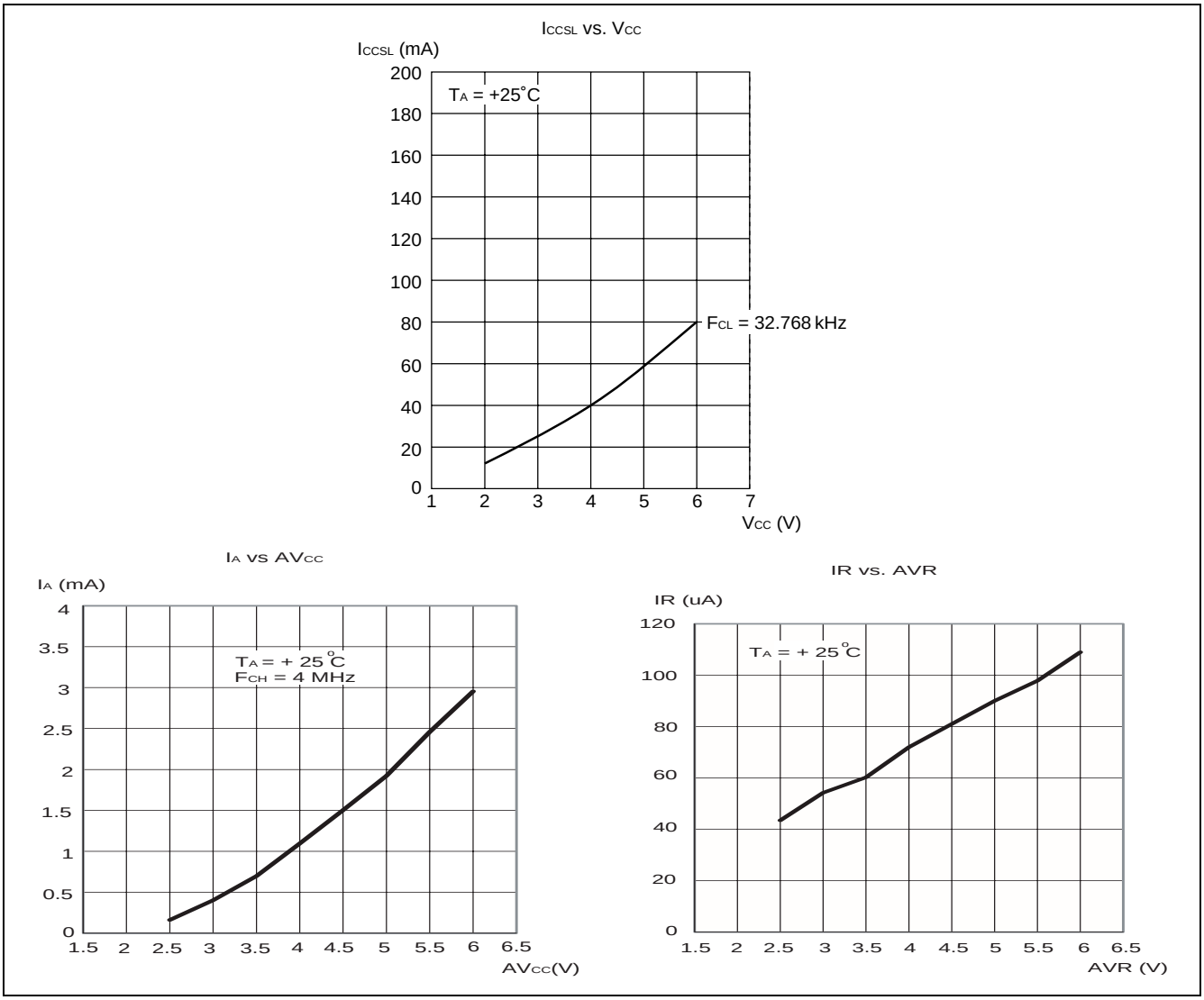

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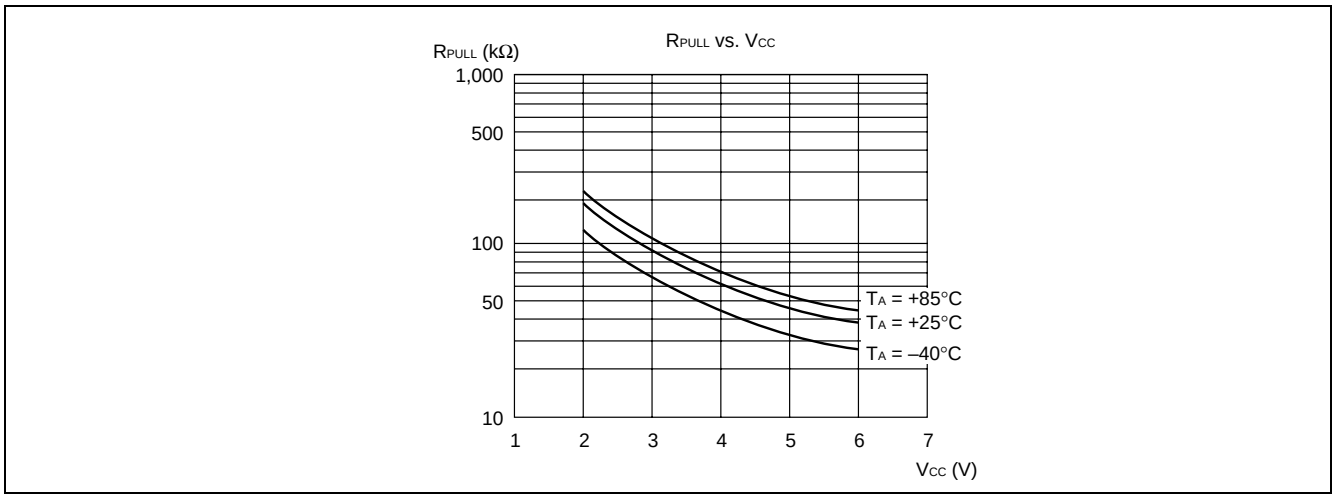
5. Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation for instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

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Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A →	–	–	–	+ + – +	03
ROLC A	2	1	← C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No.	Part number	MB89983	MB89P985	MB89PV980
	Specifying procedure	Specify when ordering masking	Setting with software	Setting with software
1	Pull-up resistors (SEG) P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P53, P60 to P65	Slectable per pin (The pull-up resistors for P40 to P47 and P60 to P65 are only selectable when these pins are not set as segment/ common outputs. When the A/D is used, P50 to P53 are must not selected.)	Selectable per pin by pull-up control registers. (Pull-up resistors are not available for P20 to P27, P40 to P47 and P60 to P65. Furthermore, P50 to P53 must be set to without a pull-up resistor when an A/D converter is used.)	Selectable per pin by pull-up control registers. (Pull-up resistors are not available for P20 to P27, P40 to P47 and P60 to P65. Furthermore, P50 to P53 must be set to without a pull-up resistor when an A/D converter is used.)
2	Power-on reset (POR) With power-on reset Without power-on reset	Selectable	Fixed with power-on reset	Fixed with power-on reset
3	Selection of oscillation stabilization time (OSC) • The initial value of the oscillation stabilization time for the main clock can be set by selecting the values of the WT1 and WT0 bits on the right.	Selectable OSC 0 : $2^2/F_{CH}$ 1 : $2^{12}/F_{CH}$ 2 : $2^{16}/F_{CH}$ 3 : $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of 2^{18}/FCH (Approx. 62.4 ms).	Fixed to oscillation stabilization time of 2^{18}/FCH (Approx. 62.4 ms).
4	Main clock oscillation type (XSL) Crystal or ceramic resonator CR	Selectable	Crystal or ceramic resonator only	Crystal or ceramic resonator only
5	Reset pin output (RST) With reset output Without reset output	Selectable	Fixed with reset output	Fixed with reset output
6	Clock mode selection (CLK) Dual-clock mode Single-clock mode	Selectable	Selection by version number 101 : Single clock 201 : Dual clock	Selection by version number 101 : Single clock 201 : Dual clock

- **Segment Options**

No.	Part number	MB89983
	Specifying procedure	**Specify when ordering masking**
7	LCD output pin configuration choices	Specify by the option combinations listed below
	SEG = 3: P40 to P47 segment output P60 to P65 segment output P70, P71 common output	Specify as SEG = 3
	SEG = 2: P40 to P43 port output P44 to P47 segment output P60 to P65 segment output P70, P71 common output	Specify as SEG = 2
	SEG = 1: P40 to P47 port output P60 to P65 segment output P70, P71 common output	Specify as SEG = 1
	SEG = 0: P40 to P47 port output P60 to P65 port output P70, P71 port output	Specify as SEG = 0

■ VERSIONS

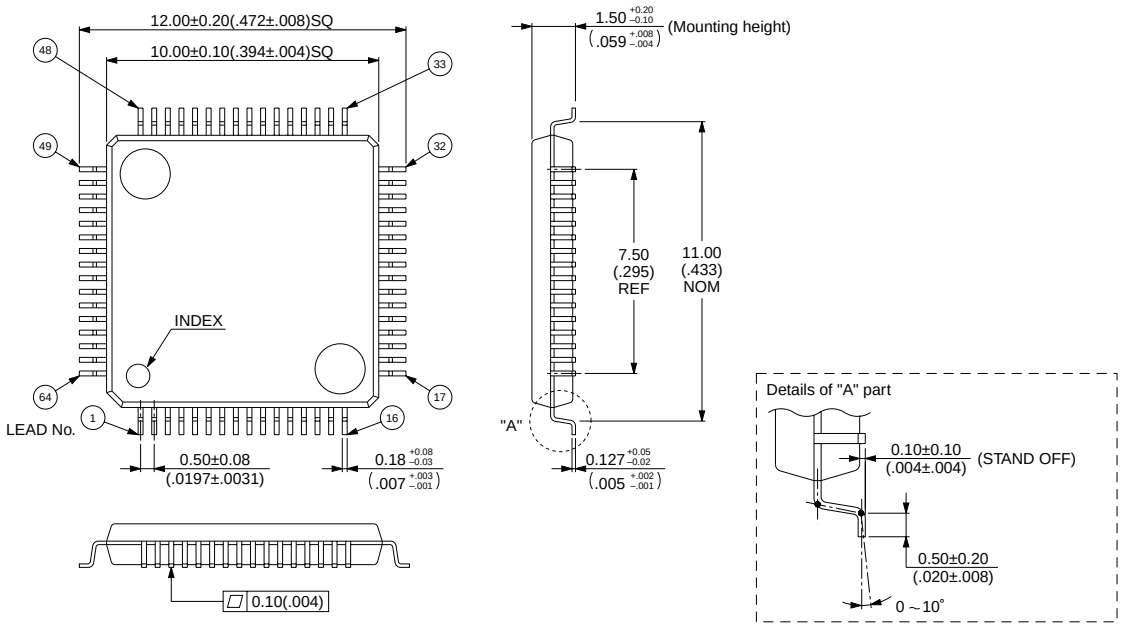
Version			Features
Mass production product	**One-time PROM product**	**Piggyback product**	**Clock mode**
MB89983	MB89P985-101	MB89PV980-101	Single clock
MB89983	MB89P985-201	MB89PV980-201	Dual clock

■ ORDERING INFORMATION

Part Number	Package	Remarks
MB89983-xxx-PFV	64-pin Plastic LQFP (FPT-64P-M03)	
MB89983-xxx-PFM	64-pin Plastic QFP (FPT-64P-M09)	
MB89P985PFV-101	64-pin Plastic LQFP (FPT-64P-M03)	Single Clock
MB89P985-PFM-101	64-pin Plastic QFP (FPT-64P-M09)	
MB89P985PFV-201	64-pin Plastic LQFP (FPT-64P-M03)	Dual Clock
MB89P985-PFM-201	64-pin Plastic QFP (FPT-64P-M09)	
MB89PV980-101	64-pin Ceramic MQFP (MQP-64C-P01)	Single Clock
MB89PV980-201	64-pin Ceramic MQFP (MQP-64C-P01)	Dual Clock

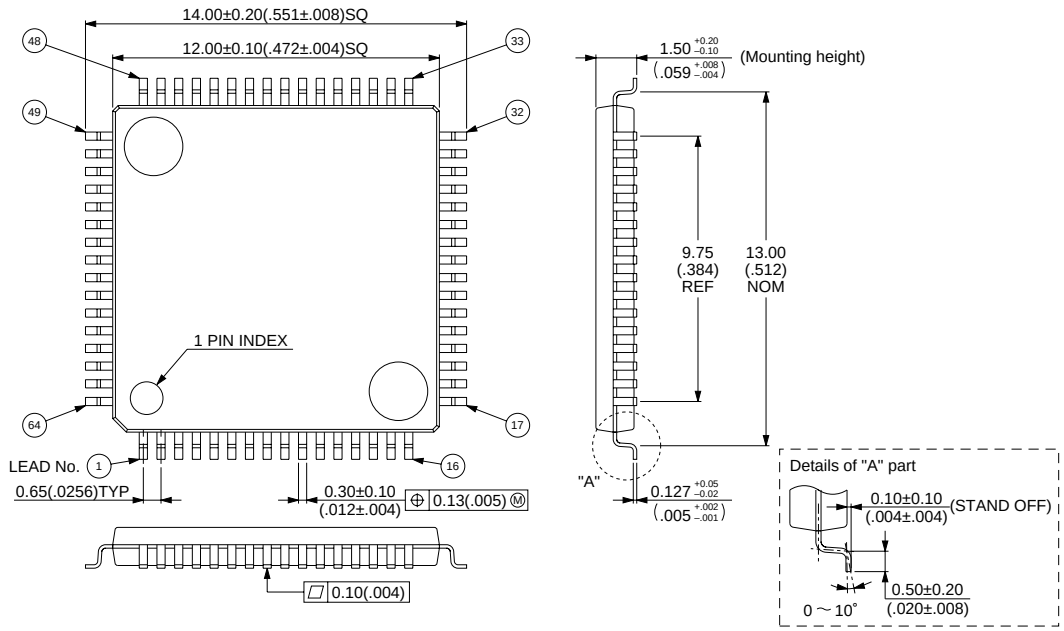
■ PACKAGE DIMENSIONS

64-pin Plastic LQFP
(FPT-64P-M03)



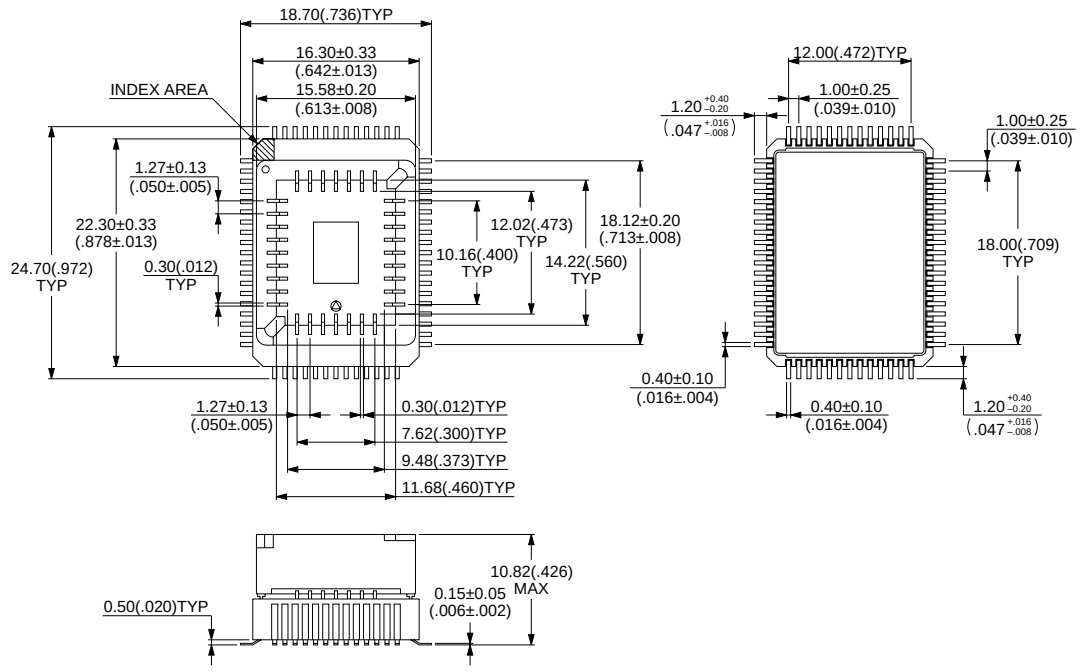
Dimension in mm (inches)

64-pin Plastic QFP
(FPT-64P-M09)



Dimension in mm (inches)

64-pin Ceramic MQFP
(MQP-64C-P01)



Dimension in mm (inches)

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