N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.011 @ V_{GS} = 10 V	15.8
	0.013 @ V_{GS} = 6 V	14.5

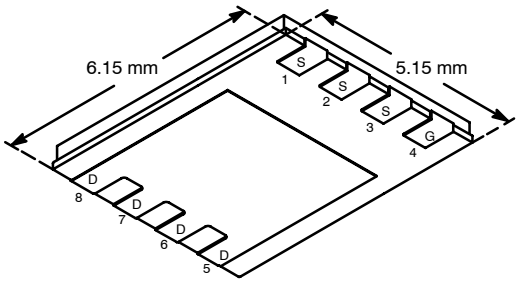
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100% R_g Tested

APPLICATIONS

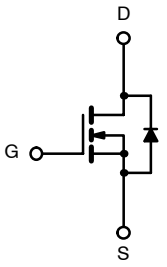
- Primary Side Switch for 24-V DC/DC Applications
- Secondary Synchronous Rectifier

PowerPAK SO-8



Bottom View

Ordering Information: Si7370DP-T1
Si7370DP-T1—E3 (Lead (Pb)-Free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	60		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	15.8	9.6	A
	T_A = 70°C		12.6	7.7	
Continuous Source Current		I_S	4.7	1.7	
Pulsed Drain Current		I_{DM}	50		
Avalanche Current		I_{AS}	50		
Single Avalanche Energy		E_{AS}	125		mJ
Maximum Power Dissipation	T_A = 25°C	P_D	5.2	1.9	W
	T_A = 70°C		3.3	1.25	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	19	24	°C/W
	Steady State		52	65	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.5	1.8	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

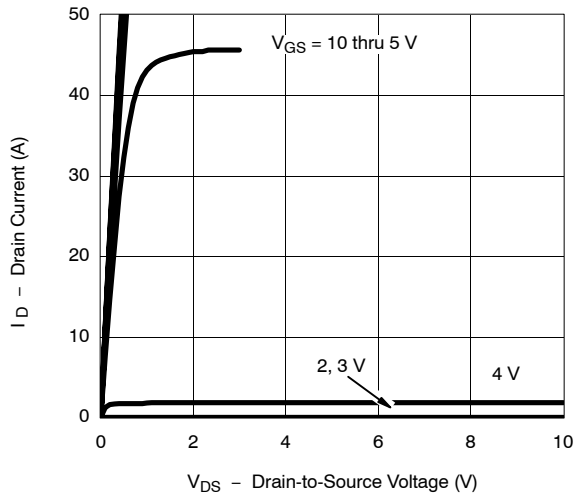
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0		4.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	μA
		V_{DS} = 60 V, V_{GS} = 0 V, T_J = 55°C			5	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	50			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 12 A		0.009	0.011	Ω
		V_{GS} = 6.0 V, I_D = 10 A		0.0105	0.013	
Forward Transconductance[a]	g_{fs}	V_{DS} = 15 V, I_D = 10 A		50		S
Diode Forward Voltage[a]	V_{SD}	I_S = 3.0 A, V_{GS} = 0 V		0.75	1.2	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = 30 V, V_{GS} = 10 V, I_D = 12 A		46	57	nC
Gate-Source Charge	Q_{gs}			11.5		
Gate-Drain Charge	Q_{gd}			11.5		
Gate Resistance	R_g		0.2	0.85	1.2	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 30 Ω I_D ≅ 1.0 A, V_{GEN} = 10 V, R_g = 6 Ω		16	25	ns
Rise Time	t_r			12	18	
Turn-Off Delay Time	$t_{d(off)}$			50	75	
Fall Time	t_f			30	45	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = 3.0 A, di/dt = 100 A/μs		40	60	

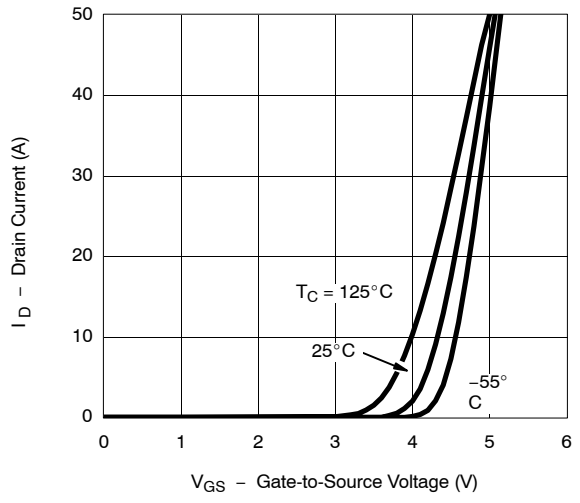
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

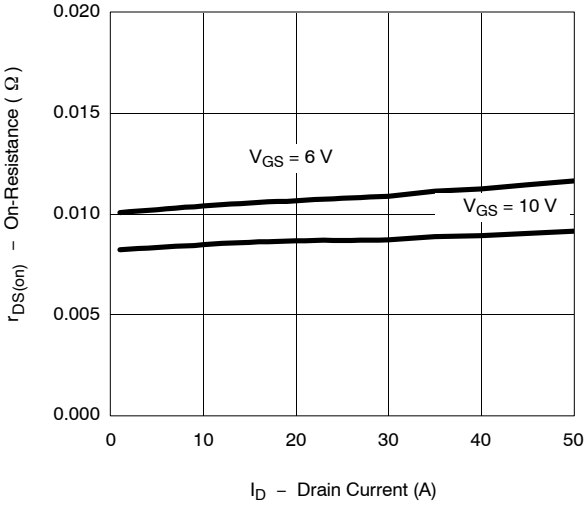


Transfer Characteristics

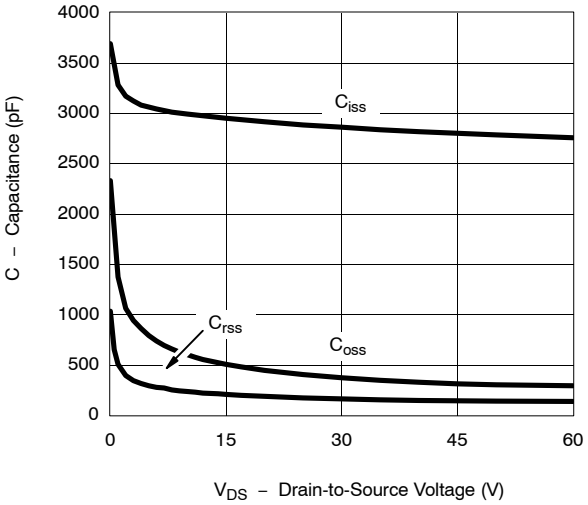


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

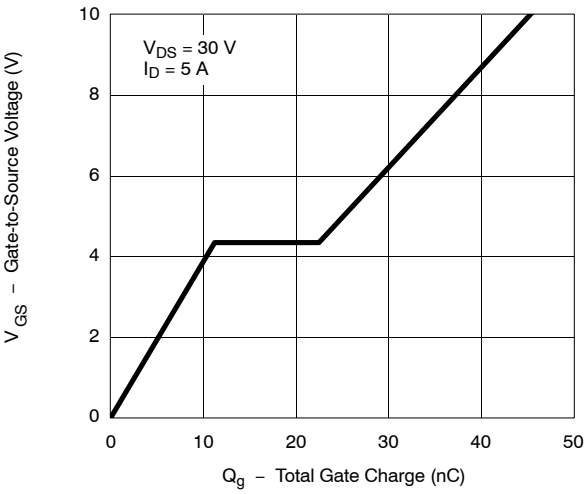
On-Resistance vs. Drain Current



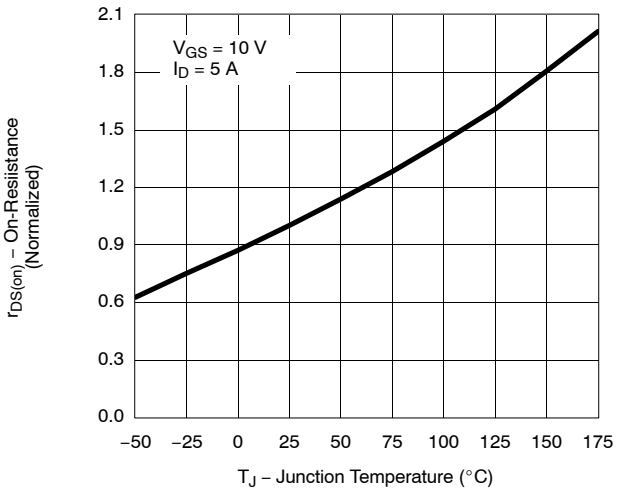
Capacitance



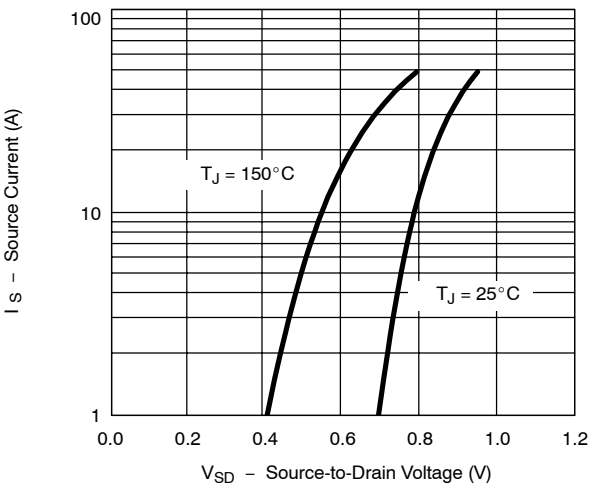
Gate Charge



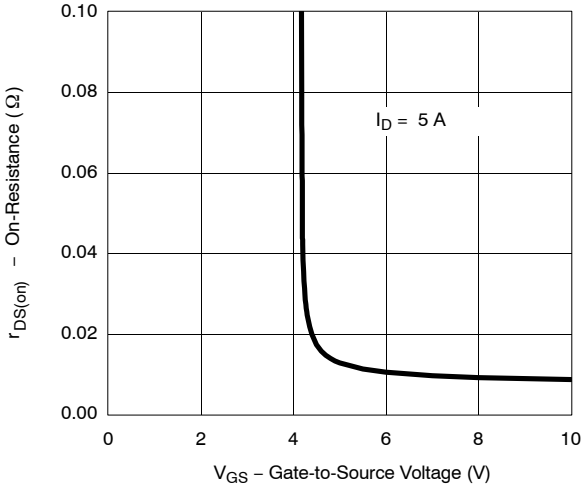
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

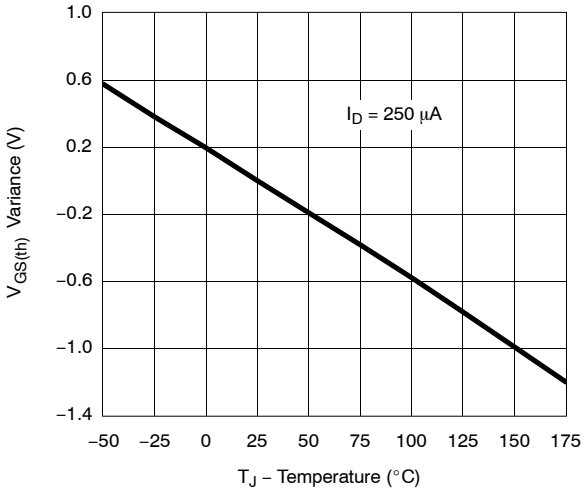


On-Resistance vs. Gate-to-Source Voltage

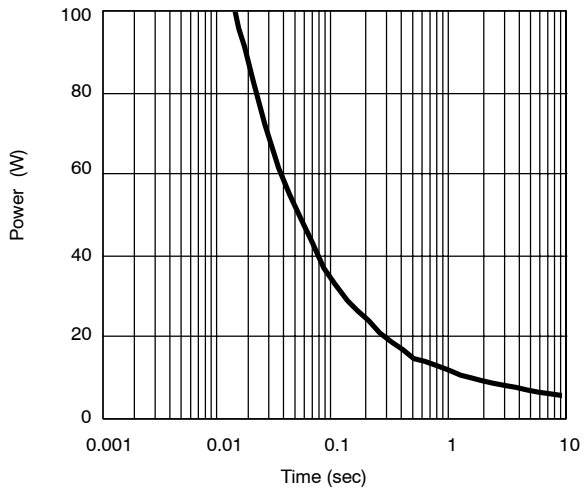


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

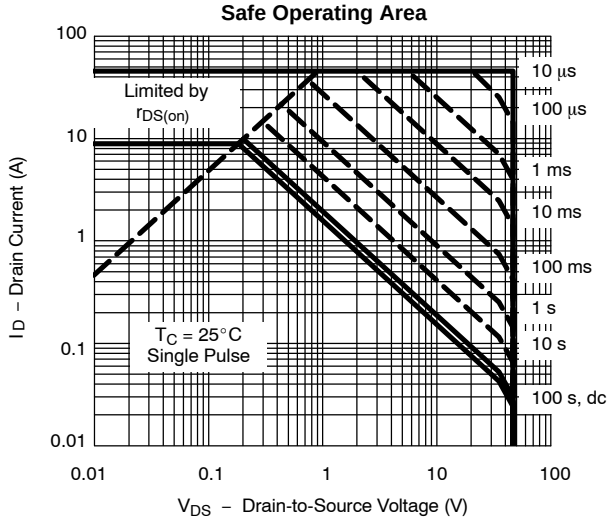
Threshold Voltage



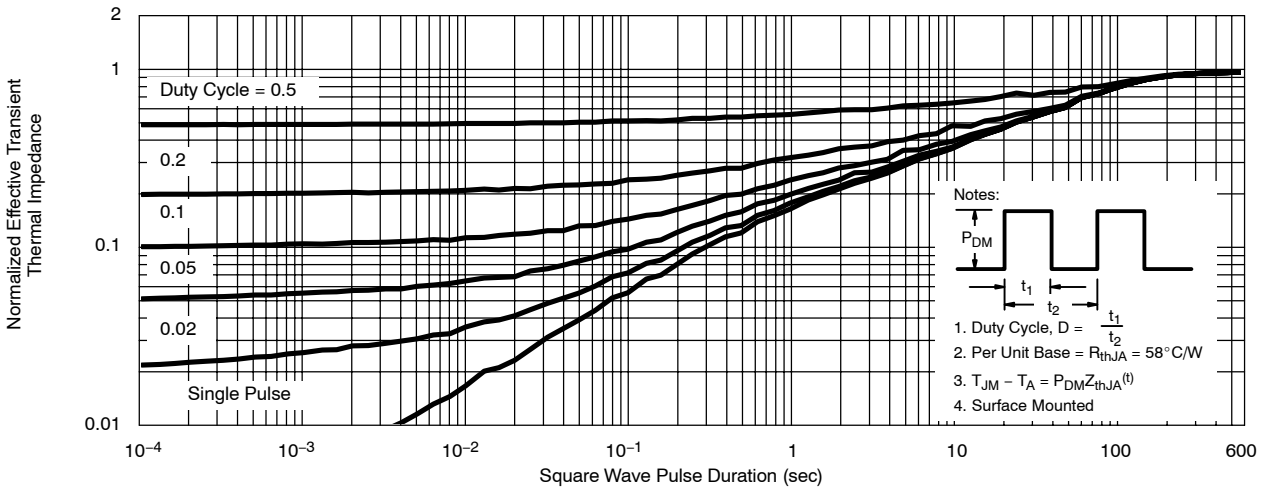
Single Pulse Power, Juncion-To-Ambient



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Case