



# DRAM

# 256K x 4 DRAM

## FAST PAGE MODE

### AVAILABLE AS MILITARY SPECIFICATION

- SMD 5962-90617
- MIL-STD-883

### FEATURES

- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- Optional FAST PAGE MODE access cycle
- Refresh modes:  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  and HIDDEN
- 512-cycle refresh distributed across 8ms
- Specifications guaranteed over full military temperature range (-55°C to +125°C)

### OPTIONS

- Timing
  - 80ns access
  - 100ns access
  - 120ns access

### MARKING

- Packages
 

|                       |    |         |
|-----------------------|----|---------|
| Ceramic DIP (300 mil) | C  | No. 103 |
| Ceramic LCC           | EC | No. 202 |

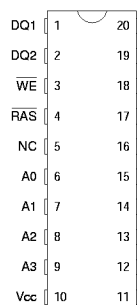
### GENERAL DESCRIPTION

The MT4C4256 883C is a randomly accessed solid-state memory containing 1,048,576 bits organized in a 262,144 x4 configuration. During READ or WRITE cycles, each 4-bit word is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time.  $\overline{\text{RAS}}$  is used to latch the first 9 bits and  $\overline{\text{CAS}}$  the latter 9 bits. A READ or WRITE cycle is selected with the  $\overline{\text{WE}}$  input. A logic HIGH on  $\overline{\text{WE}}$  dictates READ mode while a logic LOW on  $\overline{\text{WE}}$  dictates WRITE mode.

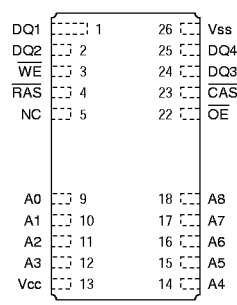
During a WRITE cycle, data in (D) is latched by the falling edge of  $\overline{\text{WE}}$  or  $\overline{\text{CAS}}$ , whichever occurs last. If  $\overline{\text{WE}}$  goes LOW prior to  $\overline{\text{CAS}}$  going LOW, the output pins (Qs) remain open (High-Z) until the next  $\overline{\text{CAS}}$  cycle. If  $\overline{\text{WE}}$  goes LOW after data reaches the outputs (Qs), the outputs are activated and retain the selected cells' data as long as  $\overline{\text{CAS}}$  remains LOW (regardless of  $\overline{\text{WE}}$  or  $\overline{\text{RAS}}$ ). This late  $\overline{\text{WE}}$  pulse results in a READ-WRITE cycle. The four data inputs and four data

### PIN ASSIGNMENT (Top View)

#### 20-Pin DIP (D-8)



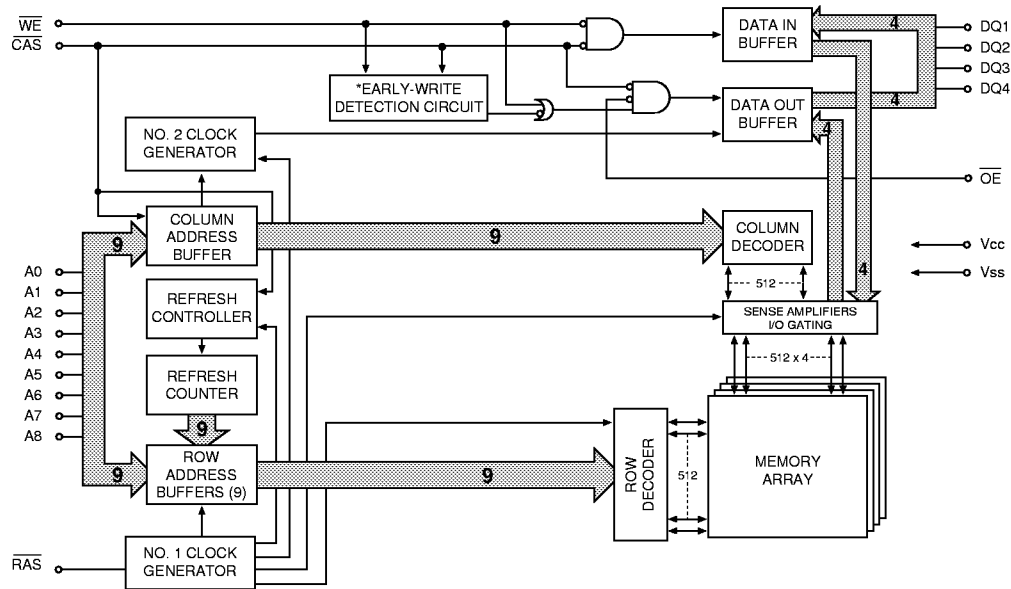
#### 20-Pin LCC



outputs are routed through four leads using common I/O, and information direction is controlled by  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$ .

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0-A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by  $\overline{\text{RAS}}$  followed by a column address strobed-in by  $\overline{\text{CAS}}$ .  $\overline{\text{CAS}}$  may be toggled-in by holding  $\overline{\text{RAS}}$  LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning  $\overline{\text{RAS}}$  HIGH terminates the FAST PAGE MODE operation.

Returning  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the  $\overline{\text{RAS}}$  high time. Memory cell data is retained in its correct state by maintaining power and executing any  $\overline{\text{RAS}}$  cycle (READ, WRITE,  $\overline{\text{RAS}}$ -ONLY,  $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ , or HIDDEN refresh) so that all 512 combinations of  $\overline{\text{RAS}}$  addresses (A0-A8) are executed at least every 8ms, regardless of sequence.

FUNCTIONAL BLOCK DIAGRAM  
FAST PAGE MODE

## TRUTH TABLE

| FUNCTION                      |           | RAS   | CAS | WE  | OE  | ADDRESSES |     | DATA IN/OUT       |
|-------------------------------|-----------|-------|-----|-----|-----|-----------|-----|-------------------|
|                               |           |       |     |     |     | 'R        | 'C  | DQ1-DQ4           |
| Standby                       |           | H     | H→X | X   | X   | X         | X   | High-Z            |
| READ                          |           | L     | L   | H   | L   | ROW       | COL | Data Out          |
| EARLY-WRITE                   |           | L     | L   | L   | X   | ROW       | COL | Data In           |
| READ-WRITE                    |           | L     | L   | H→L | L→H | ROW       | COL | Data Out, Data In |
| FAST-PAGE-MODE<br>READ        | 1st Cycle | L     | H→L | H   | L   | ROW       | COL | Data Out          |
|                               | 2nd Cycle | L     | H→L | H   | L   | n/a       | COL | Data Out          |
| FAST-PAGE-MODE<br>EARLY-WRITE | 1st Cycle | L     | H→L | L   | X   | ROW       | COL | Data In           |
|                               | 2nd Cycle | L     | H→L | L   | X   | n/a       | COL | Data In           |
| FAST-PAGE-MODE<br>READ-WRITE  | 1st Cycle | L     | H→L | H→L | L→H | ROW       | COL | Data Out, Data In |
|                               | 2nd Cycle | L     | H→L | H→L | L→H | n/a       | COL | Data Out, Data In |
| RAS-ONLY REFRESH              |           | L     | H   | X   | X   | ROW       | n/a | High-Z            |
| HIDDEN<br>REFRESH             | READ      | L→H→L | L   | H   | L   | ROW       | COL | Data Out          |
|                               | WRITE     | L→H→L | L   | L   | X   | ROW       | COL | Data In           |
| CAS-BEFORE-RAS REFRESH        |           | H→L   | L   | X   | X   | X         | X   | High-Z            |

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to V<sub>SS</sub> ..... -1.5V to +7.0V  
 Storage Temperature Range ..... -65°C to +150°C  
 Power Dissipation ..... 1W  
 Lead Temperature (Soldering 5 Seconds) ..... 270°C  
 Junction Temperature (T<sub>J</sub>) ..... +175°C  
 Short Circuit Output Current ..... 50mA

\*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC ELECTRICAL PERFORMANCE CHARACTERISTICS**

(Notes: 1, 6, 7) (-55°C ≤ T<sub>C</sub> ≤ +125°C; V<sub>CC</sub> = 5V ±10%)

| PARAMETER/CONDITION                                                                                     | SYMBOL          | MIN | MAX                  | UNITS | NOTES |
|---------------------------------------------------------------------------------------------------------|-----------------|-----|----------------------|-------|-------|
| Supply Voltage                                                                                          | V <sub>CC</sub> | 4.5 | 5.5                  | V     |       |
| Input High (Logic 1) Voltage, All Inputs                                                                | V <sub>IH</sub> | 2.4 | V <sub>CC</sub> + .5 | V     |       |
| Input Low (Logic 0) Voltage, All Inputs                                                                 | V <sub>IL</sub> | -.5 | 0.8                  | V     |       |
| INPUT LEAKAGE CURRENT<br>Any Input (0V ≤ V <sub>IN</sub> ≤ 6.5V),<br>All other pins not under test = 0V | I <sub>I</sub>  | -5  | 5                    | μA    |       |
| OUTPUT LEAKAGE CURRENT (Q is Disabled, 0V ≤ V <sub>OUT</sub> ≤ 6.5V)                                    | I <sub>OZ</sub> | -5  | 5                    | μA    |       |
| OUTPUT LEVELS<br>Output High Voltage (I <sub>OUT</sub> = -5mA)                                          | V <sub>OH</sub> | 2.4 |                      | V     |       |
| Output Low Voltage (I <sub>OUT</sub> = 4.2mA)                                                           | V <sub>OL</sub> |     | 0.4                  | V     |       |

| PARAMETER/CONDITION                                                                                                                                          | SYMBOL           | MAX |     |     | UNITS | NOTES |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|-----|-----|-----|-------|-------|
|                                                                                                                                                              |                  | -8  | -10 | -12 |       |       |
| STANDBY CURRENT: (TTL)<br>(RAS = CAS = V <sub>IH</sub> )                                                                                                     | I <sub>CC1</sub> | 3   | 3   | 3   | mA    |       |
| STANDBY CURRENT: (CMOS)<br>(RAS = CAS = V <sub>CC</sub> - 0.2V; all other inputs = V <sub>CC</sub> - 0.2V)                                                   | I <sub>CC2</sub> | 1   | 1   | 1   | mA    |       |
| OPERATING CURRENT: Random READ/WRITE<br>Average power supply current<br>(RAS, CAS, Address Cycling: t <sub>RC</sub> = t <sub>RC</sub> (MIN))                 | I <sub>CC3</sub> | 70  | 60  | 50  | mA    | 3, 4  |
| OPERATING CURRENT: FAST PAGE MODE<br>Average power supply current<br>(RAS = V <sub>IL</sub> , CAS, Address Cycling: t <sub>PC</sub> = t <sub>PC</sub> (MIN)) | I <sub>CC4</sub> | 50  | 40  | 30  | mA    | 3, 4  |
| REFRESH CURRENT: RAS-ONLY<br>Average power supply current<br>(RAS Cycling, CAS = V <sub>IH</sub> ; t <sub>RC</sub> = t <sub>RC</sub> (MIN))                  | I <sub>CC5</sub> | 70  | 60  | 50  | mA    | 3     |
| REFRESH CURRENT: CAS-BEFORE-RAS<br>Average power supply current<br>(RAS, CAS, Address Cycling: t <sub>RC</sub> = t <sub>RC</sub> (MIN))                      | I <sub>CC6</sub> | 70  | 60  | 50  | mA    | 3, 5  |



## CAPACITANCE

| PARAMETER                           | SYMBOL          | MIN | MAX | UNITS | NOTES |
|-------------------------------------|-----------------|-----|-----|-------|-------|
| Input Capacitance: (A0-A8), D       | C <sub>I1</sub> |     | 7   | pF    | 2     |
| Input Capacitance: RAS, CAS, WE, OE | C <sub>I2</sub> |     | 7   | pF    | 2     |
| Input/Output Capacitance: (DQ1-DQ4) | C <sub>O</sub>  |     | 8   | pF    | 2     |

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T<sub>C</sub> ≤ +125°C; V<sub>CC</sub> = 5V ± 10%)

| AC CHARACTERISTICS                           |                   | -8  |         | -10 |         | -12 |         |       |       |
|----------------------------------------------|-------------------|-----|---------|-----|---------|-----|---------|-------|-------|
| PARAMETER                                    | SYM               | MIN | MAX     | MIN | MAX     | MIN | MAX     | UNITS | NOTES |
| Random READ or WRITE cycle time              | t <sub>RC</sub>   | 150 |         | 180 |         | 210 |         | ns    |       |
| READ-WRITE cycle time                        | t <sub>RWC</sub>  | 195 |         | 235 |         | 275 |         | ns    |       |
| FAST-PAGE-MODE READ or WRITE cycle time      | t <sub>PC</sub>   | 45  |         | 55  |         | 65  |         | ns    |       |
| FAST-PAGE-MODE READ-WRITE cycle time         | t <sub>PRWC</sub> | 90  |         | 110 |         | 130 |         | ns    |       |
| Access time from RAS                         | t <sub>RAC</sub>  |     | 80      |     | 100     |     | 120     | ns    | 14    |
| Access time from CAS                         | t <sub>CAC</sub>  |     | 20      |     | 25      |     | 30      | ns    | 15    |
| Output Enable                                | t <sub>OE</sub>   |     | 20      |     | 25      |     | 30      | ns    | 23    |
| Access time from column address              | t <sub>AA</sub>   |     | 40      |     | 50      |     | 60      | ns    |       |
| Access time from CAS precharge               | t <sub>CPA</sub>  |     | 40      |     | 50      |     | 60      | ns    |       |
| RAS pulse width                              | t <sub>RAS</sub>  | 80  | 100,000 | 100 | 100,000 | 120 | 100,000 | ns    |       |
| RAS pulse width (FAST PAGE MODE)             | t <sub>RASP</sub> | 80  | 100,000 | 100 | 100,000 | 120 | 100,000 | ns    |       |
| RAS hold time                                | t <sub>RSH</sub>  | 20  |         | 25  |         | 30  |         | ns    |       |
| RAS precharge time                           | t <sub>RP</sub>   | 60  |         | 70  |         | 80  |         | ns    |       |
| CAS pulse width                              | t <sub>CAS</sub>  | 20  | 100,000 | 25  | 100,000 | 30  | 100,000 | ns    |       |
| CAS hold time                                | t <sub>CSH</sub>  | 80  |         | 100 |         | 120 |         | ns    |       |
| CAS precharge time                           | t <sub>CPN</sub>  | 10  |         | 12  |         | 15  |         | ns    | 16    |
| CAS precharge time (FAST PAGE MODE)          | t <sub>CP</sub>   | 10  |         | 12  |         | 15  |         | ns    |       |
| RAS to CAS delay time                        | t <sub>RCD</sub>  | 20  | 60      | 25  | 75      | 25  | 90      | ns    | 17    |
| CAS to RAS precharge time                    | t <sub>CRP</sub>  | 5   |         | 5   |         | 10  |         | ns    |       |
| Row address setup time                       | t <sub>ASR</sub>  | 0   |         | 0   |         | 0   |         | ns    |       |
| Row address hold time                        | t <sub>RAH</sub>  | 10  |         | 15  |         | 15  |         | ns    |       |
| RAS to column address delay time             | t <sub>RAD</sub>  | 15  | 40      | 20  | 50      | 20  | 60      | ns    | 18    |
| Column address setup time                    | t <sub>ASC</sub>  | 0   |         | 0   |         | 0   |         | ns    |       |
| Column address hold time                     | t <sub>CAH</sub>  | 15  |         | 20  |         | 20  |         | ns    |       |
| Column address hold time (referenced to RAS) | t <sub>AR</sub>   | 60  |         | 70  |         | 80  |         | ns    |       |
| Column address to RAS lead time              | t <sub>RAL</sub>  | 40  |         | 50  |         | 60  |         | ns    |       |
| Read command setup time                      | t <sub>RCS</sub>  | 0   |         | 0   |         | 0   |         | ns    |       |
| Read command hold time (referenced to CAS)   | t <sub>RCH</sub>  | 0   |         | 0   |         | 0   |         | ns    | 19    |
| Read command hold time (referenced to RAS)   | t <sub>RRH</sub>  | 0   |         | 0   |         | 0   |         | ns    | 19    |
| CAS to output in Low-Z                       | t <sub>CLZ</sub>  | 0   |         | 0   |         | 0   |         | ns    |       |

**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ( $-55^{\circ}\text{C} \leq T_{\text{C}} \leq +125^{\circ}\text{C}$ ;  $V_{\text{CC}} = 5\text{V} \pm 10\%$ )

| AC CHARACTERISTICS                                                                                        |                  | -8  |     | -10 |     | -12 |     |       |        |
|-----------------------------------------------------------------------------------------------------------|------------------|-----|-----|-----|-----|-----|-----|-------|--------|
| PARAMETER                                                                                                 | SYM              | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES  |
| Output buffer turn-off delay                                                                              | $t_{\text{OFF}}$ | 0   | 20  | 0   | 20  | 0   | 25  | ns    | 20, 26 |
| Output disable                                                                                            | $t_{\text{OD}}$  |     | 20  |     | 20  |     | 25  | ns    | 26     |
| $\overline{\text{WE}}$ command setup time                                                                 | $t_{\text{WCS}}$ | 0   |     | 0   |     | 0   |     | ns    | 21     |
| Write command hold time                                                                                   | $t_{\text{WCH}}$ | 15  |     | 20  |     | 25  |     | ns    |        |
| Write command hold time<br>(referenced to $\overline{\text{RAS}}$ )                                       | $t_{\text{WCR}}$ | 60  |     | 70  |     | 80  |     | ns    |        |
| Write command pulse width                                                                                 | $t_{\text{WP}}$  | 15  |     | 15  |     | 20  |     | ns    |        |
| Write command to $\overline{\text{RAS}}$ lead time                                                        | $t_{\text{RWL}}$ | 20  |     | 25  |     | 30  |     | ns    |        |
| Write command to $\overline{\text{CAS}}$ lead time                                                        | $t_{\text{CWL}}$ | 20  |     | 25  |     | 30  |     | ns    |        |
| Data-in setup time                                                                                        | $t_{\text{DS}}$  | 0   |     | 0   |     | 0   |     | ns    | 22     |
| Data-in hold time                                                                                         | $t_{\text{DH}}$  | 15  |     | 20  |     | 25  |     | ns    | 22     |
| Data-in hold time<br>(referenced to $\overline{\text{RAS}}$ )                                             | $t_{\text{DHR}}$ | 60  |     | 70  |     | 80  |     | ns    |        |
| $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time                                              | $t_{\text{RWD}}$ | 105 |     | 125 |     | 150 |     | ns    | 21     |
| Column address<br>to $\overline{\text{WE}}$ delay time                                                    | $t_{\text{AWD}}$ | 65  |     | 75  |     | 90  |     | ns    | 21     |
| $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time                                              | $t_{\text{CWD}}$ | 45  |     | 50  |     | 60  |     | ns    | 21     |
| Transition time (rise or fall)                                                                            | $t_{\text{T}}$   | 3   | 50  | 3   | 50  | 3   | 50  | ns    |        |
| Refresh period (512 cycles)                                                                               | $t_{\text{REF}}$ |     | 8   |     | 8   |     | 8   | ms    |        |
| $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time                                         | $t_{\text{RPC}}$ | 0   |     | 0   |     | 0   |     | ns    |        |
| $\overline{\text{CAS}}$ setup time<br>( $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh) | $t_{\text{CSR}}$ | 10  |     | 10  |     | 10  |     | ns    | 5      |
| $\overline{\text{CAS}}$ hold time<br>( $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ refresh)  | $t_{\text{CHR}}$ | 15  |     | 20  |     | 25  |     | ns    | 5      |
| $\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$ during<br>READ-MODIFY-WRITE cycle            | $t_{\text{OEH}}$ | 20  |     | 20  |     | 25  |     | ns    | 25     |
| $\overline{\text{OE}}$ setup prior to $\overline{\text{RAS}}$ during<br>HIDDEN REFRESH cycle              | $t_{\text{ORD}}$ | 0   |     | 0   |     | 0   |     | ns    | 24     |

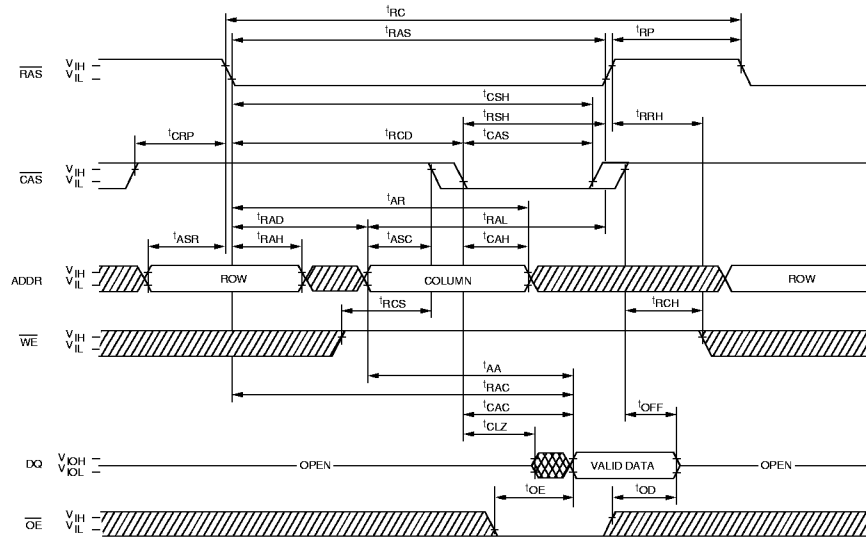


## NOTES

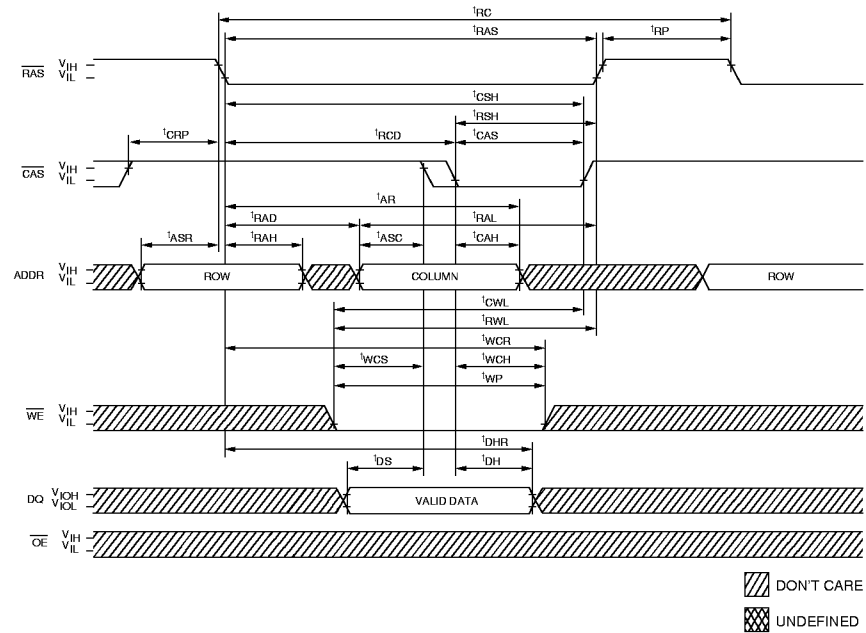
1. All voltages referenced to V<sub>SS</sub>.
2. This parameter is sampled. V<sub>CC</sub> = 5V ±10%, f = 1 MHz.
3. I<sub>CC</sub> is dependent on cycle rates.
4. I<sub>CC</sub> is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T<sub>C</sub> ≤ +125°C) is assured.
7. An initial pause of 100μs is required after power-up followed by any eight RAS cycles before proper device operation is assured. The eight RAS cycle wake-up should be repeated any time the tREF refresh requirement is exceeded.
8. AC characteristics assume tT = 5ns. This parameter is not measured.
9. V<sub>IH</sub> (MIN) and V<sub>IL</sub> (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>).
10. In addition to meeting the transition rate specification, all input signals must transit between V<sub>IH</sub> and V<sub>IL</sub> (or between V<sub>IL</sub> and V<sub>IH</sub>) in a monotonic manner.
11. If CAS = V<sub>IH</sub>, data outputs (DQs) are High-Z.
12. If CAS = V<sub>IL</sub>, data outputs (DQs) may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that tRCD < tRCD (MAX). If tRCD is greater than the maximum recommended value shown in this table, tRAC will increase by the amount that tRCD exceeds the value shown.
15. Assumes that tRCD ≥ tRCD (MAX).
16. If CAS is LOW at the falling edge of RAS, DQs will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, CAS must be pulsed HIGH for tCPN.
17. Operation within the tRCD (MAX) limit ensures that tRAC (MAX) can be met. tRCD (MAX) is specified as a reference point only; if tRCD is greater than the specified tRCD (MAX) limit, then access time is controlled exclusively by tCAC.
18. Operation within the tRAD (MAX) limit ensures that tRAC (MIN) and tCAC (MIN) can be met. tRAD (MAX) is specified as a reference point only; if tRAD is greater than the specified tRAD (MAX) limit, then access time is controlled exclusively by tAA.
19. Either tRCH or tRRH must be satisfied for a READ cycle.
20. tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V<sub>OH</sub> or V<sub>OL</sub>.
21. tWCS, tRWD, tAWD and tCWD are not restrictive operating parameters. tWCS applies to EARLY-WRITE cycles. tRWD, tAWD and tCWD apply to READ-MODIFY-WRITE cycles. If tWCS ≥ tWCS (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If tRWD ≥ tRWD (MIN), tAWD ≥ tAWD (MIN) and tCWD ≥ tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. OE held HIGH and WE taken LOW after CAS goes LOW results in a LATE-WRITE (OE controlled) cycle. tWCS, tRWD, tCWD and tAWD are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to CAS leading edge in EARLY-WRITE cycles and WE leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If OE is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE = LOW and OE = HIGH.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both tOD and tOE met (OE HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS remains LOW and OE is taken back LOW after tOE is met. If CAS goes HIGH prior to OE going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once tOD or tOFF occur. If CAS goes HIGH first, OE becomes a "don't care." If OE goes HIGH and CAS stays LOW, OE is not a "don't care;" and the DQs will provide the previously read data if OE is taken back LOW (while CAS remains LOW).



## READ CYCLE

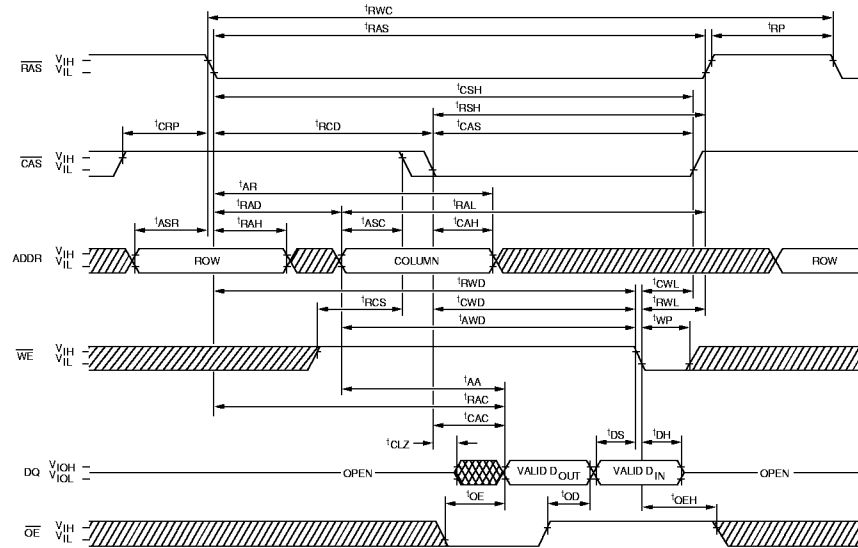


## EARLY-WRITE CYCLE

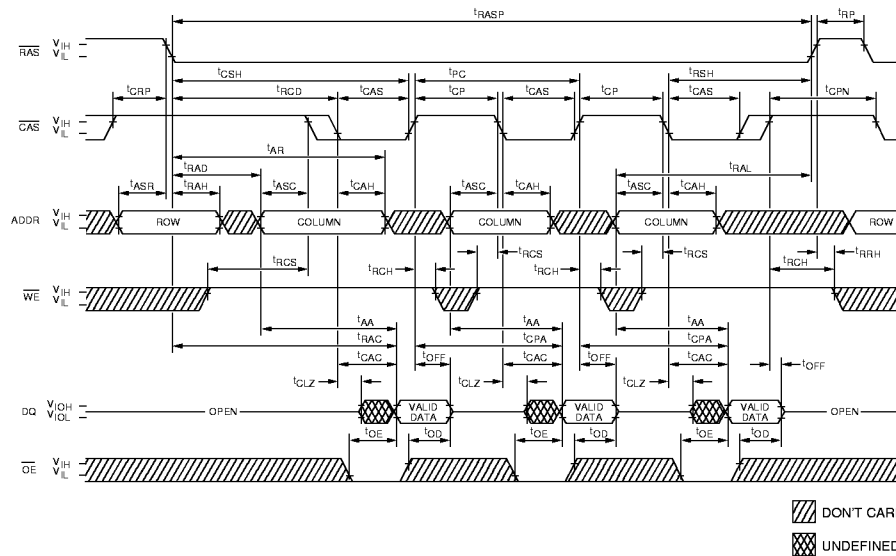


▨ DON'T CARE  
▩ UNDEFINED

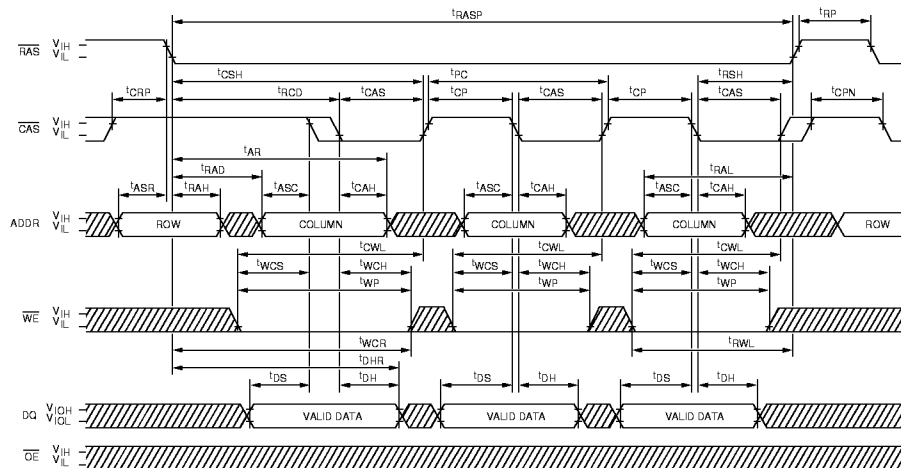
### READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



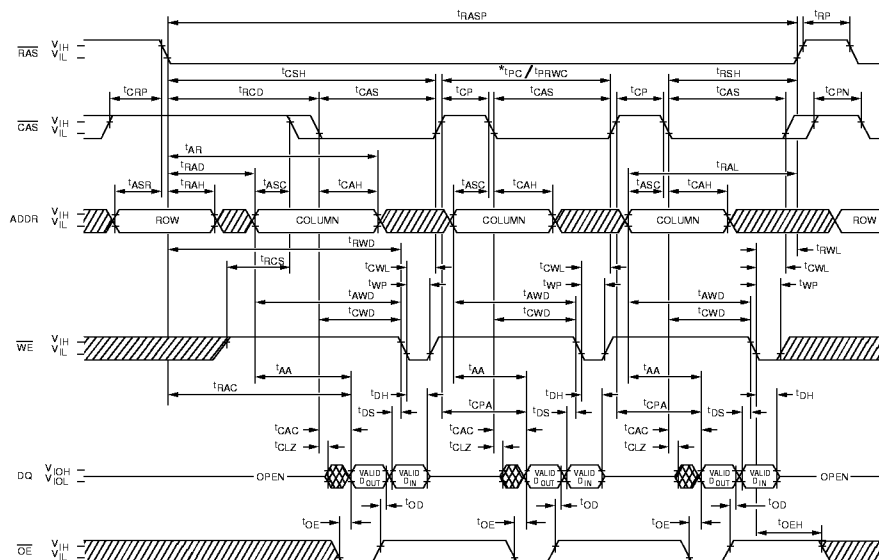
### FAST-PAGE-MODE READ CYCLE



### FAST-PAGE-MODE EARLY-WRITE CYCLE



### FAST-PAGE-MODE READ-WRITE CYCLE (LATE-WRITE and READ-MODIFY-WRITE CYCLES)



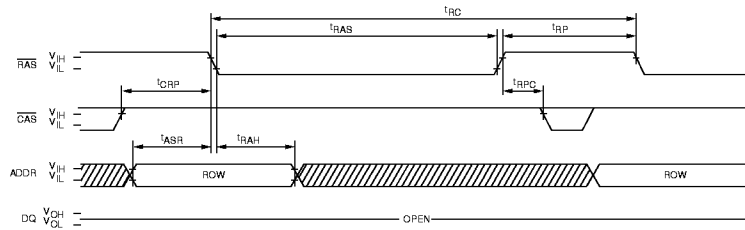
\*t<sub>PC</sub> = LATE-WRITE cycle  
t<sub>PRWC</sub> = FAST READ-MODIFY-WRITE cycle

 DON'T CARE

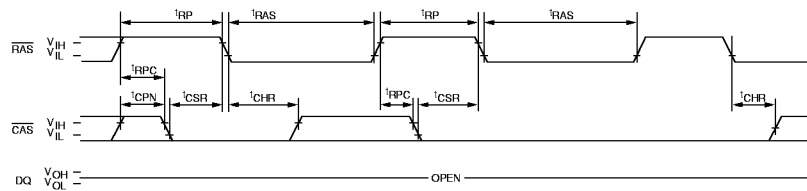
 UNDEFINED



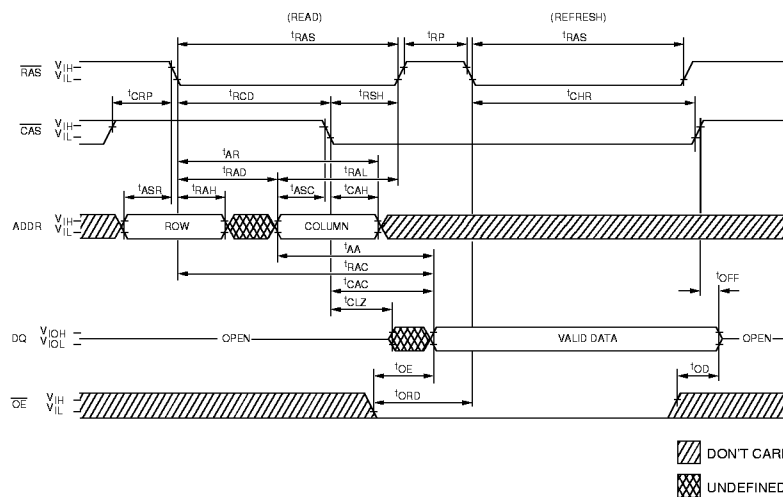
**$\overline{\text{RAS}}$ -ONLY REFRESH CYCLE**  
(ADDR = A0-A8;  $\overline{\text{WE}}$  = DON'T CARE)



**$\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$  REFRESH CYCLE**  
(A0-A8,  $\overline{\text{WE}}$  and  $\overline{\text{OE}}$  = DON'T CARE)



**HIDDEN REFRESH CYCLE <sup>24</sup>**  
( $\overline{\text{WE}}$  = HIGH,  $\overline{\text{OE}}$  = LOW)

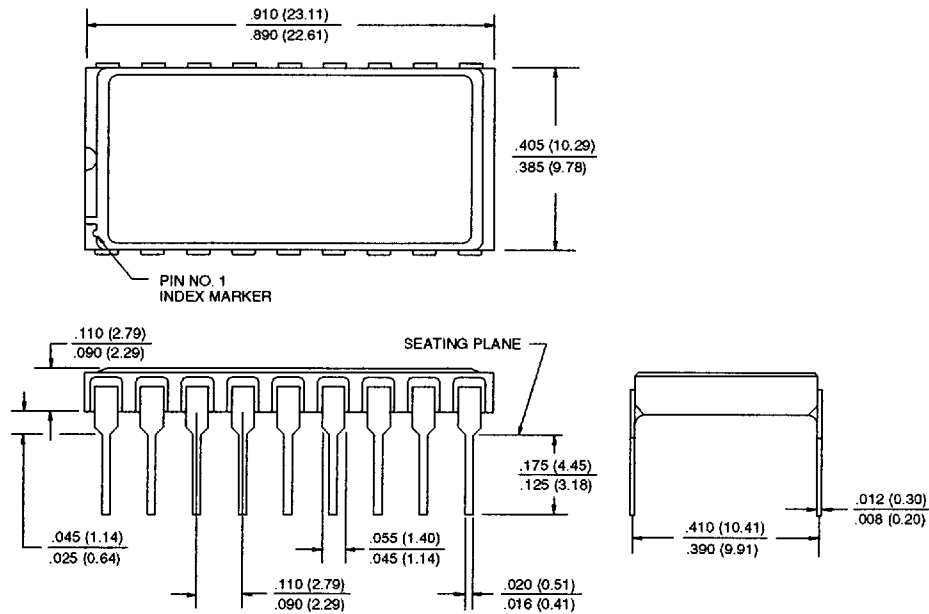
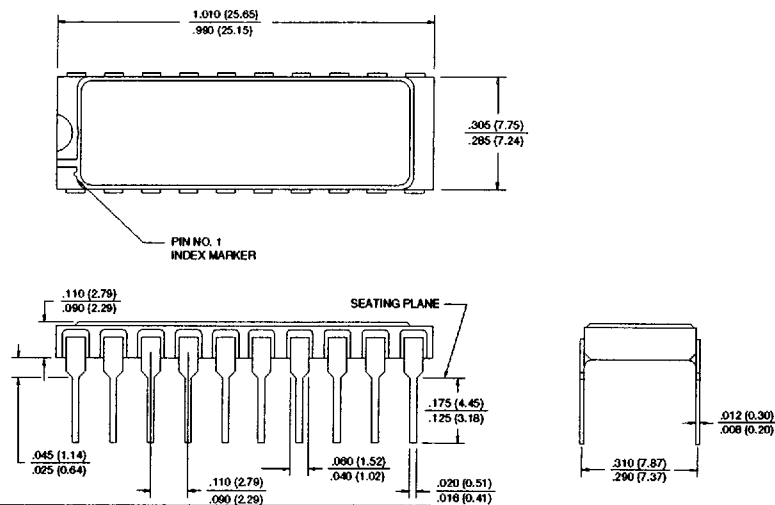


**ELECTRICAL TEST REQUIREMENTS**

| <b>MIL-STD-883 TEST REQUIREMENTS</b>                              | <b>SUBGROUPS<br/>(per Method 5005, Table I)</b> |
|-------------------------------------------------------------------|-------------------------------------------------|
| INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS<br>(Method 5004) | 2, 8A, 10                                       |
| FINAL ELECTRICAL TEST PARAMETERS<br>(Method 5004)                 | 1*, 2, 3, 7*, 8, 9, 10, 11                      |
| GROUP A TEST REQUIREMENTS<br>(Method 5005)                        | 1, 2, 3, 4**, 7, 8, 9, 10, 11                   |
| GROUP C AND D END-POINT ELECTRICAL PARAMETERS<br>(Method 5005)    | 1, 2, 3, 7, 8, 9, 10, 11                        |

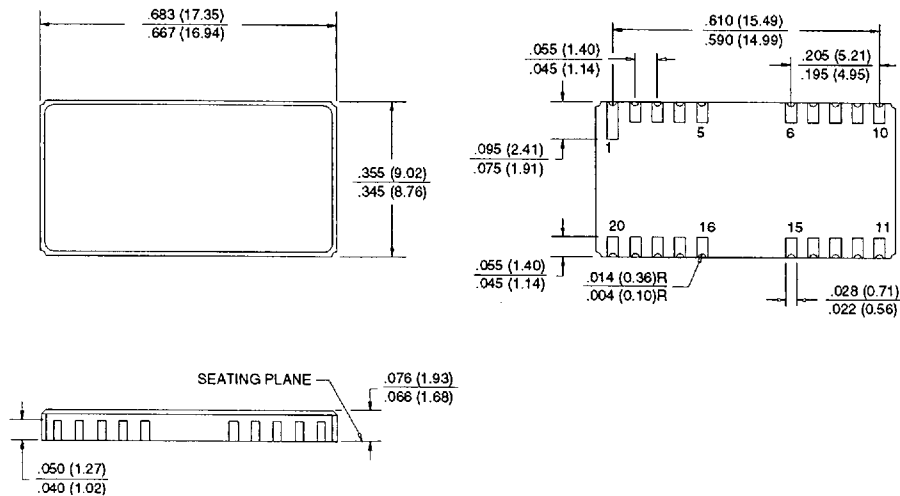
\* PDA applies to subgroups 1 and 7.

\*\* Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.

**PACKAGE No. 102  
18 CDIP (400 mils)****PACKAGE No. 103  
20 CDIP D-8 (300 mils)**



**PACKAGE No. 202**  
**20 CLCC**



**PACKAGE No. 203**  
**28 CLCC**

