

# SCAN921023 and SCAN921224 20-66 MHz 10 Bit Bus LVDS Serializer and Deserializer with IEEE 1149.1 (JTAG) and at-speed BIST

## General Description

The SCAN921023 transforms a 10-bit wide parallel LVCMOS/LVTTL data bus into a single high speed Bus LVDS serial data stream with embedded clock. The SCAN921224 receives the Bus LVDS serial data stream and transforms it back into a 10-bit wide parallel data bus and recovers parallel clock. Both devices are compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), Test Clock (TCK), and the optional Test Reset ( $\overline{\text{TRST}}$ ). IEEE 1149.1 features provide the designer or test engineer access to the backplane or cable interconnects and the ability to verify differential signal integrity to enhance their system test strategy. The pair of devices also features an at-speed BIST mode which allows the interconnects between the Serializer and Deserializer to be verified at-speed.

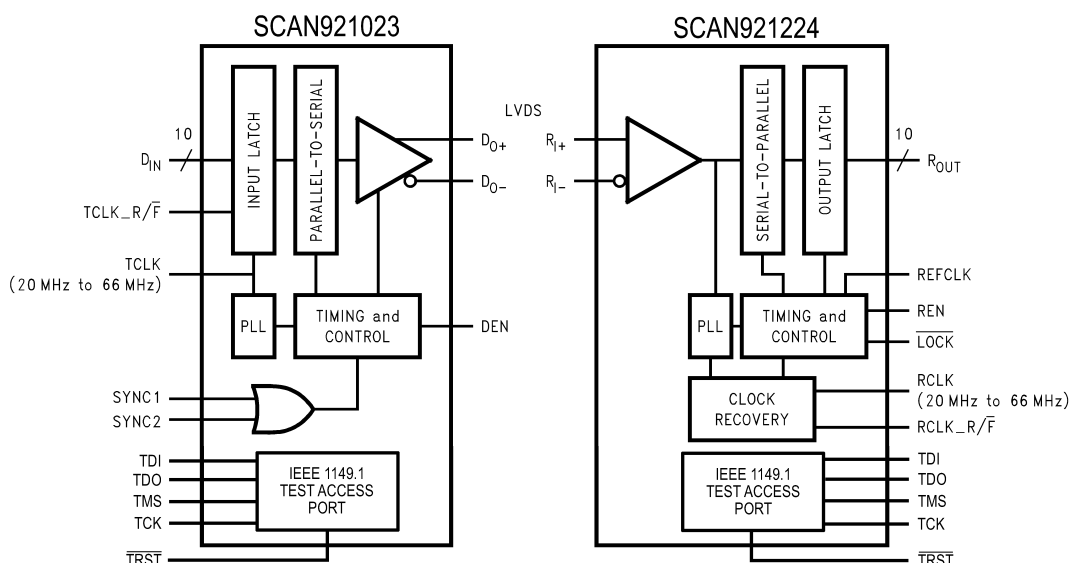
The SCAN921023 transmits data over backplanes or cable. The single differential pair data path makes PCB design easier. In addition, the reduced cable, PCB trace count, and connector size tremendously reduce cost. Since one output transmits clock and data bits serially, it eliminates clock-to-data and data-to-data skew. The powerdown pin saves power by reducing supply current when not using either device. Upon power up of the Serializer, you can choose to activate synchronization mode or allow the Deserializer to

use the synchronization-to-random-data feature. By using the synchronization mode, the Deserializer will establish lock to a signal within specified lock times. In addition, the embedded clock guarantees a transition on the bus every 12-bit cycle. This eliminates transmission errors due to charged cable conditions. Furthermore, you may put the SCAN921023 output pins into TRI-STATE to achieve a high impedance state. The PLL can lock to frequencies between 20 MHz and 66 MHz.

## Features

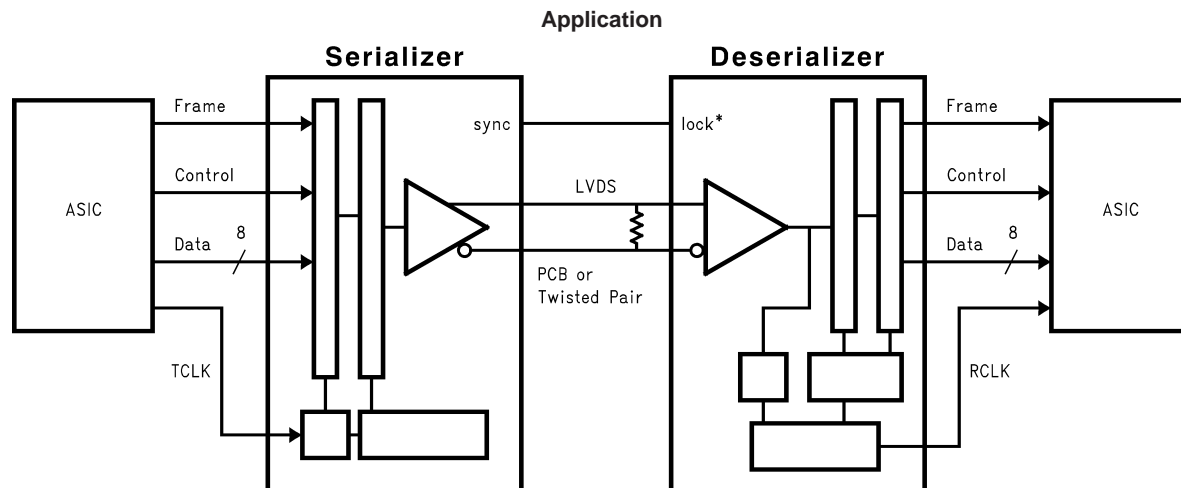
- IEEE 1149.1 (JTAG) Compliant and At-Speed BIST test mode.
- Clock recovery from PLL lock to random data patterns.
- Guaranteed transition every data transfer cycle
- Chipset (Tx + Rx) power consumption < 500 mW (typ) @ 66 MHz
- Single differential pair eliminates multi-channel skew
- Flow-through pinout for easy PCB layout
- 660 Mbps serial Bus LVDS data rate (at 66 MHz clock)
- 10-bit parallel interface for 1 byte data plus 2 control bits
- Synchronization mode and LOCK indicator
- Programmable edge trigger on clock
- High impedance on receiver inputs when power is off
- Bus LVDS serial output rated for 27 $\Omega$  load
- Small 49-lead BGA package

## Block Diagrams



DS200001-1

## Block Diagrams (Continued)



DS200001-2

## Functional Description

The SCAN921023 and SCAN921224 are a 10-bit Serializer and Deserializer chipset designed to transmit data over differential backplanes at clock speeds from 20 to 66 MHz. The chipset is also capable of driving data over Unshielded Twisted Pair (UTP) cable.

The chipset has three active states of operation: Initialization, Data Transfer, and Resynchronization; and two passive states: Powerdown and TRI-STATE. In addition to the active and passive states, there are also test modes for JTAG access and at-speed BIST.

The following sections describe each operation and passive state and the test modes.

## Initialization

Initialization of both devices must occur before data transmission begins. Initialization refers to synchronization of the Serializer and Deserializer PLL's to local clocks, which may be the same or separate. Afterwards, synchronization of the Deserializer to Serializer occurs.

**Step 1:** When you apply  $V_{CC}$  to both Serializer and/or Deserializer, the respective outputs enter TRI-STATE, and on-chip power-on circuitry disables internal circuitry. When  $V_{CC}$  reaches  $V_{CCOK}$  (2.5V) the PLL in each device begins locking to a local clock. For the Serializer, the local clock is the transmit clock (TCLK) provided by the source ASIC or other device. For the Deserializer, you must apply a local clock to the REFCLK pin.

The Serializer outputs remain in TRI-STATE while the PLL locks to the TCLK. After locking to TCLK, the Serializer is now ready to send data or SYNC patterns, depending on the levels of the SYNC1 and SYNC2 inputs or a data stream. The SYNC pattern sent by the Serializer consists of six ones and six zeros switching at the input clock rate.

Note that the Deserializer  $\overline{LOCK}$  output will remain high while its PLL locks to the incoming data or to SYNC patterns on the input.

**Step 2:** The Deserializer PLL must synchronize to the Serializer to complete initialization. The Deserializer will lock to non-repetitive data patterns. However, the transmission of SYNC patterns enables the Deserializer to lock to the Serializer signal within a specified time. See Figure 9.

The user's application determines control of the SYNC1 and SYNC 2 pins. One recommendation is a direct feedback loop from the  $\overline{LOCK}$  pin. Under all circumstances, the Serializer stops sending SYNC patterns after both SYNC inputs return low.

When the Deserializer detects edge transitions at the Bus LVDS input, it will attempt to lock to the embedded clock information. When the Deserializer locks to the Bus LVDS clock, the  $\overline{LOCK}$  output will go low. When  $\overline{LOCK}$  is low, the Deserializer outputs represent incoming Bus LVDS data.

## Data Transfer

After initialization, the Serializer will accept data from inputs DIN0–DIN9. The Serializer uses the TCLK input to latch incoming Data. The TCLK\_R/F pin selects which edge the Serializer uses to strobe incoming data. TCLK\_R/F high selects the rising edge for clocking data and low selects the falling edge. If either of the SYNC inputs is high for  $5 \times \text{TCLK}$  cycles, the data at DIN0–DIN9 is ignored regardless of clock edge.

After determining which clock edge to use, a start and stop bit, appended internally, frame the data bits in the register. The start bit is always high and the stop bit is always low. The start and stop bits function as the embedded clock bits in the serial stream.

The Serializer transmits serialized data and clock bits (10+2 bits) from the serial data output (DO±) at 12 times the TCLK frequency. For example, if TCLK is 66 MHz, the serial rate is  $66 \times 12 = 792$  Mega-bits-per-second. Since only 10 bits are from input data, the serial "payload" rate is 10 times the TCLK frequency. For instance, if TCLK = 66 MHz, the payload data rate is  $66 \times 10 = 660$  Mbps. The data source provides TCLK and must be in the range of 20 MHz to 66 MHz nominal.

The Serializer outputs (DO±) can drive a point-to-point connection or in limited multi-point or multi-drop backplanes. The outputs transmit data when the enable pin (DEN) is high, PWRDN = high, and SYNC1 and SYNC2 are low. When DEN is driven low, the Serializer output pins will enter TRI-STATE.

When the Deserializer synchronizes to the Serializer, the  $\overline{LOCK}$  pin is low. The Deserializer locks to the embedded

## Data Transfer (Continued)

clock and uses it to recover the serialized data. ROUT data is valid when  $\overline{\text{LOCK}}$  is low. Otherwise ROUT0–ROUT9 is invalid.

The ROUT0–ROUT9 pins use the RCLK pin as the reference to data. The polarity of the RCLK edge is controlled by the RCLK\_R/ $\overline{\text{F}}$  input. See Figure 13.

ROUT(0-9),  $\overline{\text{LOCK}}$  and RCLK outputs will drive a maximum of three CMOS input gates (15 pF load) with a 66 MHz clock.

## Resynchronization

When the Deserializer PLL locks to the embedded clock edge, the Deserializer  $\overline{\text{LOCK}}$  pin asserts a low. If the Deserializer loses lock, the  $\overline{\text{LOCK}}$  pin output will go high and the outputs (including RCLK) will enter TRI-STATE.

The user's system monitors the  $\overline{\text{LOCK}}$  pin to detect a loss of synchronization. Upon detection, the system can arrange to pulse the Serializer SYNC1 or SYNC2 pin to resynchronize. Multiple resynchronization approaches are possible. One recommendation is to provide a feedback loop using the  $\overline{\text{LOCK}}$  pin itself to control the sync request of the Serializer (SYNC1 or SYNC2). Dual SYNC pins are provided for multiple control in a multi-drop application. Sending sync patterns for resynchronization is desirable when lock times within a specific time are critical. However, the Deserializer can lock to random data, which is discussed in the next section.

## Random Lock Initialization and Resynchronization

The initialization and resynchronization methods described in their respective sections are the fastest ways to establish the link between the Serializer and Deserializer. However, the SCAN921224 can attain lock to a data stream without requiring the Serializer to send special SYNC patterns. This allows the SCAN921224 to operate in "open-loop" applications. Equally important is the Deserializer's ability to support hot insertion into a running backplane. In the open loop or hot insertion case, we assume the data stream is essentially random. Therefore, because lock time varies due to data stream characteristics, we cannot possibly predict exact lock time. However, please see Table 1 for some general random lock times under specific conditions. The primary constraint on the "random" lock time is the initial phase relation between the incoming data and the REFCLK when the Deserializer powers up. As described in the next paragraph, the data contained in the data stream can also affect lock time.

If a specific pattern is repetitive, the Deserializer could enter "false lock" - falsely recognizing the data pattern as the clocking bits. We refer to such a pattern as a repetitive multi-transition, RMT. This occurs when more than one Low-High transition takes place in a clock cycle over multiple cycles. This occurs when any bit, except DIN 9, is held at a low state and the adjacent bit is held high, creating a 0-1 transition. In the worst case, the Deserializer could become locked to the data pattern rather than the clock. Circuitry within the SCAN921224 can detect that the possibility of "false lock" exists. The circuitry accomplishes this by detecting more than one potential position for clocking bits. Upon detection, the circuitry will prevent the  $\overline{\text{LOCK}}$  output from becoming active until the potential "false lock" pattern changes. The false lock detect circuitry expects the data will eventually change, causing the Deserializer to lose lock to the data pattern and then continue searching for clock bits in

the serial data stream. Graphical representations of RMT are shown in Figure 1. Please note that RMT only applies to bits DIN0–DIN8.

## Powerdown

When no data transfer occurs, you can use the Powerdown state. The Serializer and Deserializer use the Powerdown state, a low power sleep mode, to reduce power consumption. The Deserializer enters Powerdown when you drive  $\overline{\text{PWRDN}}$  and REN low. The Serializer enters Powerdown when you drive  $\overline{\text{PWRDN}}$  low. In Powerdown, the PLL stops and the outputs enter TRI-STATE, which disables load current and reduces supply current to the milliampere range. To exit Powerdown, you must drive the  $\overline{\text{PWRDN}}$  pin high.

Before valid data exchanges between the Serializer and Deserializer, you must reinitialize and resynchronize the devices to each other. Initialization of the Serializer takes 510 TCLK cycles. The Deserializer will initialize and assert  $\overline{\text{LOCK}}$  high until lock to the Bus LVDS clock occurs.

## TRI-STATE

The Serializer enters TRI-STATE when the DEN pin is driven low. This puts both driver output pins (DO+ and DO–) into TRI-STATE. When you drive DEN high, the Serializer returns to the previous state, as long as all other control pins remain static (SYNC1, SYNC2,  $\overline{\text{PWRDN}}$ , TCLK\_R/ $\overline{\text{F}}$ ).

When you drive the REN pin low, the Deserializer enters TRI-STATE. Consequently, the receiver output pins (ROUT0–ROUT9) and RCLK will enter TRI-STATE. The  $\overline{\text{LOCK}}$  output remains active, reflecting the state of the PLL.

TABLE 1.

Random Lock Times for the SCAN921224		
	66 MHz	Units
Maximum	18	$\mu\text{S}$
Mean	3.0	$\mu\text{S}$
Minimum	0.43	$\mu\text{S}$
Conditions:	PRBS 2 <sup>15</sup> , V <sub>CC</sub> = 3.3V	

1) Difference in lock times are due to different starting points in the data pattern with multiple parts.

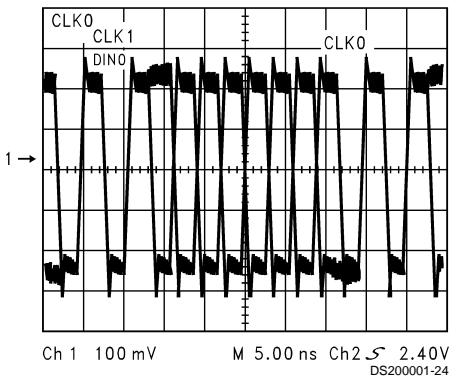
## Test Modes

In addition to the IEEE 1149.1 test access to the digital TTL pins, the SCAN921023 and SCAN921224 have two instructions to test the LVDS interconnects. The first is EXTEST. This is implemented at LVDS levels and is only intended as a go no-go test (e.g. missing cables). The second method is the RUNBIST instruction. It is an "at-system-speed" interconnect test. It is executed in approximately 33mS with a system clock speed of 66MHz. There are two bits in the RX BIST data register for notification of PASS/FAIL and TEST\_COMPLETE. Pass indicates that the BER (Bit-Error-Rate) is better than 10<sup>-7</sup>.

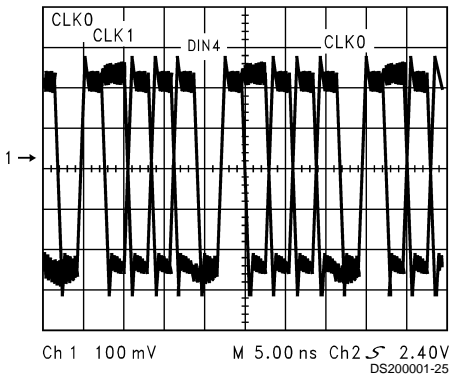
An important detail is that once both devices have the RUNBIST instruction loaded into their respective instruction registers, both devices must move into the RTI state within 4K system clocks (At a SCLK of 66Mhz and TCK of 1MHz this allows for 66 TCK cycles). This is not a concern when both devices are on the same scan chain or LSP, however, it can be a problem with some multi-drop devices. This test mode has been simulated and verified using National's SCANSTA111.

# Ordering Information

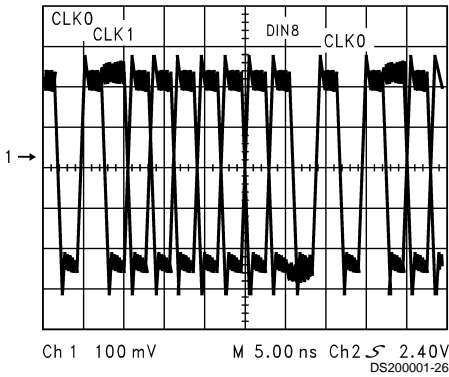
NSID	Function	Package
SCAN921023SLC	Serializer	SLC49a
SCAN921224SLC	Deserializer	SLC49a



DIN0 Held Low-DIN1 Held High Creates an RMT Pattern



DIN4 Held Low-DIN5 Held High Creates an RMT Pattern



DIN8 Held Low-DIN9 Held High Creates an RMT Pattern

FIGURE 1. RMT Patterns Seen on the Bus LVDS Serial Output

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	–0.3V to +4V
LVC MOS/LVTTL Input Voltage	–0.3V to ( $V_{CC}$ +0.3V)
LVC MOS/LVTTL Output Voltage	–0.3V to ( $V_{CC}$ +0.3V)
Bus LVDS Receiver Input Voltage	–0.3V to +3.9V
Bus LVDS Driver Output Voltage	–0.3V to +3.9V
Bus LVDS Output Short Circuit Duration	10mS
Junction Temperature	+150°C
Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 4 seconds)	+260°C
Maximum Package Power Dissipation Capacity @ 25°C Package:	
49L BGA	1.47 W

Package Derating:

49L BGA

$\theta_{ja}$

ESD Rating

HBM

MM

11.8 mW/°C above +25°C  
85°C/W

>2kV

250V

## Recommended Operating Conditions

	Min	Nom	Max	Units
Supply Voltage ( $V_{CC}$ )	3.0	3.3	3.6	V
Operating Free Air Temperature ( $T_A$ )	–40	+25	+85	°C
Receiver Input Range	0		2.4	V
Supply Noise Voltage ( $V_{CC}$ )			100 mV <sub>P-P</sub>	

## Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>SERIALIZER LVC MOS/LVTTL DC SPECIFICATIONS (apply to DIN0-9, TCLK, PWRDN, TCLK_R/F, SYNC1, SYNC2, DEN)</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA		–0.86	–1.5	V
$I_{IN}$	Input Current	$V_{IN} = 0V$ or 3.6V	–10	±1	+10	µA
<b>DESERIALIZER LVC MOS/LVTTL DC SPECIFICATIONS (apply to pins PWRDN, RCLK_R/F, REN, REFCLK = inputs; apply to pins ROUT, RCLK, LOCK = outputs)</b>						
$V_{IH}$	High Level Input Voltage		2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage		GND		0.8	V
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18$ mA		–0.62	–1.5	V
$I_{IN}$	Input Current	$V_{IN} = 0V$ or 3.6V	–10	±1	+15	µA
$I_{ILR}$	Input Current, TMS, TDI, TRST inputs	$V_{IN} = 0V$ or 3.6V	–20	–10		µA
$V_{OH}$	High Level Output Voltage	$I_{OH} = -9$ mA	2.2	3.0	$V_{CC}$	V
$V_{OL}$	Low Level Output Voltage	$I_{OL} = 9$ mA	GND	0.25	0.5	V
$I_{OS}$	Output Short Circuit Current	$V_{OUT} = 0V$	–15	–47	–85	mA
$I_{OS}$	Output Short Circuit Current, TDO output		–15	–70	–100	mA
$I_{OZ}$	TRI-STATE Output Current	$\overline{PWRDN}$ or REN = 0.8V, $V_{OUT} = 0V$ or VCC	–10	±0.1	+10	µA
<b>SERIALIZER Bus LVDS DC SPECIFICATIONS (apply to pins DO+ and DO–)</b>						
$V_{OD}$	Output Differential Voltage (DO+)–(DO–)	RL = 27Ω, Figure 18	200	290		mV
$\Delta V_{OD}$	Output Differential Voltage Unbalance				35	mV
$V_{OS}$	Offset Voltage		1.05	1.1	1.3	V
$\Delta V_{OS}$	Offset Voltage Unbalance			4.8	35	mV
$I_{OS}$	Output Short Circuit Current	DO = 0V, DIN = High, $\overline{PWRDN}$ and DEN = 2.4V		–56	–90	mA
$I_{OZ}$	TRI-STATE Output Current	$\overline{PWRDN}$ or DEN = 0.8V, DO = 0V or VCC	–10	±1	+10	µA
$I_{OX}$	Power-Off Output Current	VCC = 0V, DO=0V or 3.6V	–20	±1	+25	µA

## Electrical Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
DESERIALIZER Bus LVDS DC SPECIFICATIONS (apply to pins RI+ and RI-)							
VTH	Differential Threshold High Voltage	VCM = +1.1V		+6	+50	mV	
VTL	Differential Threshold Low Voltage		-50	-12		mV	
IIN	Input Current	VIN = +2.4V, VCC = 3.6V or 0V	-10	±1	+15	µA	
		VIN = 0V, VCC = 3.6V or 0V	-10	±0.05	+10	µA	
SERIALIZER SUPPLY CURRENT (apply to pins DVCC and AVCC)							
ICCD	Serializer Supply Current	RL = 27Ω	f = 20 MHz		47	60	mA
	Worst Case	Figure 2	f = 66 MHz		75	90	mA
ICCXD	Serializer Supply Current Powerdown	PWRDN = 0.8V			47	500	µA
DESERIALIZER SUPPLY CURRENT (apply to pins DVCC and AVCC)							
ICCR	Deserializer Supply Current	CL = 15 pF	f = 20 MHz		58	75	mA
	Worst Case	Figure 3	f = 66 MHz		110	130	mA
ICCXR	Deserializer Supply Current Powerdown	PWRDN = 0.8V, REN = 0.8V			0.36	1.0	mA

## Serializer Timing Requirements for TCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>TCP</sub>	Transmit Clock Period		15.15	T	50.0	nS
t <sub>TCIH</sub>	Transmit Clock High Time		0.4T	0.5T	0.6T	nS
t <sub>TCIL</sub>	Transmit Clock Low Time		0.4T	0.5T	0.6T	nS
t <sub>CLKT</sub>	TCLK Input Transition Time			3	6	nS
t <sub>JIT</sub>	TCLK Input Jitter	Figure 17			150	pS (RMS)

## Serializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>LLHT</sub>	Bus LVDS Low-to-High Transition Time	R <sub>L</sub> = 27Ω C <sub>L</sub> = 10pF to GND Figure 4 (Note 4)		0.2	0.4	nS
t <sub>LHLT</sub>	Bus LVDS High-to-Low Transition Time			0.25	0.4	nS
t <sub>DIS</sub>	DIN (0-9) Setup to TCLK	R <sub>L</sub> = 27Ω, C <sub>L</sub> = 10pF to GND Figure 7	0			nS
t <sub>DIH</sub>	DIN (0-9) Hold from TCLK		4.0			nS
t <sub>HZD</sub>	DO ± HIGH to TRI-STATE Delay	R <sub>L</sub> = 27Ω, C <sub>L</sub> = 10pF to GND Figure 8 (Note 5)		3	10	nS
t <sub>LZD</sub>	DO ± LOW to TRI-STATE Delay			3	10	nS
t <sub>ZHD</sub>	DO ± TRI-STATE to HIGH Delay			5	10	nS
t <sub>ZLD</sub>	DO ± TRI-STATE to LOW Delay			6.5	10	nS
t <sub>SPW</sub>	SYNC Pulse Width	R <sub>L</sub> = 27Ω Figure 10	5*t <sub>TCP</sub>			nS
t <sub>PLD</sub>	Serializer PLL Lock Time		510*t <sub>TCP</sub>		513*t <sub>TCP</sub>	nS
t <sub>SD</sub>	Serializer Delay	R <sub>L</sub> = 27Ω, Figure 11	t <sub>TCP</sub> + 1.0	t <sub>TCP</sub> + 2.5	t <sub>TCP</sub> + 3.5	nS



## Serializer Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t <sub>DJIT</sub>	Deterministic Jitter	R <sub>L</sub> = 27Ω, C <sub>L</sub> =10pF to GND, (Note 6)	20 MHz	-300	-135	35	pS
			66 MHz	-245	-40	160	pS
t <sub>RJIT</sub>	Random Jitter	R <sub>L</sub> = 27Ω, C <sub>L</sub> =10pF to GND			19	25	pS (RMS)

## Deserializer Timing Requirements for REFCLK

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{RFCP}$	REFCLK Period		15.15	T	50	nS
$t_{RFDC}$	REFCLK Duty Cycle		30	50	70	%
$t_{RFCP} / t_{TCP}$	Ratio of REFCLK to TCLK		95	1	105	
$t_{RFTT}$	REFCLK Transition Time			3	6	nS

## Deserializer Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units	
t <sub>RCP</sub>	Receiver out Clock Period	t <sub>RCP</sub> = t <sub>TCP</sub> Figure 11	RCLK	15.15		50	nS	
t <sub>CLH</sub>	CMOS/TTL Low-to-High Transition Time	CL = 15 pF Figure 5	Rout(0-9), LOCK, RCLK		1.2	4	nS	
t <sub>CHL</sub>	CMOS/TTL High-to-Low Transition Time				1.1	4	nS	
t <sub>DD</sub>	Deserializer Delay Figure 12	All Temp./ All Freq.		1.75*t <sub>RCP</sub> +1.25	1.75*t <sub>RCP</sub> +5.0	1.75*t <sub>RCP</sub> +7.5	nS	
		Room Temp./3.3V/20MHz		1.75*t <sub>RCP</sub> +2.25	1.75*t <sub>RCP</sub> +5.0	1.75*t <sub>RCP</sub> +6.5	nS	
		Room Temp./3.3V/66MHz		1.75*t <sub>RCP</sub> +2.25	1.75*t <sub>RCP</sub> +5.0	1.75*t <sub>RCP</sub> +6.5	nS	
t <sub>ROS</sub>	ROUT Data Valid before RCLK	Figure 13	RCLK 20MHz	0.4*t <sub>RCP</sub>	0.5*t <sub>RCP</sub>		nS	
			RCLK 66MHz	0.38*t <sub>RCP</sub>	0.5*t <sub>RCP</sub>		nS	
t <sub>ROH</sub>	ROUT Data valid after RCLK	Figure 13	20MHz	-0.4*t <sub>RCP</sub>	-0.5*t <sub>RCP</sub>		nS	
			66MHz	-0.38*t <sub>RCP</sub>	-0.5*t <sub>RCP</sub>		nS	
t <sub>RDC</sub>	RCLK Duty Cycle			45	50	55	%	
t <sub>HZR</sub>	HIGH to TRI-STATE Delay	Figure 14	Rout(0-9)		2.8	10	nS	
t <sub>LZR</sub>	LOW to TRI-STATE Delay				2.8	10	nS	
t <sub>ZHR</sub>	TRI-STATE to HIGH Delay				4.2	10	nS	
t <sub>ZLR</sub>	TRI-STATE to LOW Delay				4.2	10	nS	
t <sub>DSR1</sub>	Deserializer PLL Lock Time from PWRDWN (with SYNCPAT)			Figure 15 Figure 16 (Note 7)	20MHz		2.6	4
		66MHz			0.84	3	μS	
t <sub>DSR2</sub>	Deserializer PLL Lock time from SYNCPAT	20MHz			1	2	μS	
		66MHz			0.29	0.8	μS	
t <sub>ZHLK</sub>	TRI-STATE to HIGH Delay (power-up)		LOCK			3.7	12	nS

## Deserializer Switching Characteristics (Continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
$t_{\text{RNM}}$	Deserializer Noise Margin	Figure 17 (Note 8)	20 MHz	1.0	1.6		nS
			66 MHz	250	400		pS

## SCAN Circuitry Timing Requirements

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$f_{\text{MAX}}$	Maximum TCK Clock Frequency	$R_L = 500\Omega$ , $C_L = 35 \text{ pF}$	25.0	50.0		MHz
$t_{\text{S}}$	TDI to TCK, H or L		1.0			ns
$t_{\text{H}}$	TDI to TCK, H or L		2.0			ns
$t_{\text{S}}$	TMS to TCK, H or L		2.5			ns
$t_{\text{H}}$	TMS to TCK, H or L		1.5			ns
$t_{\text{W}}$	TCK Pulse Width, H or L		10.0			ns
$t_{\text{W}}$	$\overline{\text{TRST}}$ Pulse Width, L		2.5			ns
$t_{\text{REC}}$	Recovery Time, $\overline{\text{TRST}}$ to TCK		2.0			ns

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" specifies conditions of device operation.

**Note 2:** Typical values are given for  $V_{\text{CC}} = 3.3\text{V}$  and  $T_A = +25^\circ\text{C}$ .

**Note 3:** Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground except VOD,  $\Delta\text{VOD}$ , VTH and VTL which are differential voltages.

**Note 4:**  $t_{\text{LLHT}}$  and  $t_{\text{LHLT}}$  specifications are Guaranteed By Design (GBD) using statistical analysis.

**Note 5:** Because the Serializer is in TRI-STATE mode, the Deserializer will lose PLL lock and have to resynchronize before data transfer.

**Note 6:**  $t_{\text{DJIT}}$  specifications are Guaranteed By Design using statistical analysis.

**Note 7:** For the purpose of specifying deserializer PLL performance,  $t_{\text{DSR1}}$  and  $t_{\text{DSR2}}$  are specified with the REFCLK running and stable, and with specific conditions for the incoming data stream (SYNCPATs). It is recommended that the deserializer be initialized using either  $t_{\text{DSR1}}$  timing or  $t_{\text{DSR2}}$  timing.  $t_{\text{DSR1}}$  is the time required for the deserializer to indicate lock upon power-up or when leaving the power-down mode. Synchronization patterns should be sent to the device before initiating either condition.  $t_{\text{DSR2}}$  is the time required to indicate lock for the powered-up and enabled deserializer when the input (RI+ and RI-) conditions change from not receiving data to receiving synchronization patterns (SYNCPATs).

**Note 8:**  $t_{\text{RNM}}$  is a measure of how much phase noise (jitter) the deserializer can tolerate in the incoming data stream before bit errors occur. The Deserializer Noise Margin is Guaranteed By Design (GBD) using statistical analysis.

## AC Timing Diagrams and Test Circuits

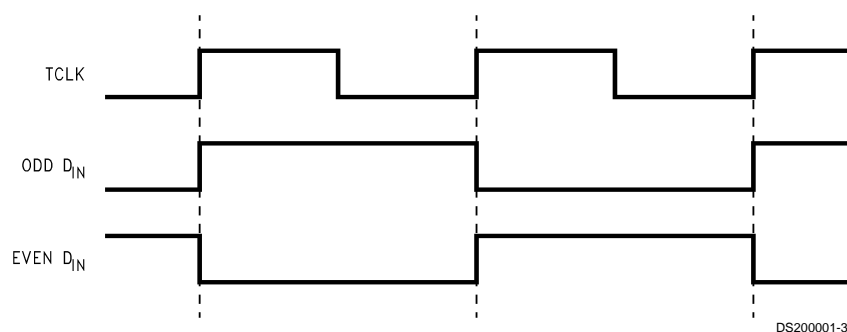


FIGURE 2. "Worst Case" Serializer ICC Test Pattern



## AC Timing Diagrams and Test Circuits (Continued)

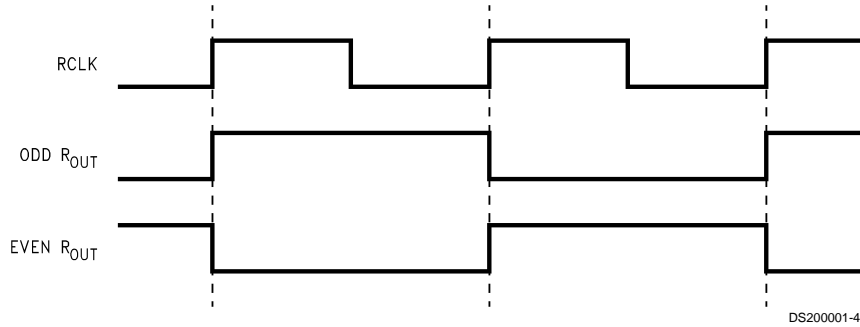


FIGURE 3. "Worst Case" Deserializer ICC Test Pattern

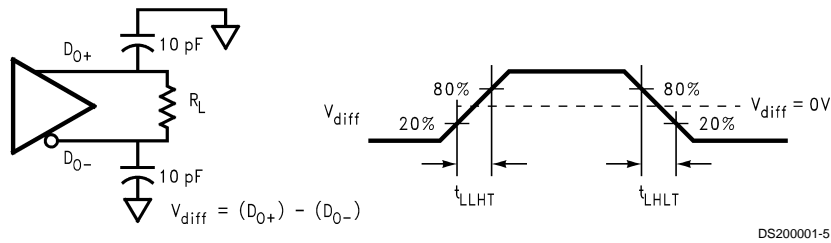


FIGURE 4. Serializer Bus LVDS Output Load and Transition Times

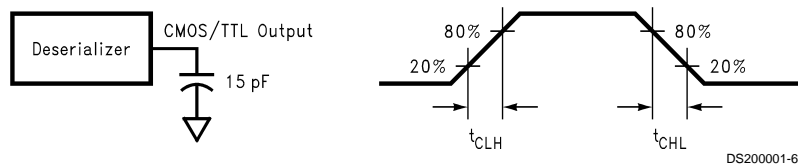


FIGURE 5. Deserializer CMOS/TTL Output Load and Transition Times

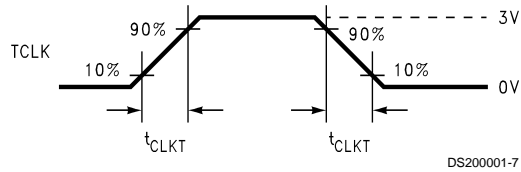
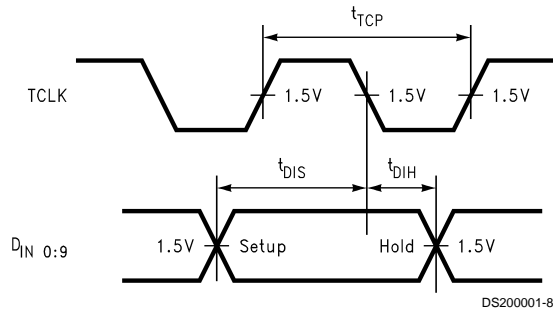


FIGURE 6. Serializer Input Clock Transition Time



Timing shown for TCLK\_R/F = LOW

FIGURE 7. Serializer Setup/Hold Times

## AC Timing Diagrams and Test Circuits (Continued)

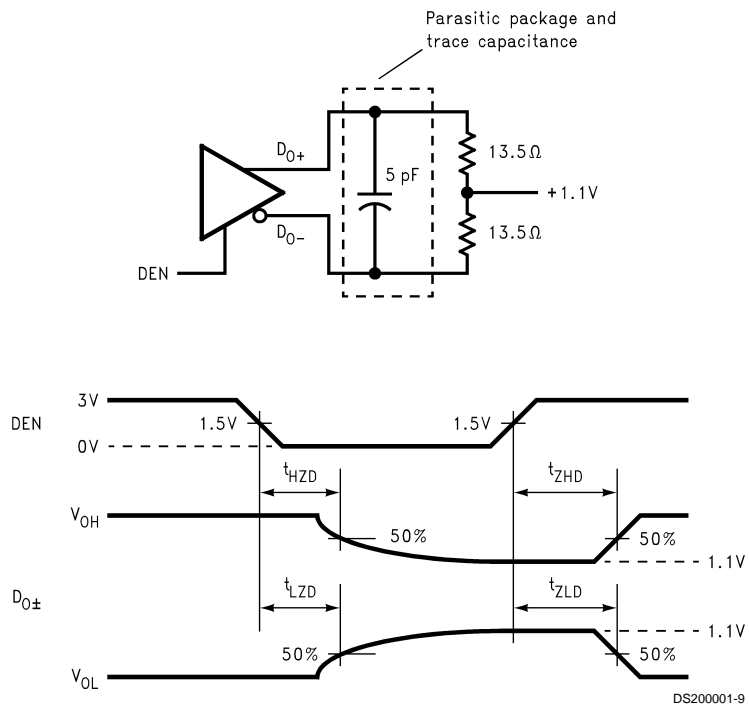


FIGURE 8. Serializer TRI-STATE Test Circuit and Timing

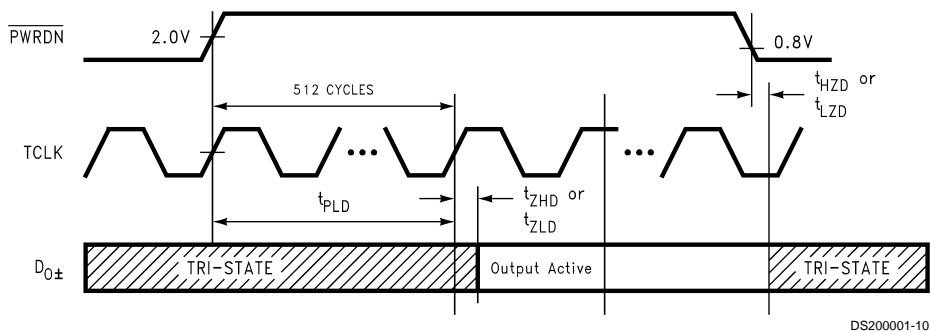


FIGURE 9. Serializer PLL Lock Time, and  $\overline{\text{PWRDN}}$  TRI-STATE Delays

## AC Timing Diagrams and Test Circuits (Continued)

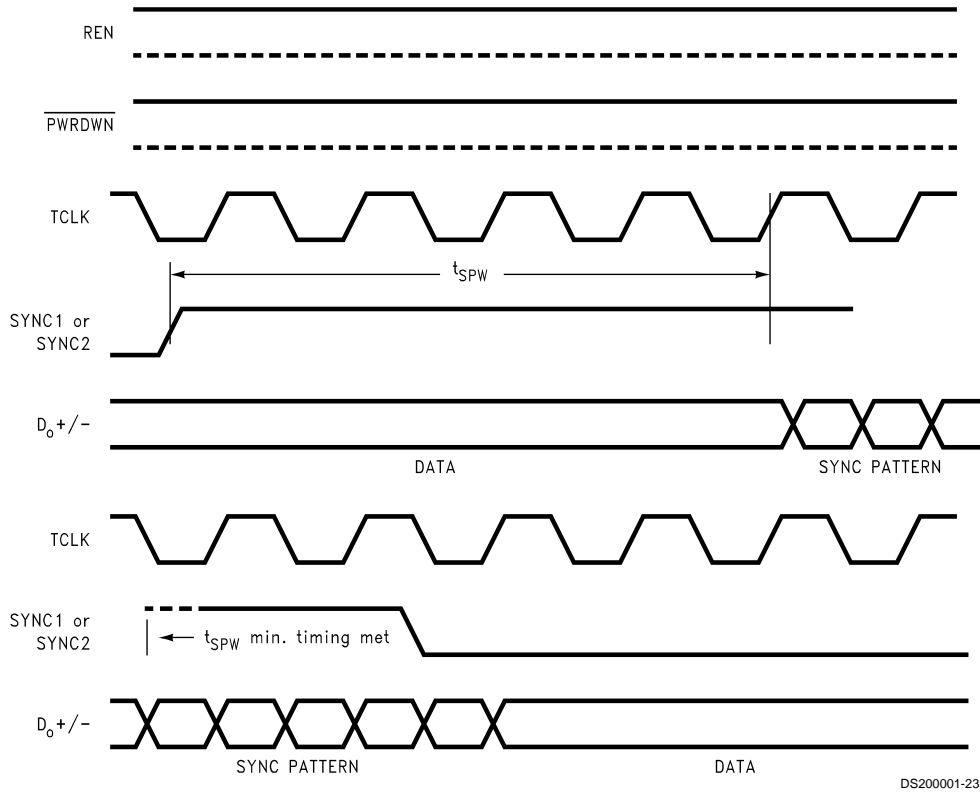


FIGURE 10. SYNC Timing Delays

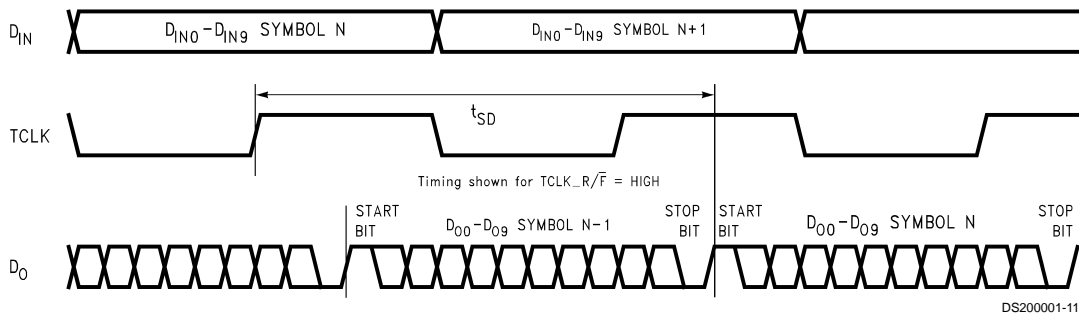


FIGURE 11. Serializer Delay

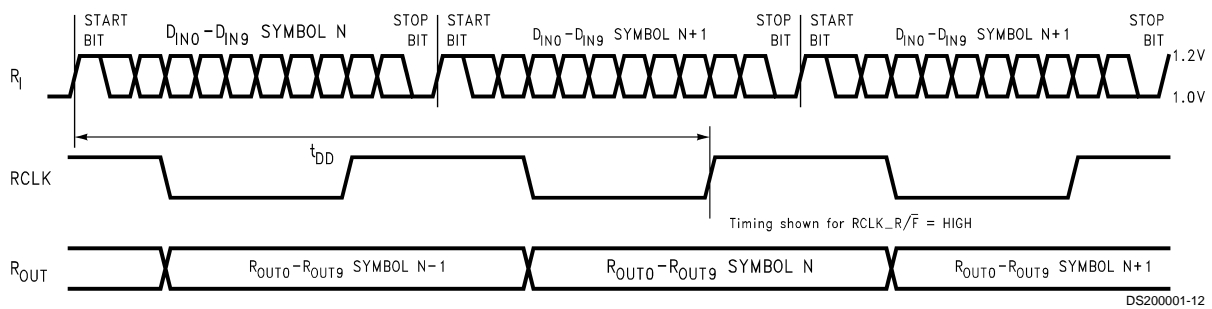
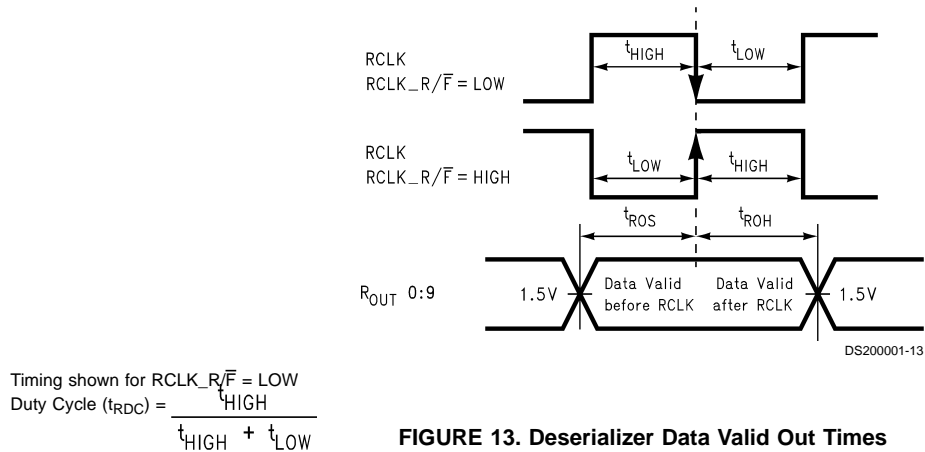
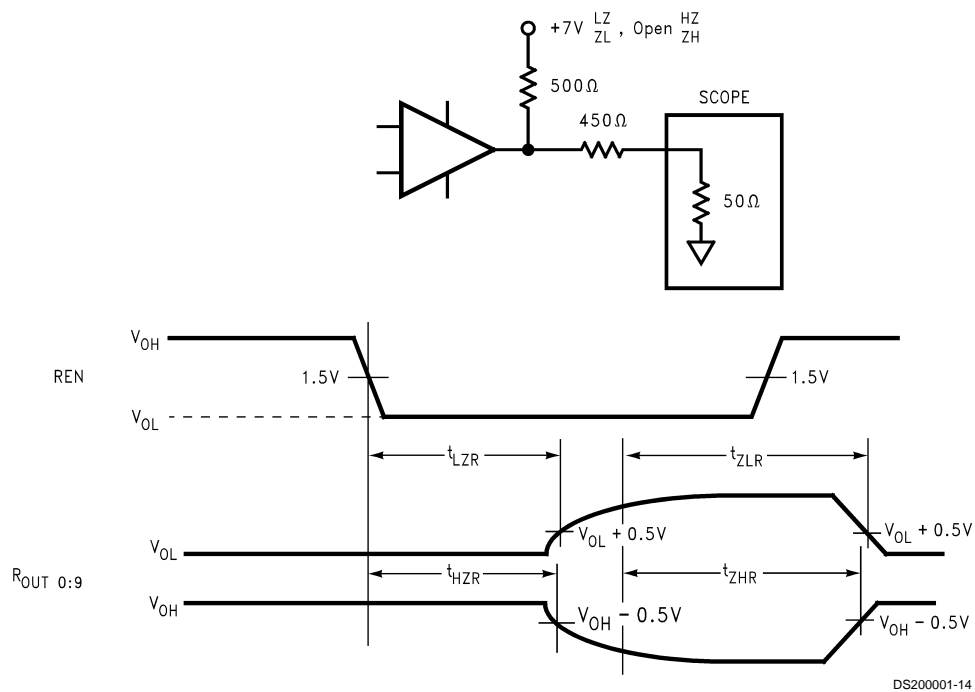


FIGURE 12. Deserializer Delay

## AC Timing Diagrams and Test Circuits (Continued)



**FIGURE 13. Deserializer Data Valid Out Times**



**FIGURE 14. Deserializer TRI-STATE Test Circuit and Timing**

## AC Timing Diagrams and Test Circuits (Continued)

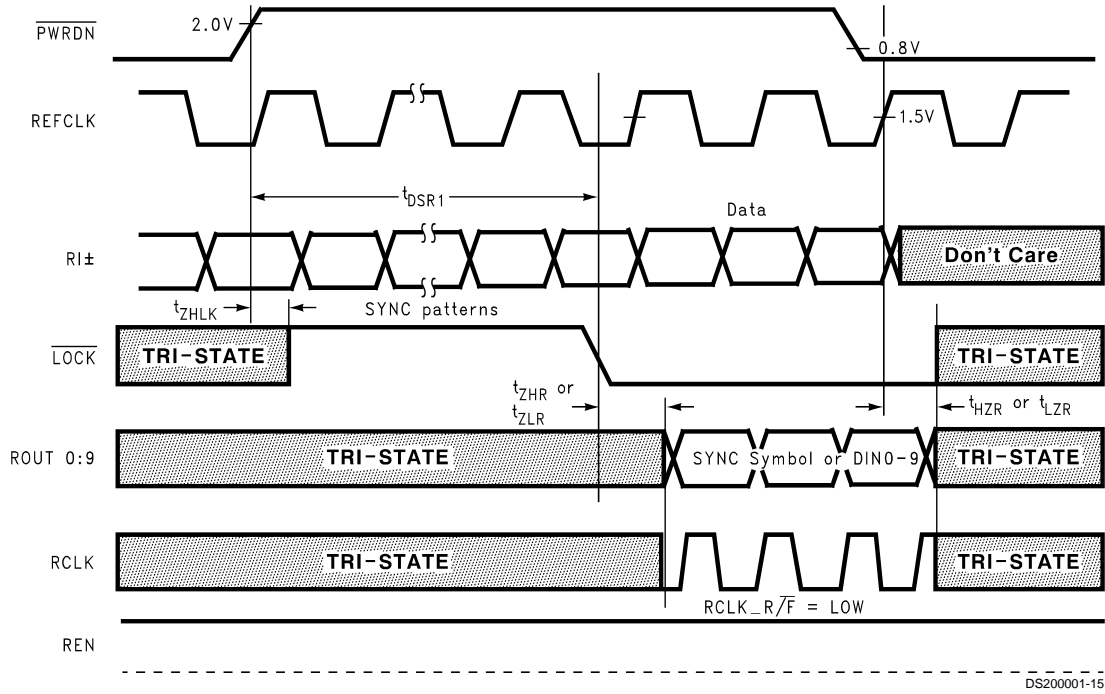


FIGURE 15. Deserializer PLL Lock Times and  $\overline{\text{PWRDN}}$  TRI-STATE Delays

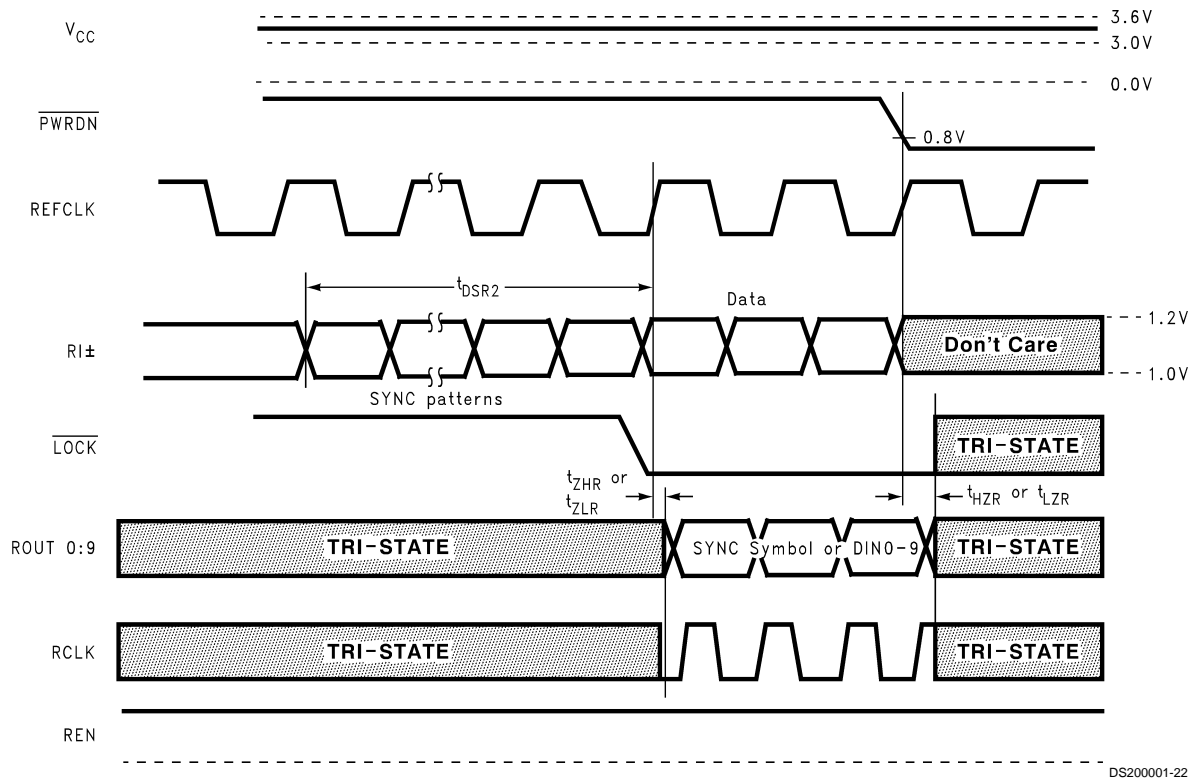
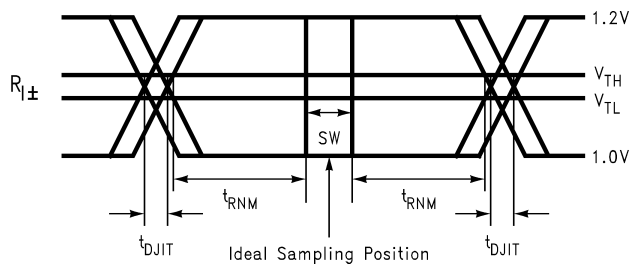


FIGURE 16. Deserializer PLL Lock Time from SyncPAT

## AC Timing Diagrams and Test Circuits (Continued)



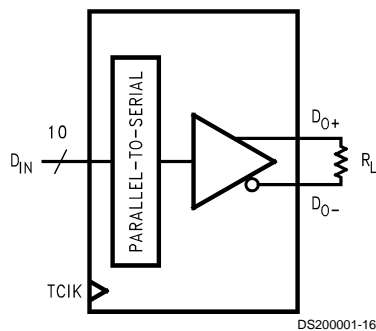
DS200001-21

SW - Setup and Hold Time (Internal Data Sampling Window)

$t_{DJIT}$  - Serializer Output Bit Position Jitter that results from Jitter on TCLK

$t_{RNM}$  = Receiver Noise Margin Time

**FIGURE 17. Receiver Bus LVDS Input Skew Margin**



DS200001-16

$V_{OD} = (D0^+) - (D0^-)$ .

Differential output signal is shown as (D0+)-(D0-), device in Data Transfer mode.

**FIGURE 18.  $V_{OD}$  Diagram**



## Application Information

### Using the SCAN921023 and SCAN921224

The Serializer and Deserializer chipset is an easy to use transmitter and receiver pair that sends 10 bits of parallel LVTTTL data over a serial Bus LVDS link up to 660 Mbps. An on-board PLL serializes the input data and embeds two clock bits within the data stream. The Deserializer uses a separate reference clock (REFCLK) and an onboard PLL to extract the clock information from the incoming data stream and then deserialize the data. The Deserializer monitors the incoming clock information, determines lock status, and asserts the  $\overline{\text{LOCK}}$  output high when loss of lock occurs.

### Power Considerations

An all CMOS design of the Serializer and Deserializer makes them inherently low power devices. In addition, the constant current source nature of the Bus LVDS outputs minimizes the slope of the speed vs.  $I_{CC}$  curve of conventional CMOS designs.

### Powering Up the Deserializer

The SCAN921224 can be powered up at any time by following the proper sequence. The REFCLK input can be running before the Deserializer powers up, and it must be running in order for the Deserializer to lock to incoming data. The Deserializer outputs will remain in TRI-STATE until the Deserializer detects data transmission at its inputs and locks to the incoming data stream.

### Transmitting Data

Once you power up the Serializer and Deserializer, they must be phase locked to each other to transmit data. Phase locking occurs when the Deserializer locks to incoming data or when the Serializer sends patterns. The Serializer sends SYNC patterns whenever the SYNC1 or SYNC2 inputs are high. The  $\overline{\text{LOCK}}$  output of the Deserializer remains high until it has locked to the incoming data stream. Connecting the  $\overline{\text{LOCK}}$  output of the Deserializer to one of the SYNC inputs of the Serializer will guarantee that enough SYNC patterns are sent to achieve Deserializer lock.

The Deserializer can also lock to incoming data by simply powering up the device and allowing the "random lock" circuitry to find and lock to the data stream.

While the Deserializer  $\overline{\text{LOCK}}$  output is low, data at the Deserializer outputs (ROUT0-9) is valid, except for the specific case of loss of lock during transmission which is further discussed in the 'Recovering from LOCK Loss' section below.

### Noise Margin

The Deserializer noise margin is the amount of input jitter (phase noise) that the Deserializer can tolerate and still reliably receive data. Various environmental and systematic factors include:

Serializer: TCLK jitter,  $V_{CC}$  noise (noise bandwidth and out-of-band noise)

Media: ISI, Large  $V_{CM}$  shifts

Deserializer:  $V_{CC}$  noise

### Recovering from LOCK Loss

In the case where the Deserializer loses lock during data transmission, up to 3 cycles of data that were previously received can be invalid. This is due to the delay in the lock detection circuit. The lock detect circuit requires that invalid clock information be received 4 times in a row to indicate loss of lock. Since clock information has been lost, it is possible that data was also lost during these cycles. There-

fore, after the Deserializer relocks to the incoming data stream and the Deserializer  $\overline{\text{LOCK}}$  pin goes low, at least three previous data cycles should be suspect for bit errors.

The Deserializer can relock to the incoming data stream by making the Serializer resend SYNC patterns, as described above, or by random locking, which can take more time, depending on the data patterns being received.

### Hot Insertion

All the BLVDS devices are hot pluggable if you follow a few rules. When inserting, ensure the Ground pin(s) makes contact first, then the VCC pin(s), and then the I/O pins. When removing, the I/O pins should be unplugged first, then the VCC, then the Ground. Random lock hot insertion is illustrated in Figure 21.

### PCB Considerations

The Bus LVDS Serializer and Deserializer should be placed as close to the edge connector as possible. In multiple Deserializer applications, the distance from the Deserializer to the slot connector appears as a stub to the Serializer driving the backplane traces. Longer stubs lower the impedance of the bus, increase the load on the Serializer, and lower the threshold margin at the Deserializers. Deserializer devices should be placed much less than one inch from slot connectors. Because transition times are very fast on the Serializer Bus LVDS outputs, reducing stub lengths as much as possible is the best method to ensure signal integrity.

### Transmission Media

The Serializer and Deserializer can also be used in point-to-point configuration of a backplane, through a PCB trace, or through twisted pair cable. In point-to-point configuration, the transmission media need only be terminated at the receiver end. Please note that in point-to-point configuration, the potential of offsetting the ground levels of the Serializer vs. the Deserializer must be considered. Also, Bus LVDS provides a  $\pm 1.2V$  common mode range at the receiver inputs.

### Failsafe Biasing for the SCAN921224

The SCAN921224 has an improved input threshold sensitivity of  $\pm 50mV$  versus  $\pm 100mV$  for the DS92LV1210 or DS92LV1212. This allows for greater differential noise margin in the SCAN921224. However, in cases where the receiver input is not being actively driven, the increased sensitivity of the SCAN921224 can pickup noise as a signal and cause unintentional locking. For example, this can occur when the input cable is disconnected.

External resistors can be added to the receiver circuit board to prevent noise pick-up. Typically, the non-inverting receiver input is pulled up and the inverting receiver input is pulled down by high value resistors. The pull-up and pull-down resistors ( $R_1$  and  $R_2$ ) provide a current path through the termination resistor ( $R_L$ ) which biases the receiver inputs when they are not connected to an active driver. The value of the pull-up and pull-down resistors should be chosen so that enough current is drawn to provide a +15mV drop across the termination resistor. Please see Figure 19 for the Failsafe Biasing Setup.

### Using $t_{DJIT}$ and $t_{RNM}$ to Validate Signal Quality

The parameters  $t_{DJIT}$  and  $t_{RNM}$  can be used to generate an eye pattern mask to validate signal quality in an actual application or in simulation.

The parameter  $t_{DJIT}$  measures the transmitter's ability to place data bits in the ideal position to be sampled by the receiver. The typical  $t_{DJIT}$  parameter of -80pS indicates that the crossing point of the Tx data is 80pS ahead of the ideal

## Application Information (Continued)

crossing point. The  $t_{DJIT(min)}$  and  $t_{DJIT(max)}$  parameters specify the earliest and latest, respectively, time that a crossing will occur relative to the ideal position.

The parameter  $t_{RNM}$  is calculated by first measuring how much of the ideal bit the receiver needs to ensure correct sampling. After determining this amount, what remains of the

ideal bit that is available for external sources of noise is called  $t_{RNM}$ . It is the offset from  $t_{DJIT(min \text{ or } max)}$  for the test mask within the eye opening.

The vertical limits of the mask are determined by the SCAN921224 receiver input threshold of  $\pm 50\text{mV}$ .

Please refer to the eye mask pattern of Figure 20 for a graphic representation of  $t_{DJIT}$  and  $t_{RNM}$ .

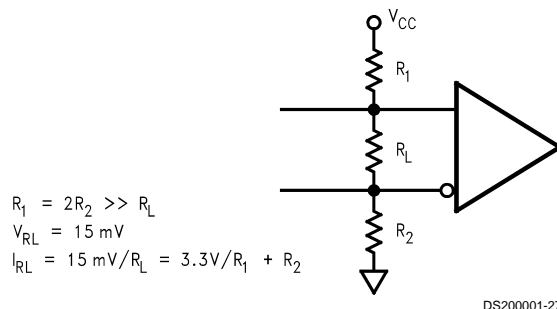


FIGURE 19. Failsafe Biasing Setup

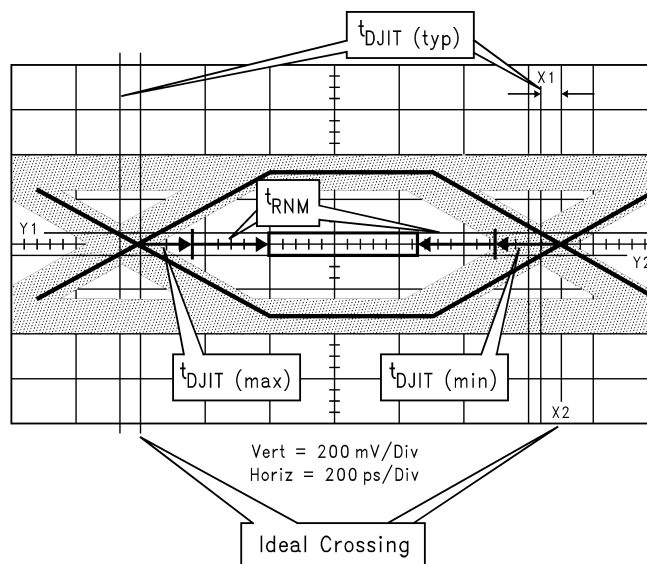


FIGURE 20. Using  $t_{DJIT}$  and  $t_{RNM}$  to Generate an Eye Pattern Mask and Validate Signal Quality

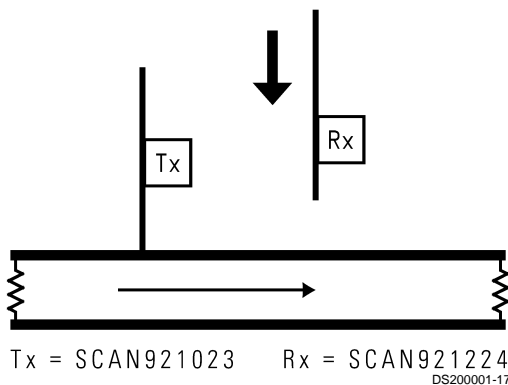
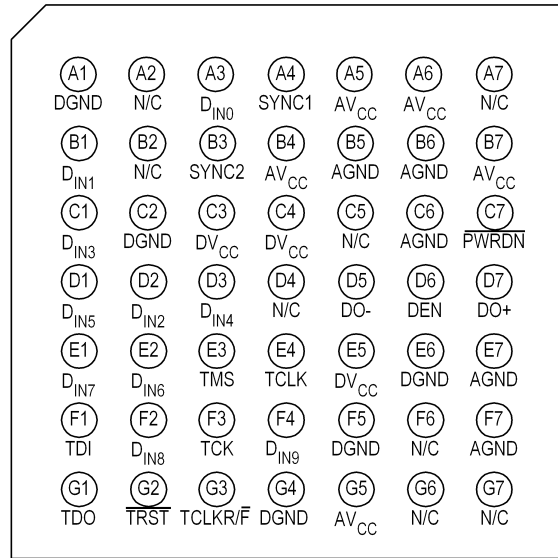


FIGURE 21. Random Lock Hot Insertion

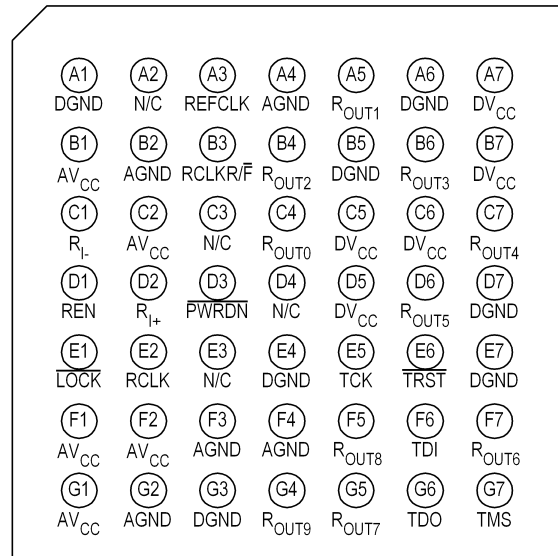
# Pin Diagrams

**SCAN921023SLC - Serializer  
(Top View)**



DS200001-30

**SCAN921224SLC - Deserializer  
(Top View)**



DS200001-31

## Serializer Pin Description

Pin Name	I/O	Ball Id.	Description
DIN	I	A3, B1, C1, D1, D2, D3, E1, E2, F2, F4	Data Input. LVTTTL levels inputs. Data on these pins are loaded into a 10-bit input register.
TCLKR/ $\overline{F}$	I	G3	Transmit Clock Rising/Falling strobe select. LVTTTL level input. Selects TCLK active edge for strobing of DIN data. High selects rising edge. Low selects falling edge.
DO+	O	D7	+ Serial Data Output. Non-inverting Bus LVDS differential output.
DO-	O	D5	- Serial Data Output. Inverting Bus LVDS differential output.
DEN	I	D6	Serial Data Output Enable. LVTTTL level input. A low puts the Bus LVDS outputs in TRI-STATE.
$\overline{PWRDN}$	I	C7	Powerdown. LVTTTL level input. $\overline{PWRDN}$ driven low shuts down the PLL and TRI-STATes outputs putting the device into a low power sleep mode.
TCLK	I	E4	Transmit Clock. LVTTTL level input. Input for 20 MHz–66 MHz system clock.
SYNC	I	A4, B3	Assertion of SYNC (high) for at least 1024 synchronization symbols to be transmitted on the Bus LVDS serial output. Synchronization symbols continue to be sent if SYNC continues to be asserted. TTL level input. The two SYNC pins are ORed.
DVCC	I	C3, C4, E5	Digital Circuit power supply.
DGND	I	A1, C2, F5, E6, G4	Digital Circuit ground.
AVCC	I	A5, A6, B4, B7, G5	Analog power supply (PLL and Analog Circuits).
AGND	I	B5, B6, C6, E7, F7	Analog ground (PLL and Analog Circuits).
TDI	I	F1	Test Data Input to support IEEE 1149.1
TDO	O	G1	Test Data Output to support IEEE 1149.1
TMS	I	E3	Test Mode Select Input to support IEEE 1149.1
TCK	I	F3	Test Clock Input to support IEEE 1149.1
$\overline{TRST}$	I	G2	Test Reset Input to support IEEE 1149.1
N/C	N/A	A2, A7, B2, C5, D4, F6, G6, G7	Leave open circuit, do not connect

## Deserializer Pin Description

Pin Name	I/O	Ball Id.	Description
ROUT	O	A5, B4, B6, C4, C7, D6, F5, F7, G4, G5	Data Output. $\pm 9$ mA CMOS level outputs.
RCLKR/ $\overline{F}$	I	B3	Recovered Clock Rising/Falling strobe select. TTL level input. Selects RCLK active edge for strobing of ROUT data. High selects rising edge. Low selects falling edge.
RI+	I	D2	+ Serial Data Input. Non-inverting Bus LVDS differential input.
RI-	I	C1	- Serial Data Input. Inverting Bus LVDS differential input.
$\overline{PWRDN}$	I	D3	Powerdown. TTL level input. $\overline{PWRDN}$ driven low shuts down the PLL and TRI-STATes outputs putting the device into a low power sleep mode.

## Deserializer Pin Description (Continued)

Pin Name	I/O	Ball Id.	Description
$\overline{\text{LOCK}}$	O	E1	$\overline{\text{LOCK}}$ goes low when the Deserializer PLL locks onto the embedded clock edge. CMOS level output. Totem pole output structure, does not directly support wired OR connections.
RCLK	O	E2	Recovered Clock. Parallel data rate clock recovered from embedded clock. Used to strobe ROUT, CMOS level output.
REN	I	D1	Output Enable. TTL level input. When driven low, TRI-STATes ROUT0–ROUT9 and RCLK.
DVCC	I	A7, B7, C5, C6, D5	Digital Circuit power supply.
DGND	I	A1, A6, B5, D7, E4, E7, G3	Digital Circuit ground.
AVCC	I	B1, C2, F1, F2, G1	Analog power supply (PLL and Analog Circuits).
AGND	I	A4, B2, F3, F4, G2	Analog ground (PLL and Analog Circuits).
REFCLK	I	A3	Use this pin to supply a REFCLK signal for the internal PLL frequency.
TDI	I	F6	Test Data Input to support IEEE 1149.1
TDO	O	G6	Test Data Output to support IEEE 1149.1
TMS	I	G7	Test Mode Select Input to support IEEE 1149.1
TCK	I	E5	Test Clock Input to support IEEE 1149.1
$\overline{\text{TRST}}$	I	E6	Test Reset Input to support IEEE 1149.1
N/C	N/A	A2, C3, D4, E3	Leave open circuit, do not connect

## Deserializer Truth Table

INPUTS		OUTPUTS		
$\overline{\text{PWRDN}}$	REN	ROUT [0:9]	$\overline{\text{LOCK}}$	RCLK
H (4)	H	Z	H	Z
H	H	Active	L	Active
L	X	Z	Z	Z
H	L	Z	Active	Z

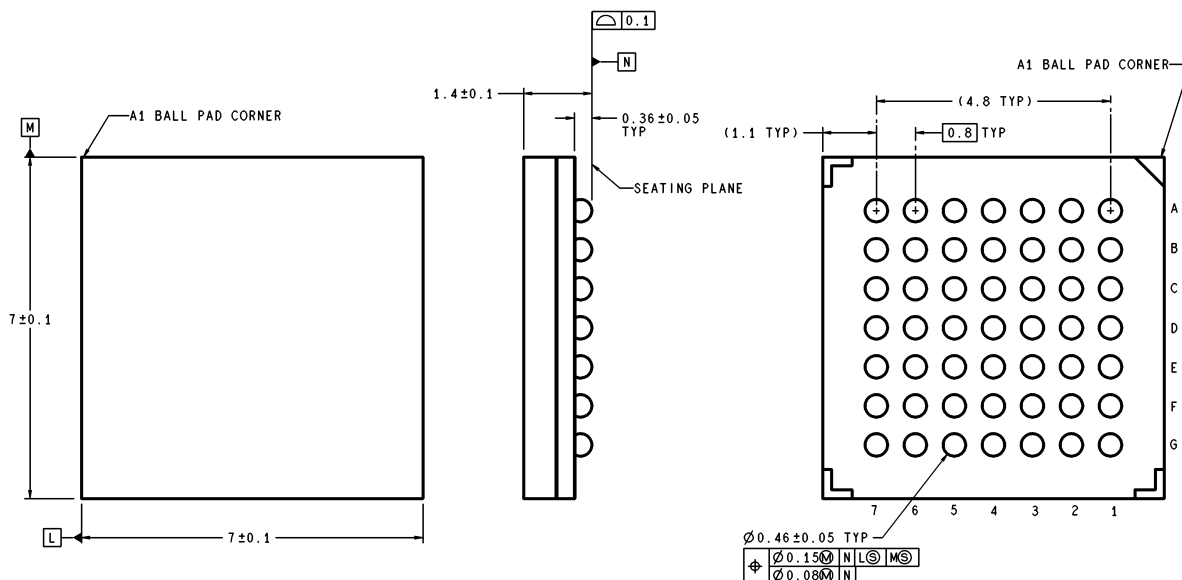
1)  $\overline{\text{LOCK}}$  Active indicates the  $\overline{\text{LOCK}}$  output will reflect the state of the Deserializer with regard to the selected data stream.

2) RCLK Active indicates the RCLK will be running if the Deserializer is locked. The Timing of RCLK with respect to ROUT is determined by RCLK\_R/F.

3) ROUT and RCLK are TRI-STATed when  $\overline{\text{LOCK}}$  is asserted High.

4) During Power-up.

## Physical Dimensions inches (millimeters) unless otherwise noted



DIMENSIONS ARE IN MILLIMETERS

SLC49A (Rev A)

Order Number SCAN921023SLC or SCAN921224SLC  
NS Package Number SLC49A

### LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT AND GENERAL COUNSEL OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com  
www.national.com

**National Semiconductor Europe**  
Fax: +49 (0) 180-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 69 9508 6208  
English Tel: +44 (0) 870 24 0 2171  
Français Tel: +33 (0) 1 41 91 8790

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: ap.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507