



N-Channel 20-V (D-S) MOSFET

CHARACTERISTICS

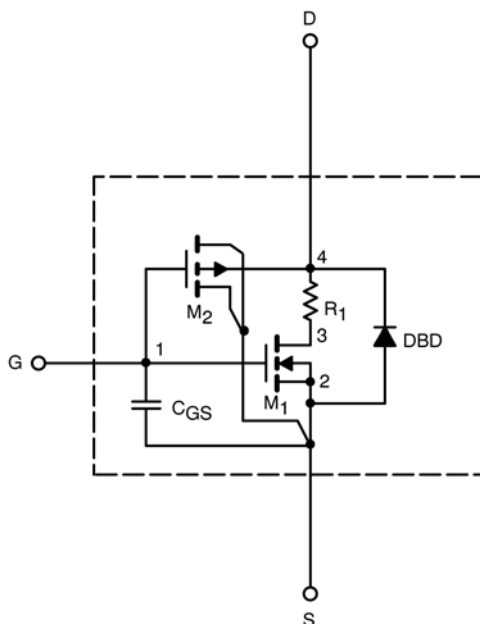
- N-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the -55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over the -55 to 125°C temperature ranges under the pulsed 0 to 10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2.2	2	V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = 10\ \text{V}$, $V_{GS} = 10\ \text{V}$	8.9		A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\ \text{V}$, $I_D = 0.30\ \text{A}$	0.47	0.47	Ω
		$V_{GS} = 4.5\ \text{V}$, $I_D = 0.10\ \text{A}$	0.81	0.80	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 10\ \text{V}$, $I_D = 0.30\ \text{A}$	569	550	mS
Diode Forward Voltage ^a	V_{SD}	$I_S = 0.30\ \text{A}$, $V_{GS} = 0\ \text{V}$	0.77	0.85	V
Dynamic^b					
Total Gate Charge	Q_g	$V_{DS} = 16\ \text{V}$, $V_{GS} = 10\ \text{V}$, $I_D = 0.30\ \text{A}$	776	1000	pC
Gate-Source Charge	Q_{gs}		205	205	
Gate-Drain Charge	Q_{gd}		200	200	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\ \text{V}$, $R_L = 50\ \Omega$ $I_D \cong 0.30\ \text{A}$, $V_{GEN} = 10\ \text{V}$, $R_G = 6\ \Omega$	4	4.5	ns
Rise Time	t_r		10	8	
Turn-Off Delay Time	$t_{d(off)}$		8	9	
Fall Time	t_f		36	6.3	

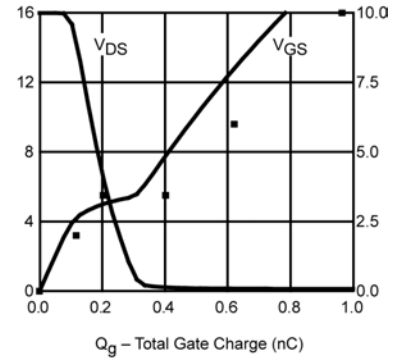
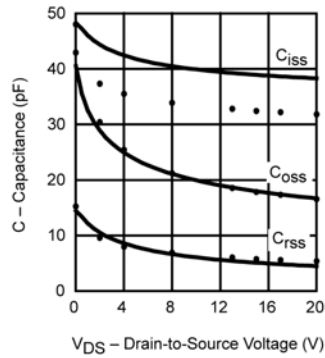
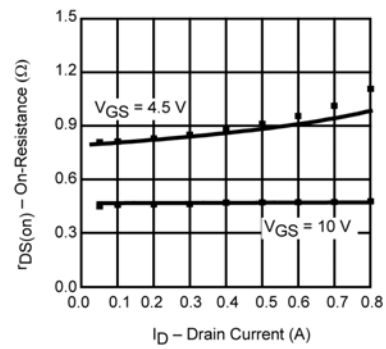
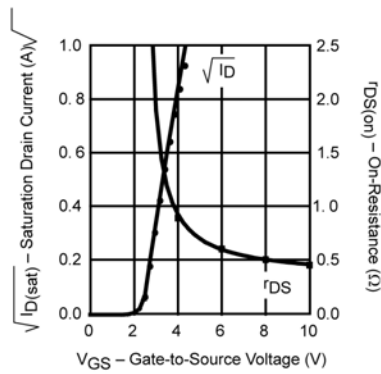
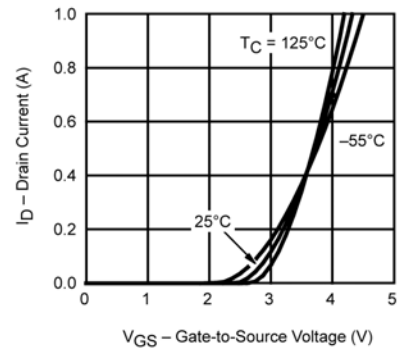
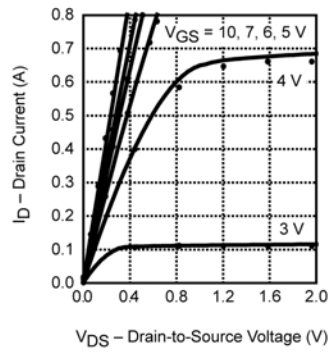
Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.



COMPARISON OF MODEL WITH MEASURED DATA ($T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.