PRELIMINARY

November 2004

FPD87370AXA

Low EMI, Low Dynamic Power VGA/XGA/WXGA TFT-LCD Timing Controller with Reduced Swing Differential Signaling (RSDS™) Outputs

General Description

The FPD87370AXA is a timing controller that combines an LVDS single pixel input interface with National's Reduced Swing Differential Signaling (RSDS $^{\text{TM}}$) output driver interface for VGA, XGA and Wide XGA resolutions. It resides on the TFT-LCD panel and provides the data buffering and control signal generation for VGA, XGA, and Wide XGA graphic modes. The RSDS $^{\text{TM}}$ path to the column driver contributes toward lowering radiated EMI and reducing system dynamic power consumption.

This single RSDS[™] bus conveys the 8-bit color data for VGA, XGA, and Wide XGA panels at 170 Mb/s when using VESA 60 Hz standard timing.

Features

- Reduced Swing Differential Signalling (RSDS™) digital bus reduces dynamic power, EMI and bus width from the timing controller
- LVDS single pixel input interface system
- Input clock range from 25 MHz to 85 MHz
- Drives RSDS™ Column Drivers at 170 Mb/s with an 85 MHz clock (Max.)
- Virtual 8 bit color depth in FRC/Dithering mode
- Single narrow 9-bit differential Source Driver bus minimizes width of Source PCB
- Ability to drive VGA, XGA and Wide XGA TFT-LCD Systems
- Failure detect function in DE mode (Bonding Option)
- CMOS circuitry operates from a 3.0V-3.6V supply

System Diagram

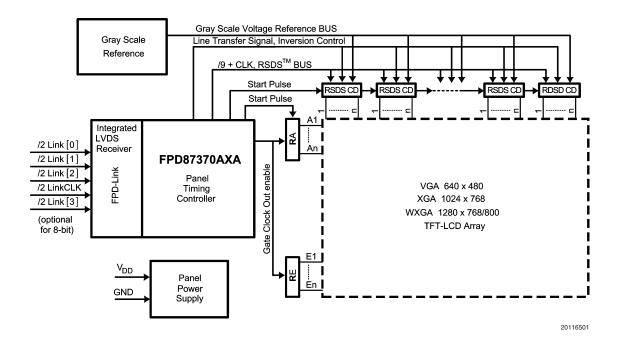
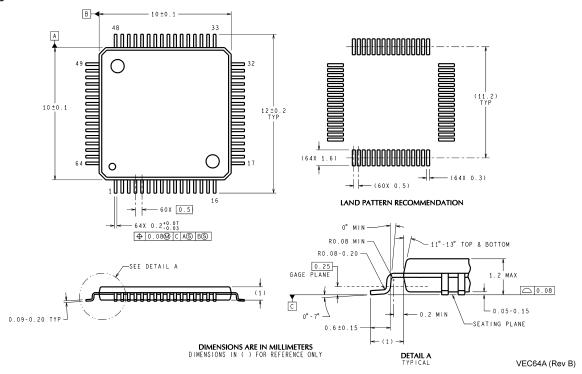


FIGURE 1. Block Diagram of the LCD Module

 $\mathsf{RSDS^{\textsc{tm}}}$ is a trademark of National Semiconductor Corporation

Physical Dimensions inches (millimeters) unless otherwise noted



64-pin TQFP Package Order Number FPD87370AXAVS NS Package Number VEC-64A

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