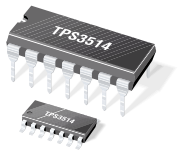


PC POWER–SUPPLY SUPERVISORS

FEATURES

- **OVER-VOLTAGE PROTECTION AND LOCKOUT: 12V, 5V, and 3.3V Supplies**
- **OVER-CURRENT PROTECTION AND LOCKOUT: 12V, 5V, and 3.3V Supplies**
- **UNDER-VOLTAGE PROTECTION AND LOCKOUT: 12V Supplies**
- **UNDER-VOLTAGE DETECT: 5V and 3.3V Supplies**
- **FAULT-PROTECTION OUTPUT WITH OPEN–DRAIN OUTPUT STAGE**
- **OPEN-DRAIN, POWER-GOOD OUTPUT SIGNAL: Monitors Power–Good Signal Input 3.3V and 5V Supplies**
- **300ms POWER-GOOD DELAY**
- **75ms DELAY: 5V, 3.3V Power-Supply Short-Circuit Turn-On Protection**
- **2.3ms $\overline{\text{PSON}}$ CONTROL TO $\overline{\text{FPO}}$ TURN–OFF DELAY**
- **38ms $\overline{\text{PSON}}$ CONTROL DEBOUNCE**
- **WIDE SUPPLY VOLTAGE RANGE: 4.5V to 15V**

DESCRIPTION

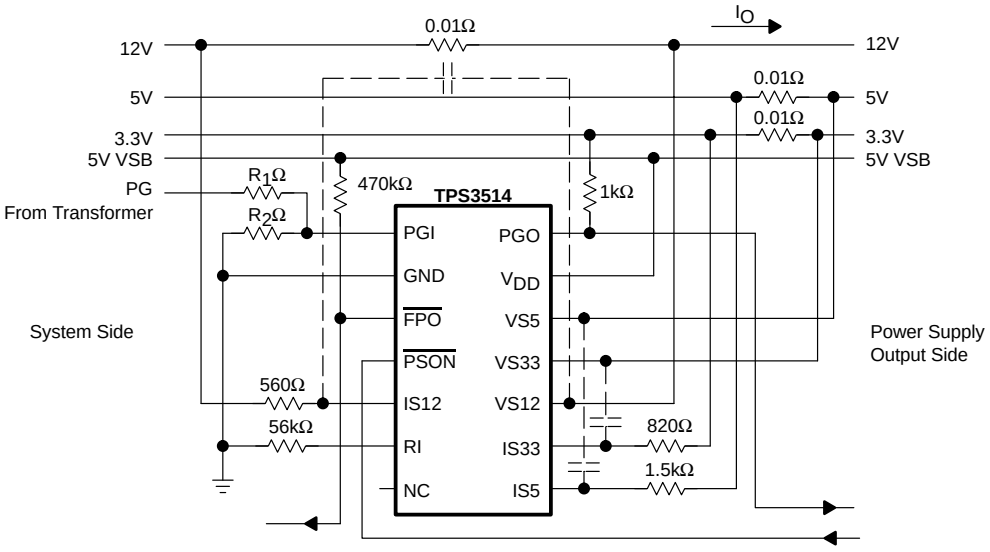
The TPS3514 is a PC switching power-supply system monitor with minimum external components. It provides under-voltage lockout (UVLO), over-voltage (OV), under-voltage (UV), over-current (OC), protection circuits, power-good indicator, and on/off control.

UVLO thresholds are 4.45V (on) and 3.65V (off). Over-current protection (OCP) and over-voltage protection (OVP) monitor 3.3V, 5V, and 12V supplies. When an OC or OV condition is detected, the power–good output (PGO) is asserted LOW and the fault protection output ($\overline{\text{FPO}}$) is latched HIGH. $\overline{\text{PSON}}$ from LOW-to-HIGH resets the latch. The OCP function will be enabled 75ms after $\overline{\text{PSON}}$ goes LOW with PGI HIGH and a debounce of typically 38ms. A built-in 2.3ms delay with 38ms debounce from $\overline{\text{PSON}}$ to $\overline{\text{FPO}}$ output is enabled at turn–off.

An external resistor is connected between the RI pin and the GND pin. This will program a precise $I_{(REF)}$ for OCP function. The programmable $I_{(REF)}$ range is from 12.5µA to 62.5µA. Three OCP comparators and the $I_{(REF)}$ section are supplied by VS12. The current draw from the VS12 pin is less than 1mA.

The power–good feature monitors PGI, the 3.3V and 5V supplies, and issues a power–good signal when the output is ready.

The TPS3514 is characterized for operation from –40°C to 85°C. The TPS3514 is available in DIP-14 and SO-14 packages.



PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE–LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TPS3514	SO-14	D	–40°C to +85°C	TPS3514	TPS3514D	Rails, 50
					TPS3514DR	Tape and Reel, 2500
	DIP-14	N			TPS3514N	Rails, 25

NOTE: (1) For the most current specifications and package information, refer to our web site at www. ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Supply Voltage, V_{DD}	16V
Voltage on $\overline{PSON}$, IS5, IS33, PGI	8V
Voltage on VS33, VS5	16V
Voltage on $\overline{FPO}$	16V
PGO	8V
All Other Pins	–0.3V to 16V
Continuous Total Power Dissipation	See Dissipation Rating Table
Operating Free-Air Temperature Range, T_A	–40°C to 85°C
Storage Temperature Range, T_{stg}	–65°C to 150°C
Soldering Temperature	260°C

NOTES: (1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability. (2) All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

At specified temperature range.

PARAMETER		MIN	MAX	UNITS
Supply Voltage	V_{DD}	4.5	15	V
Inputs	V_I			
$\overline{PSON}$, VS5, VS33, IS5, IS33			7	V
VS12, IS12			15	V
PGI			V_{DD} + 0.3V (max = 7V)	V
Outputs	V_O			
$\overline{FPO}$			15	V
PGO			7	V
Sink Current	$I_{O(SINK)}$			
$\overline{FPO}$			20	mA
PGO			10	mA
Supply Voltage Rising Time	t_R(1)	1		ms
OCP Reference Source	$I_{(REF)}$	12.5	62.5	µA
Operating Free-Air Temperature Range	T_A	–40	85	°C

NOTE: (1) V_{DD} rising and falling slew rate must be less than 14V/ms.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISSIPATION RATING TABLE

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	956mW	7.65mW/°C	612mW	497mW
N	1512mW	12.1mW/°C	968mW	786mW

OVER–CURRENT PROTECTION

	MAX OUTPUT CURRENT	OVER–CURRENT PROTECTION TRIP POINT(1)
12V	6A	9.2A
5V	16A	24.6A
3.3V	9A	13.5A

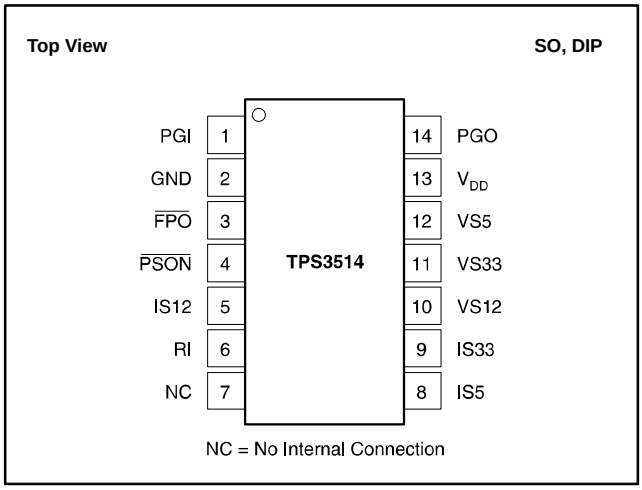
NOTE: (1) Over-current protection trip point can be programmable.

ELECTRICAL CHARACTERISTICS

Limits apply over operating free-temperature range, T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	TPS3514			UNITS
			MIN	TYP	MAX	
OVER–VOLTAGE AND OVER-CURRENT PROTECTION						
Over–Voltage Threshold						
VS33			3.7	3.9	4.1	V
VS5			5.7	6.1	6.5	V
VS12			13.2	13.8	14.4	V
Ratio of Current Sense Sink Current to Current Sense Setting Pin (RI) Source Current, $I_{(REF)}$ C		Resistor at RI = 30kΩ, 0.1% Resistor	7.6	8	8.4	
Leakage Current ($\overline{FPO}$)	I_{lkg}	$V_{(\overline{FPO})}$ = 5V			5	µA
Low-Level Output Voltage ($\overline{FPO}$)	V_{OL}	$I_{(SINK)}$ = 20mA, V_{DD} = 5V			0.7	V
Noise Deglitch Time (OVP)		V_{DD} = 5V	35	73	110	µs
Current Source Reference Voltage	$V_{(RI)}$	V_{DD} = 5V	1.1	1.15	1.2	V
UNDER–VOLTAGE LOCKOUT						
Start Threshold Voltage					4.45	V
Minimum Operating Voltage After Start–Up			3.65			V
PGI AND PGO						
Input Threshold	$V_{IT(PGI)}$		0.99 x typ	1.15	1.01 x typ	V
Under-Voltage Threshold						
VS33			2	2.2	2.4	V
VS5			3.3	3.5	3.7	V
VS12			8.5	9	9.5	V
Input Offset Voltage for OCP Comparators			–5		5	mV
Leakage Current (PGO)	I_{lkg}	PGO = 5V			5	µA
Low-Level Output Voltage (PGO)	V_{OL}	$I_{(SINK)}$ = 10mA, V_{DD} = 4.5V			0.4	V
Short-Circuit Protection Delay	3.3V, 5V		49	75	114	ms
Delay Time	$t_{d(1)}$					
PGI to PGO		V_{DD} = 5V	200	300	450	ms
PGI to $\overline{FPO}$		V_{DD} = 5V	3.2	4.8	7.2	ms
Noise Deglitch Time						
PGI to PGO		V_{DD} = 5V	88	150	225	ms
12V UVP to $\overline{FPO}$		V_{DD} = 5V	88	150	225	ms
$\overline{PSON}$ CONTROL						
Input Pull-Up Current	I_I	$\overline{PSON}$ = 0V		–120		µA
High-Level Input Voltage	V_{IH}		2.4			V
Low-Level Input Voltage	V_{IL}				1.2	V
Debounce Time ($\overline{PSON}$)	$t_{(b)}$	V_{DD} = 5V	24	38	50	ms
Delay Time ($\overline{PSON}$ to $\overline{FPO}$)	$t_{(d)(2)}$	V_{DD} = 5V	t_b + 1.1	t_b + 2.3	t_b + 4	ms
TOTAL DEVICE						
Supply Current	I_{DD}	$\overline{PSON}$ = 5V			1	mA

PIN CONFIGURATION



PIN ASSIGNMENTS

PIN	NAME	FUNCTION
3	$\overline{\text{FPO}}$	Inverted Fault Ptotection output. Open-drain output stage.
2	GND	Ground
5	IS12	12V Over-Current Protection Input
8	IS5	5V Over-Current Protection Input
9	IS33	3.3V Over-Current Protection Input
7	NC	No Internal Connection
1	PGI	Power-Good Input
14	PGO	Power-Good Output. Open-drain output stage.
4	$\overline{\text{PSON}}$	On/Off Control Input
6	RI	OCP Reference Source
13	V_{DD}	Supply Voltage
10	VS12	12V Over-Voltage/Under-Voltage Protection Input
11	VS33	3.3V Over-Voltage/Under-Voltage Protection Input
12	VS5	5V Over-Voltage/Under-Voltage Protection Input

FUNCTION TABLE

PGI	$\overline{\text{PSON}}$	UV CONDITION 3.3V/5V	OV CONDITIONS	UV CONDITION 12V OC CONDITIONS	$\overline{\text{FPO}}$(1)	PGO(2)
< 0.9V	L	No	No	No	L	L
< 0.9V	L	No	No	Yes	L	L
< 0.9V	L	No	Yes	No	H	L
< 0.9V	L	No	Yes	Yes	H	L
< 0.9V	L	Yes	No	No	L	L
< 0.9V	L	Yes	No	Yes	L	L
< 0.9V	L	Yes	Yes	No	H	L
< 0.9V	L	Yes	Yes	Yes	H	L
> 1.2V	L	No	No	No	L	H
> 1.2V	L	No	No	Yes	H	L
> 1.2V	L	No	Yes	No	H	L
> 1.2V	L	No	Yes	Yes	H	L
> 1.2V	L	Yes	No	No	H	L
> 1.2V	L	Yes	No	Yes	H	L
> 1.2V	L	Yes	Yes	No	H	L
> 1.2V	L	Yes	Yes	Yes	H	L
x	H	x	x	x	H	L

x = Don't Care.
NOTES: (1) For $\overline{\text{FPO}}$, L = Fault is not latched. H = Fault is latched. (2) For PGO, L = Fault. H = No Fault.

TIMING DIAGRAMS

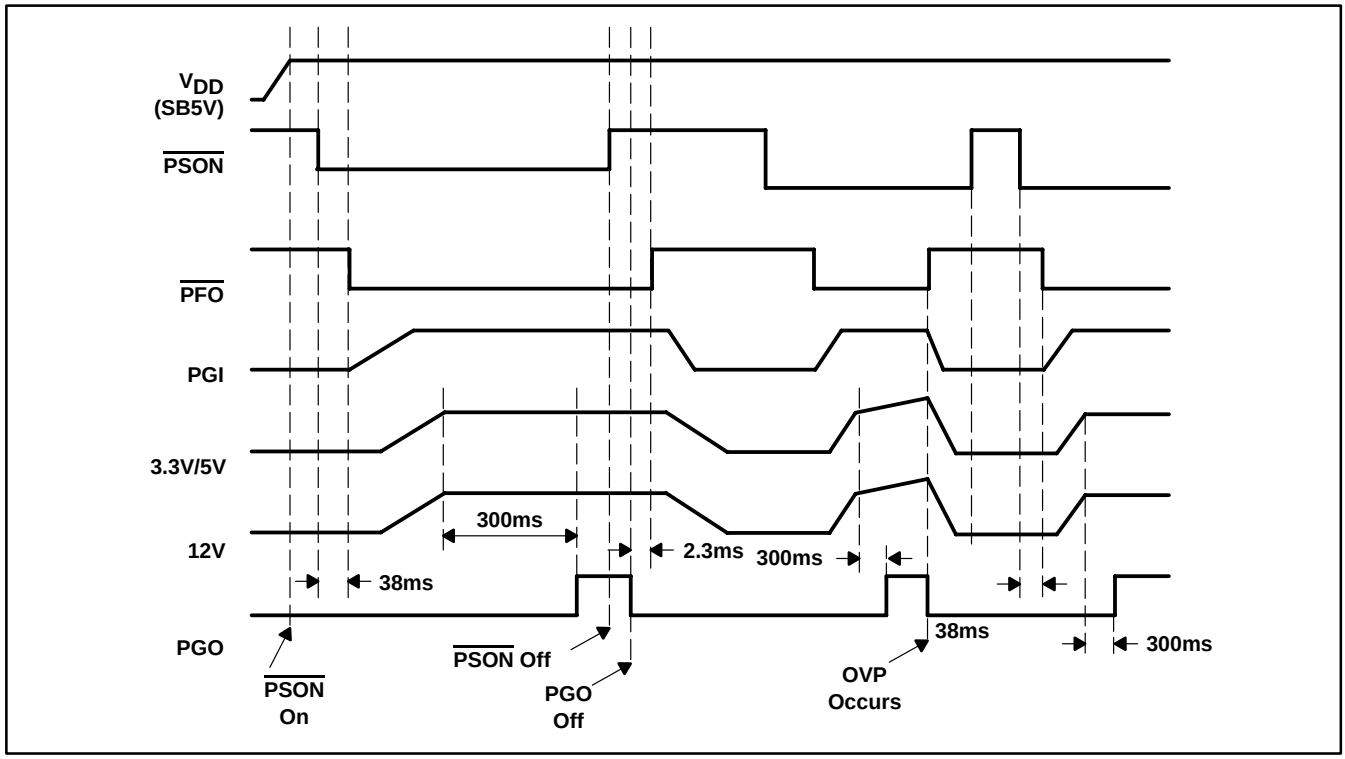


DIAGRAM 1: AC Turn-On and Over-Voltage Protect.

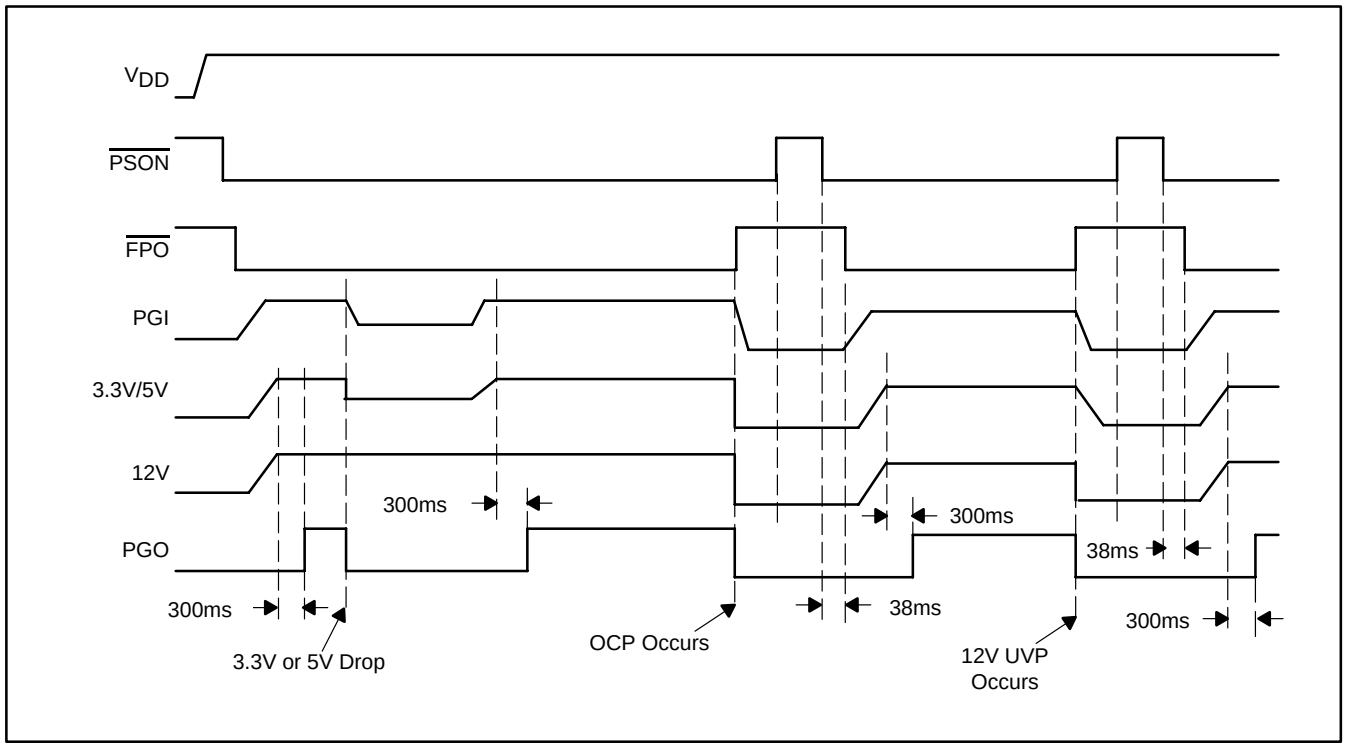
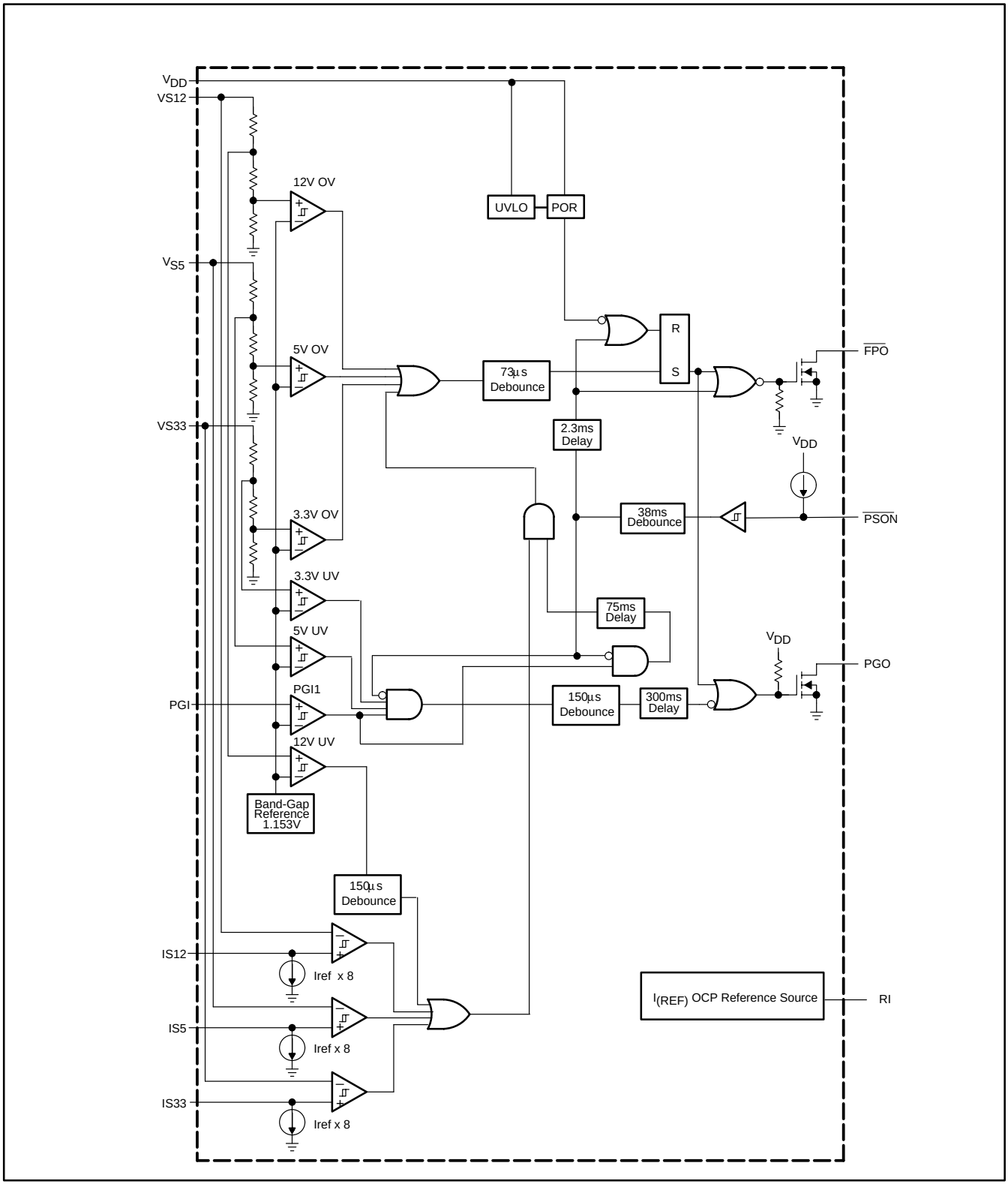


DIAGRAM 2: Over-Current and Under-Voltage Detect/Protect.

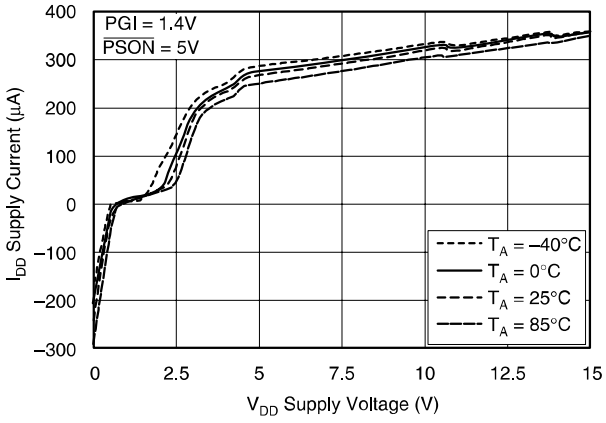
SCHEMATIC


VDD
VS12
VS5
VS33
PGI
IS12
IS5
IS33
12V OV
5V OV
3.3V OV
3.3V UV
5V UV
PGI1
12V UV
Band-Gap Reference 1.153V
UVLO
POR
R
S
73µs Debounce
2.3ms Delay
38ms Debounce
75ms Delay
150µs Debounce
300ms Delay
150µs Debounce
Iref x 8
Iref x 8
Iref x 8
I(REF) OCP Reference Source
FPO
PSON
PGO
RI

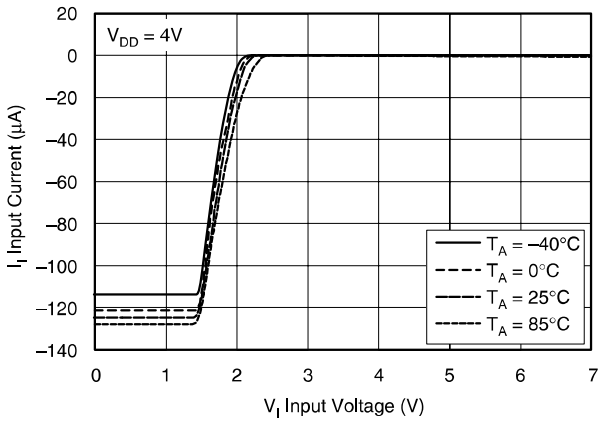
TYPICAL CHARACTERISTICS

T_A = 25° unless otherwise noted.

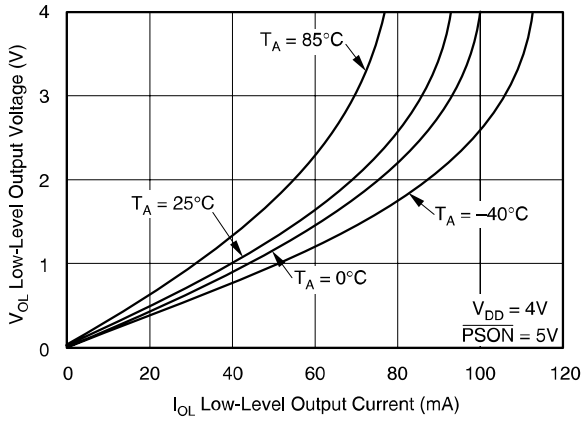
SUPPLY CURRENT vs SUPPLY VOLTAGE



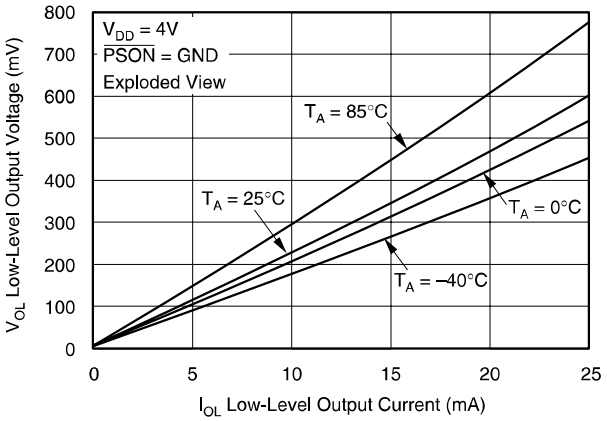
INPUT CURRENT ($\overline{PSON}$) vs INPUT VOLTAGE ($\overline{PSON}$)



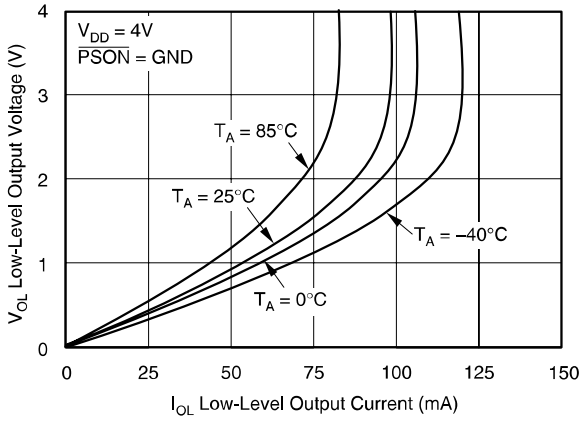
LOW-LEVEL OUTPUT VOLTAGE ($\overline{FPO}$) vs LOW-LEVEL OUTPUT CURRENT ($\overline{FPO}$)



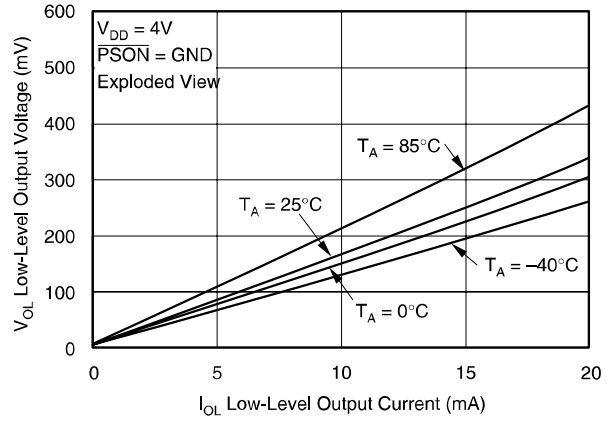
LOW-LEVEL OUTPUT VOLTAGE ($\overline{FPO}$) vs LOW-LEVEL OUTPUT CURRENT ($\overline{FPO}$)



LOW-LEVEL OUTPUT VOLTAGE (PGO) vs LOW-LEVEL OUTPUT CURRENT (PGO)

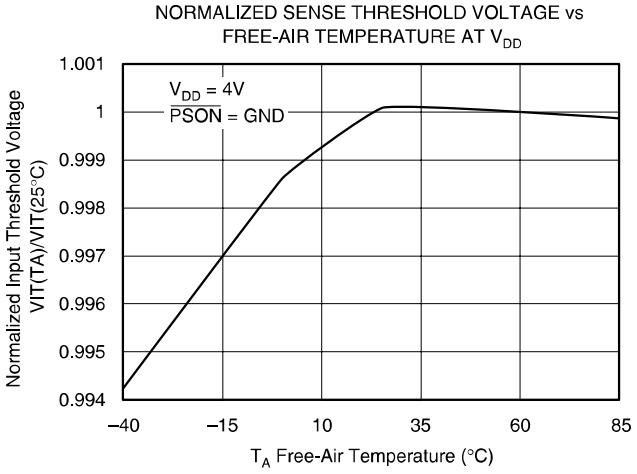


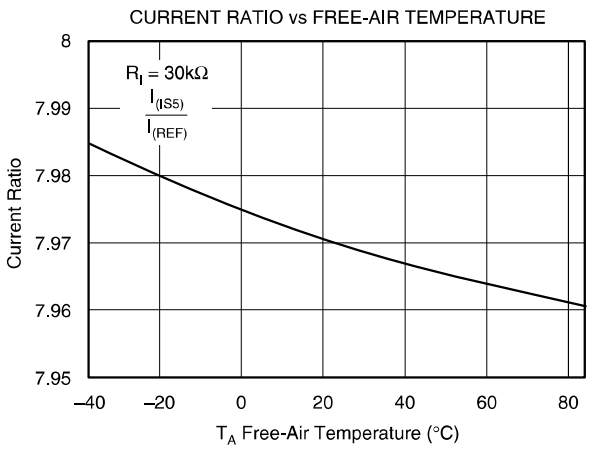
LOW-LEVEL OUTPUT VOLTAGE (PGO) vs LOW-LEVEL OUTPUT CURRENT (PGO)



TYPICAL CHARACTERISTICS (Cont.)

T_A = 25° unless otherwise noted.





DETAILED DESCRIPTION

POWER-GOOD AND POWER-GOOD DELAY

A PC power supply is commonly designed to provide a power-good signal, which is defined by the computer manufacturers. Power-Good Output (PGO) is a power-good indicator and should be asserted HIGH by the PC power supply to indicate that the 5VDC and 3.3VDC outputs are above the under-voltage threshold limit. At this time, the supply should be able to provide enough power to assure continuous operation within the specification.

Conversely, when either the 5VDC or the 3.3VDC output voltages fall below the under-voltage threshold, or when main power has been removed for a sufficiently long time so that power-supply operation is no longer assured, PGO should be deasserted to a LOW state.

The power-good, DC enable ($\overline{PSON}$), and the 5V/3.3V supply rails are shown in Figure 1.

Although there is no requirement to meet specific timing parameters, the following signal timings are recommended:

$2ms \le t_2 \le 20ms$, $100ms < t_3 < 2000ms$, $t_4 > 1ms$, $t_5 \le 10ms$

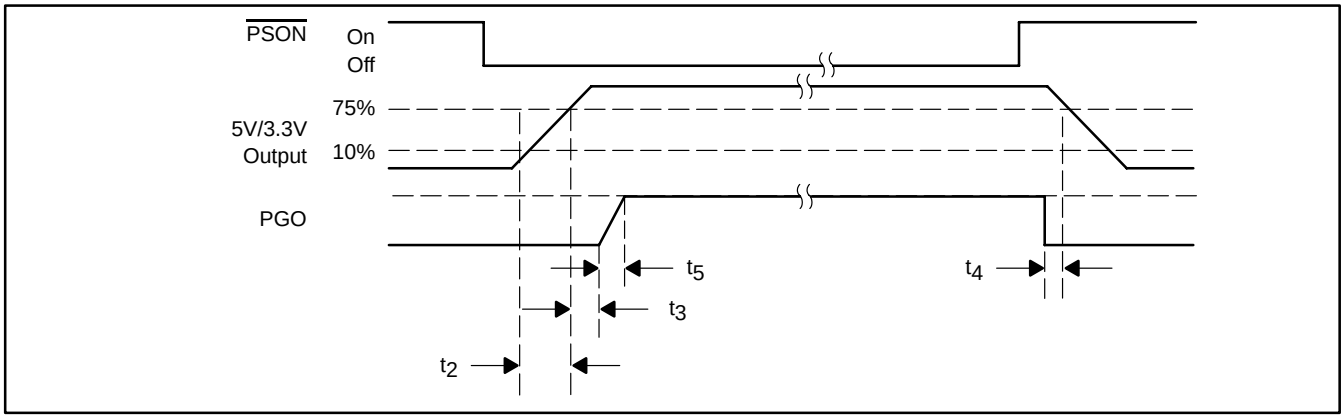


FIGURE 1: Timing of $\overline{PSON}$ and PGO.

Furthermore, motherboards should be designed to comply with the above recommended timing. If timings other than these are implemented or required, this information should be clearly specified.

The TPS3514 family of power-supply supervisors provides a PGO for the 3.3V and 5V supply voltage rails and a separate Power-Good Input (PGI). An internal timer is used to generate a 300ms power-good delay.

If the voltage signals at PGI, VS33, and VS5 rise above the under-voltage threshold, the open-drain PGO will go HIGH after a delay of 300ms. When the PGI voltage or any of the 3.3V/5V rail drops below the under-voltage threshold, PGO will be disabled immediately.

POWER-SUPPLY REMOTE ON/OFF ($\overline{\text{PSON}}$) AND FAULT PROTECT OUTPUT ($\overline{\text{FPO}}$)

Since the latest personal computer generation focuses on easy turn-on and power–saving functions, the PC power supply will require two characteristics. One is a DC power-supply remote on/off function; the other is standby voltage to achieve very low power consumption of the PC system. Thus, requiring the main power supply to be shut down.

The power-supply remote on/off ($\overline{\text{PSON}}$) is an active-LOW signal that turns on all of the main power rails including the 3.3V, 5V, –5V, and –12V power rails. When this signal is held HIGH by the PC motherboard or left open-circuited, the signal of the Fault Protect Output ($\overline{\text{FPO}}$) also goes HIGH. In this condition, the main power rails should not deliver current and should be held at 0V.

When the $\overline{\text{FPO}}$ signal is held HIGH due to an occurring fault condition, the fault status will be latched and the outputs of the main power rails should not deliver current and should be held at 0V. Toggling $\overline{\text{PSON}}$ from LOW to HIGH will reset the fault protection latch. During this fault condition, only the standby power is not affected.

When $\overline{\text{PSON}}$ goes from HIGH to LOW or LOW to HIGH, the 38ms debounce block will prevent a glitch on the input from disabling/enabling the $\overline{\text{FPO}}$ output. During the HIGH to LOW transition, the under-voltage function is disabled to prevent turn-on failure.

Power should be delivered to the rails only if the $\overline{\text{PSON}}$ signal is held at ground potential, thus, $\overline{\text{FPO}}$ is active LOW. The $\overline{\text{FPO}}$ pin can be connected to 5VDC (or up to 15VDC) through a pull-up resistor.

UNDER-VOLTAGE PROTECTION (UVP)

The TPS3514 provides Under-Voltage Protection (UVP) for the 12V rail and Under-Voltage Detect (UVD) for the 3.3V and 5V rails. When an under-voltage condition appears at the VS12 input pin for more than 150µs, the $\overline{\text{FPO}}$ output goes HIGH and PGO goes LOW. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from LOW to HIGH or V_{DD} is removed.

OVER-CURRENT PROTECTION (OCP)

In bridge, or forward type, off-line switching power supplies, usually designed for medium to large power, the overload protection design needs to be very precise. Most of these types of power supplies sense the output current for an overload condition. The trigger-point needs to be set higher than the maximum load in order to prevent false turn-on.

The TPS3514 provides Over-Current Protection (OCP) for the 3.3V, 5V, and 12V rails. When an over-current condition appears at the OCP comparator input pins for more than 73µs, the $\overline{\text{FPO}}$ output goes HIGH and PGO goes LOW. Also, this fault condition will be latched until $\overline{\text{PSON}}$ is toggled from LOW to HIGH or V_{DD} is removed.

The resistor connected between the RI pin and the GND pin will create a precise $I_{(REF)}$ for the OCP function. The formula for choosing the RI resistor is $V_{(RI)}/I_{(REF)}$. The $I_{(REF)}$ range is from 12.5µA to 62.5µA. Three OCP comparators and the $I_{(REF)}$ section are supplied through the V12 pin. Current drawn from the VS12 pin is less than 1mA.

Following is an example on calculating OCP for the 12V rail:

$RI = V_{(RI)}/I_{(REF)} = 1.15V/20\mu A = 56K\Omega$

$I_{(REF)} \bullet C \bullet R_{(IS12)} = R_{(SENSE)} \bullet I_{(OCP\_TRIP)}$

$I_{(OCP\_TRIP)} = 20\mu A \bullet 8 \bullet 560\Omega/0.01\Omega = 9.2A$

C = Current Ratio (typically = 8)

OVER-VOLTAGE PROTECTION (OVP)

The Over-Voltage Protection (OVP) of the TPS3514 monitors 3.3V, 5V, and 12V. When an over-voltage condition appears at one of the 3.3V, 5V, or 12V input pins for more than 73µs, the $\overline{FPO}$ output goes HIGH and PGO goes LOW. Also, this fault condition will be latched until $\overline{PSON}$ is toggled from LOW-to-HIGH or V_{DD} is removed.

During fault conditions, most power supplies have the potential to deliver higher output voltages than those normally specified or required. In unprotected equipment, it is possible for output voltages to be high enough to cause internal or external damage of the system. To protect the system under these abnormal conditions, it is common practice to provide over-voltage protection within the power supply.

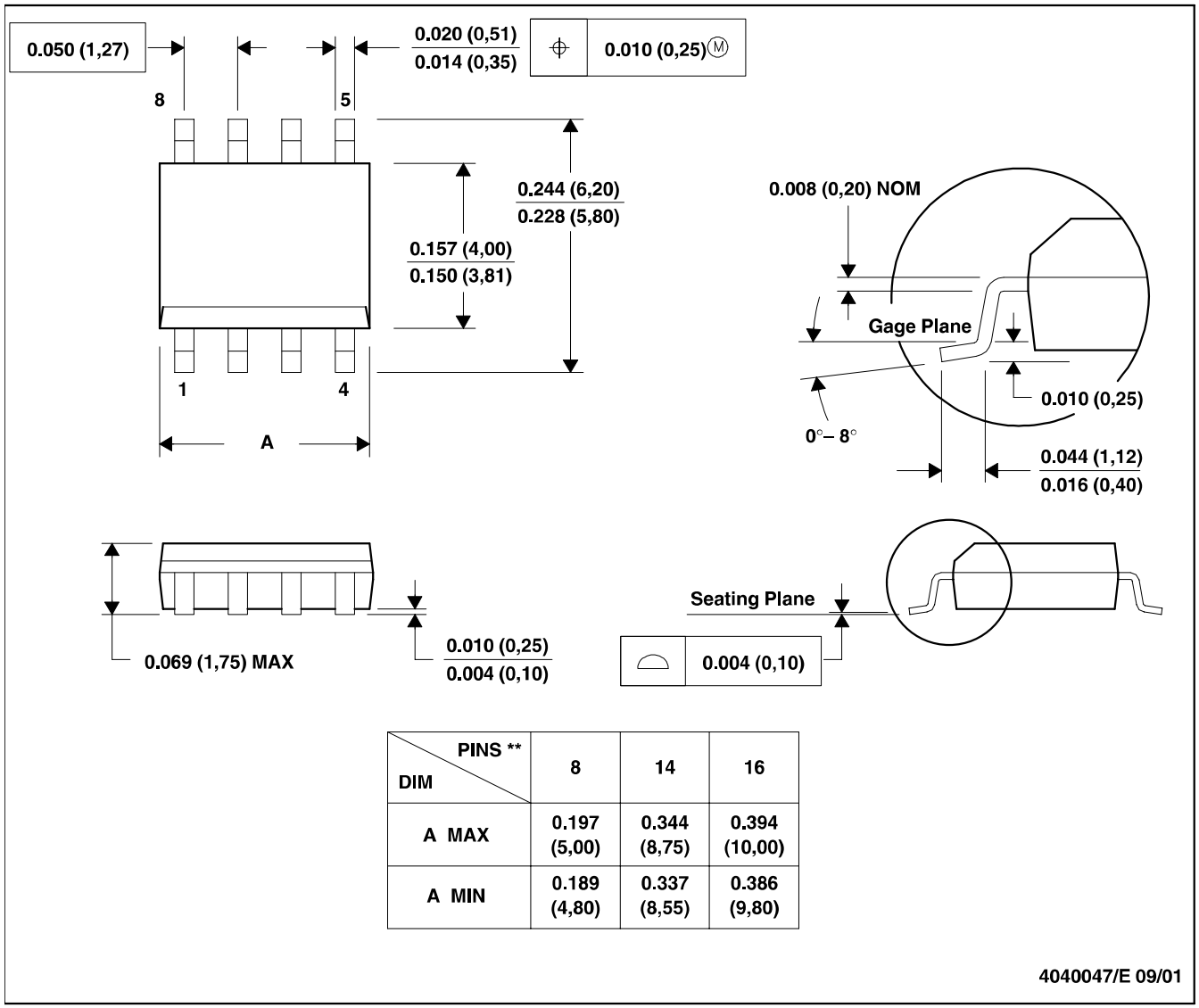
PACKAGE DRAWINGS

MSOI002B – JANUARY 1995 – REVISED SEPTEMBER 2001

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/E 09/01

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

PACKAGE DRAWINGS (Cont.)

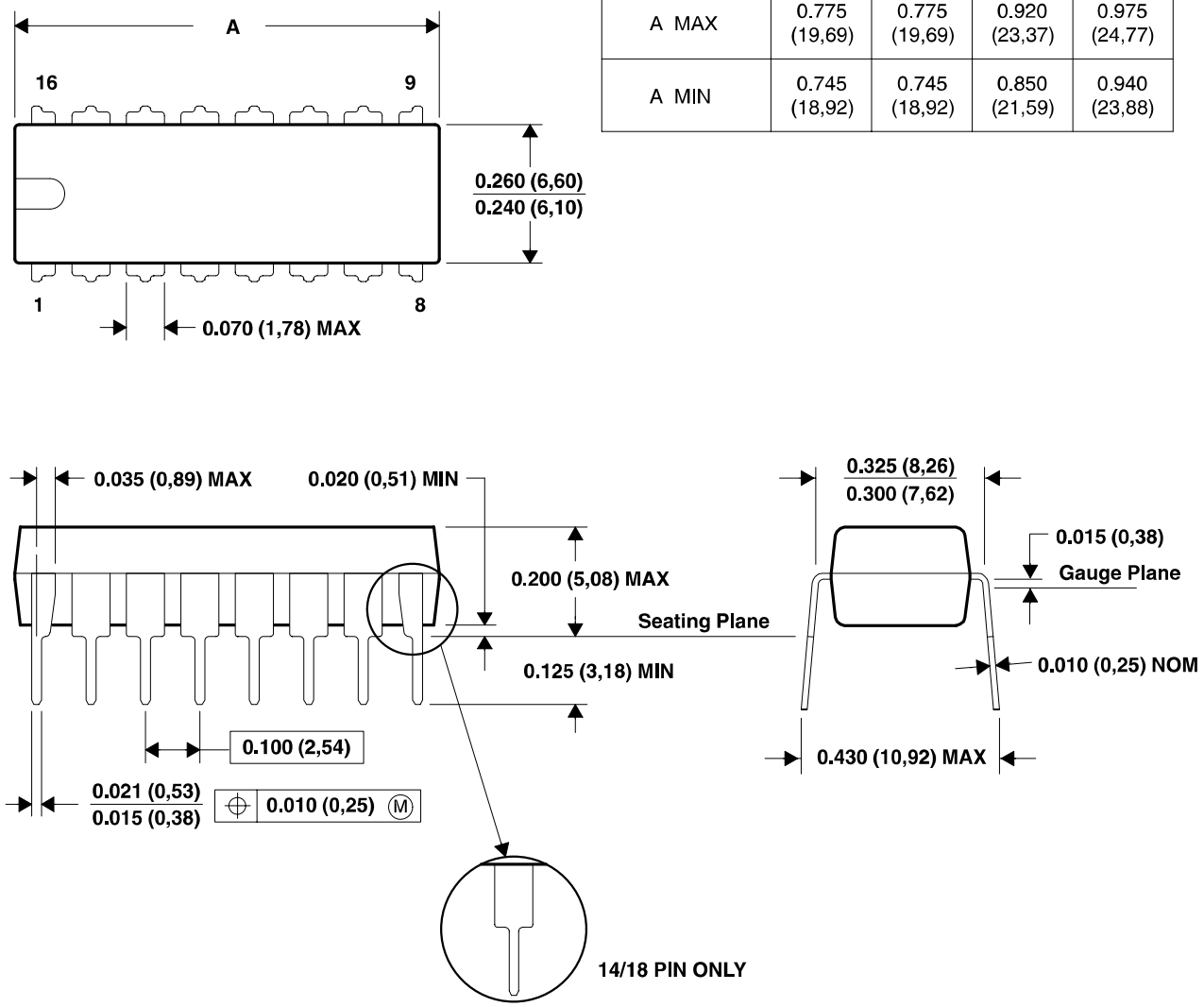
MPDI002B – JANUARY 1995 – REVISED FEBRUARY 2000

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	0.975 (24,77)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 (20-pin package is shorter than MS-001).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS3514D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TPS3514DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1YEAR/ Level-1-220C-UNLIM
TPS3514N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

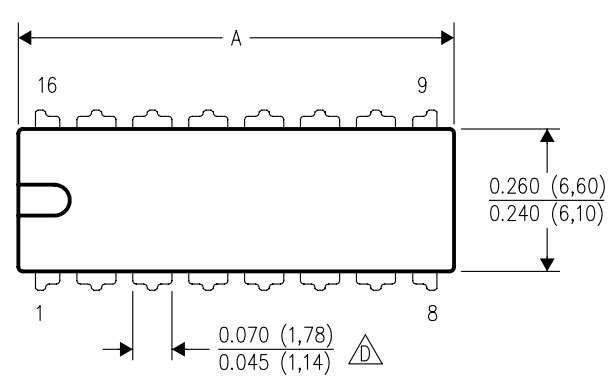
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

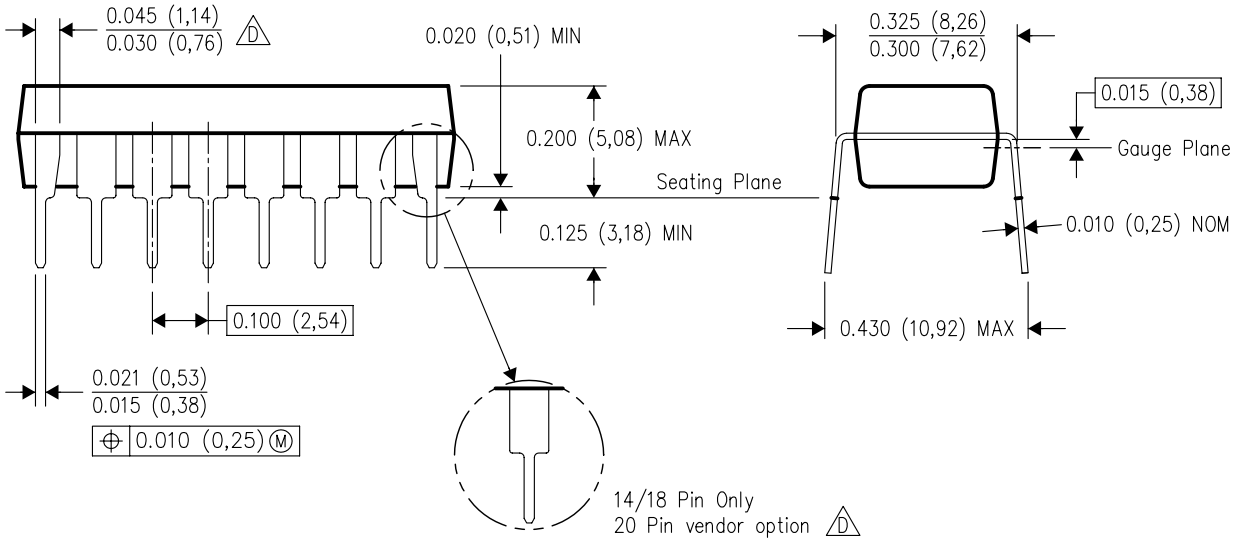
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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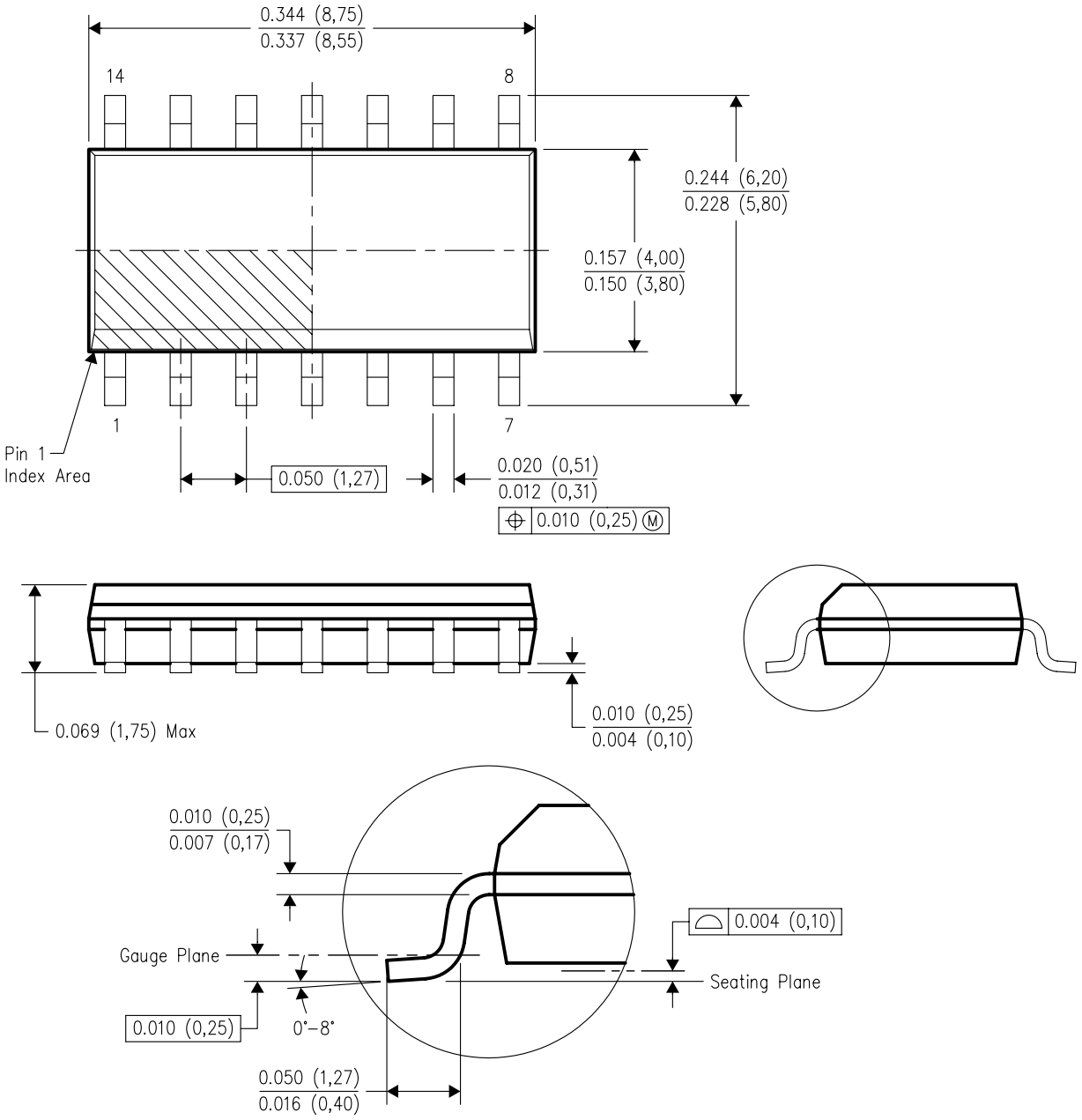
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–012 variation AB.

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