



100MS

## EMI SHIELD

### DESCRIPTION

The 100MS is an epoxy encapsulated electromagnetic/ electrostatic interference (EMI) shield for use with circuits where sensitivity to EMI is critical. It was designed to attenuate EMI by converting electromagnetic field energy into heat that is absorbed by the shield and by shunting electrostatic fields to common. The 100MS may be used in applications to either confine or exclude EMI. Its cavity was designed for 28.45mm x 28.45mm x 7.24mm, 20-pin hybrid packages. The shields in the cover and base plate are in two separate halves to maintain the electrical isolation between the adjacent rows of pins of the module it encloses. Because of the spacing between the shield halves and epoxy flow holes, the 100MS provides a partial, but adequate low reluctance path for electromagnetic flux. The 100MS is well suited for use with isolation modules such as the Burr-Brown 3656, 722, and 724.

### ASSEMBLY INSTRUCTIONS

Assemble the base plate to the module by pushing the pins of the module through the beveled holes in the base plate until the base plate and bottom of the module are in contact with each other. Place the cover

over the module so the tabs are aligned and fit into the slots in the base plate. Bend the four wide shield soldering tabs protruding from the cover to make contact with the bare metal on the base plate. Solder these four tabs to insure the integrity of their connection to the base plate.

The 100MS and the module it contains are mounted and secured to a printed circuit board (PCB) by soldering the two narrow PCB solder tabs to the appropriate common. The PCB solder tab closest to the input side of the module should be soldered to the input common. The other tab should be soldered to the output common. Figure 2 illustrates the assembly of the 100MS.

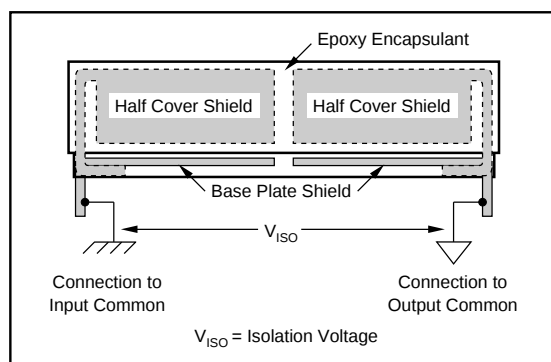


FIGURE 1. Cross-Sectional Side View of 100MS.

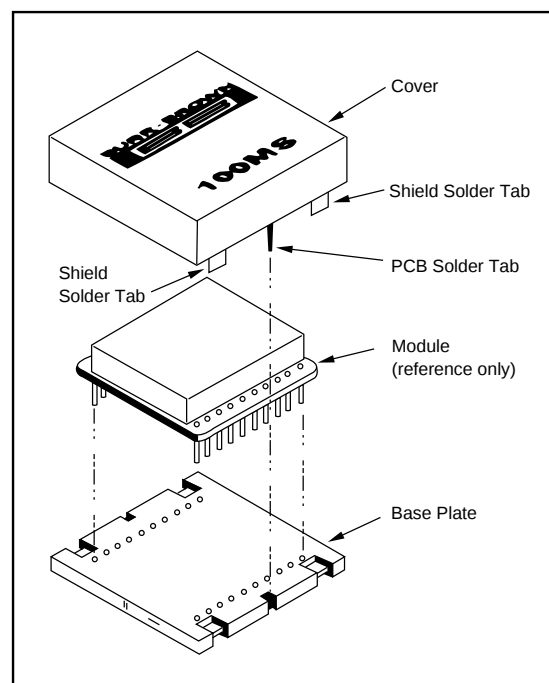


FIGURE 2. Assembly Diagram.

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# SPECIFICATIONS

## ELECTRICAL

Specifications apply between solder tabs.

| PARAMETER            | CONDITIONS | 100MS |           |     | UNITS    |
|----------------------|------------|-------|-----------|-----|----------|
|                      |            | MIN   | TYP       | MAX |          |
| Isolation Voltage    |            |       |           |     | VDC      |
| Rated Continuous, DC |            | 3500  |           |     | Vrms     |
| Rated Continuous, AC |            | 2000  |           |     | VDC      |
| Test                 | 10 Seconds | 8000  |           |     | pF       |
| Capacitance          |            |       | 5         |     | $\Omega$ |
| Resistance           |            |       | $10^{10}$ |     | $\mu A$  |
| Leakage Current      | 120V, 60Hz |       | 0.23      |     |          |

NOTE: Temperature changes ( $\Delta T/\Delta t$ ) greater than  $1^{\circ}\text{C}$  per minute below  $0^{\circ}\text{C}$  and long term storage above  $100^{\circ}\text{C}$  are not recommended.

## PACKAGE INFORMATION<sup>(1)</sup>

| MODEL | PACKAGE    | PACKAGE DRAWING NUMBER |
|-------|------------|------------------------|
| 100MS | EMI Shield | 124                    |

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## APPLICATIONS INFORMATION

### MULTIPLE DEVICE ORIENTATION

A typical application for the 100MS is shown in Figure 3. Using multiple devices within 30mm of each other can cause them to interact by forming beat frequency interference outputs. The 100MS can reduce this interference by as much as a factor of 200:1 depending on the distance between the devices and their relative orientation.

Minimum EMI results when the gaps of both shields are paralleled as in Figure 3a.

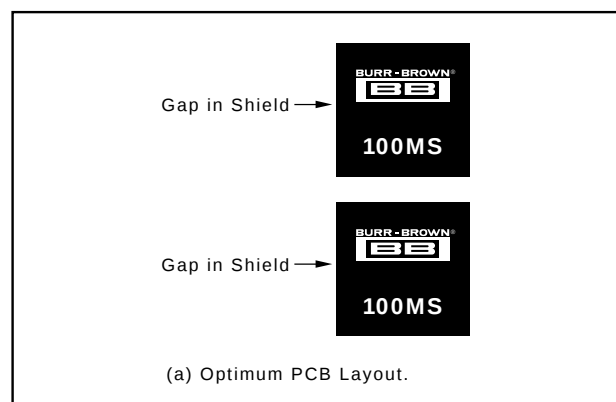


FIGURE 3a. Optimum PCB Layout. Orientation for minimum EMI.

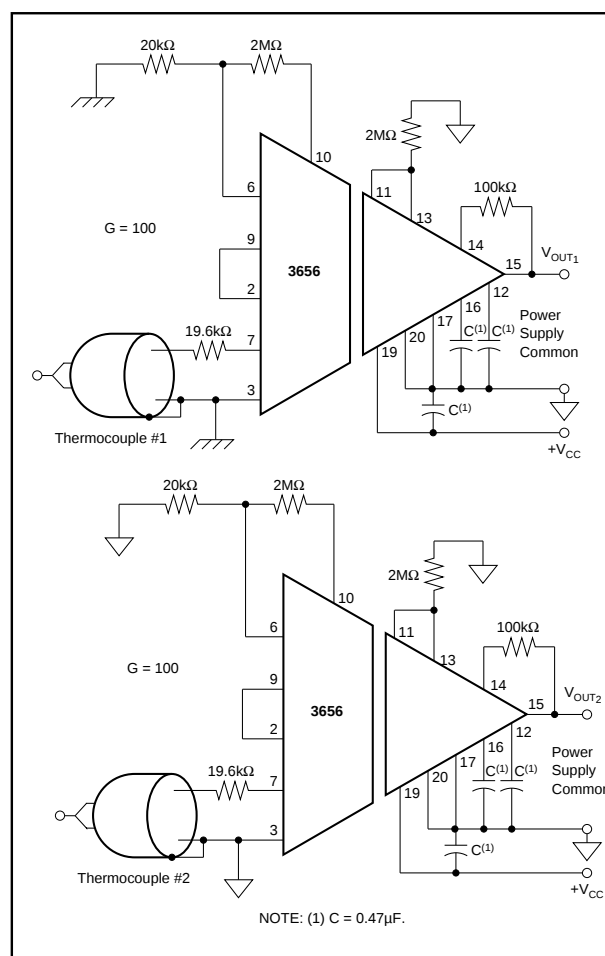


FIGURE 3b. Isolated Data Acquisition Input Circuitry. Orientation for Minimum EMI.

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## PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 0100MS           | ACTIVE                | PDIP         | NSP             | 20   | 25          | None                    | Call TI          | Level-NA-NA-NA               |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

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<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265

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